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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc206-h-mr

TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES (CONTINUED)
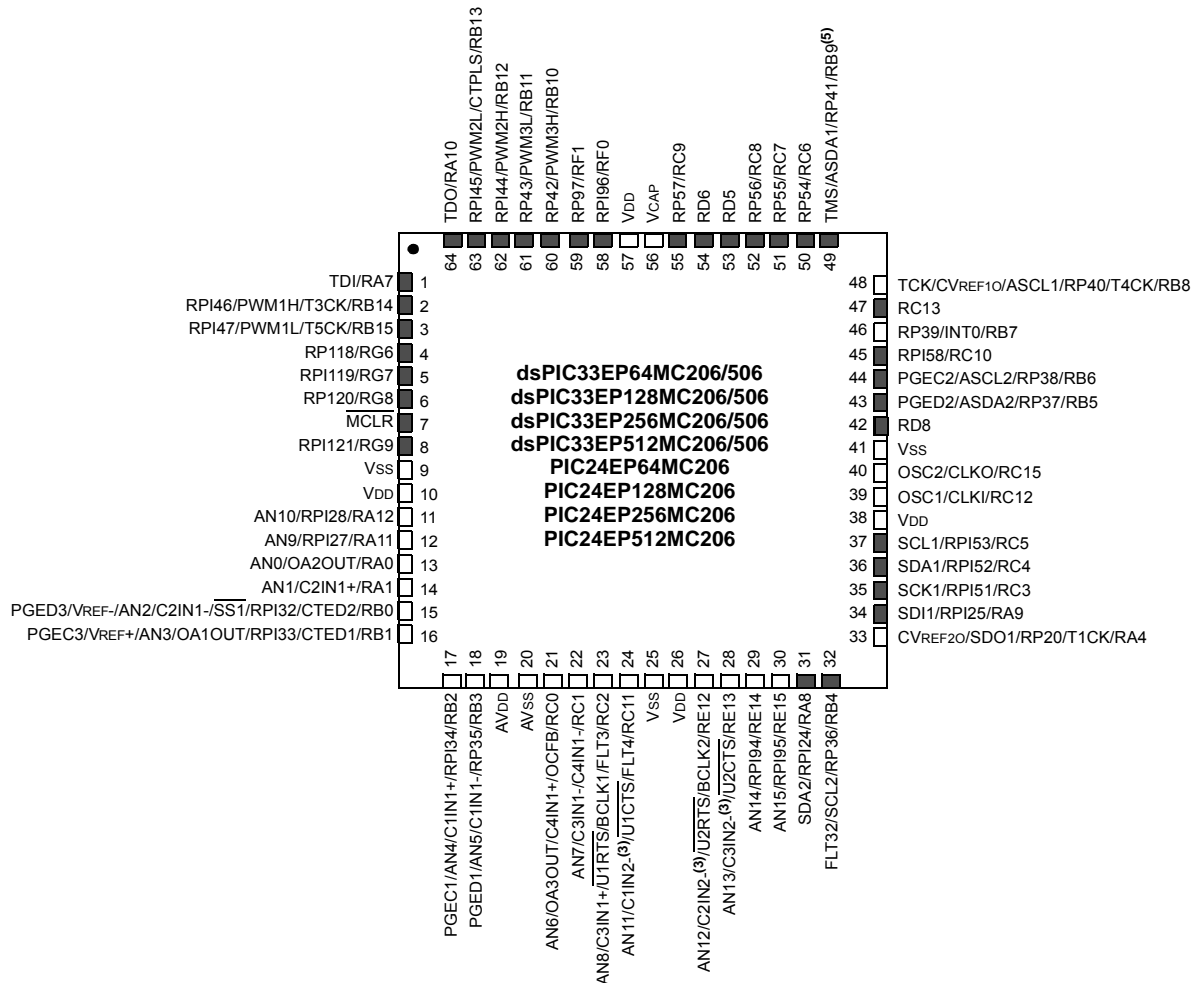
Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbytes)	Remappable Peripherals									I²C™	CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages
				16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM(4) (Channels)	Quadrature Encoder Interface	UART	SPI(2)	ECAN™ Technology	External Interrupts(3)									
dsPIC33EP32MC504	512	32	4	5	4	4	6	1	2	2	1	3	2	1	9	3/4	Yes	Yes	35	44/48	VTLA(5), TQFP, QFN, UQFN
dsPIC33EP64MC504	1024	64	8																		
dsPIC33EP128MC504	1024	128	16																		
dsPIC33EP256MC504	1024	256	32																		
dsPIC33EP512MC504	1024	512	48																		
dsPIC33EP64MC506	1024	64	8	5	4	4	6	1	2	2	1	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP128MC506	1024	128	16																		
dsPIC33EP256MC506	1024	256	32																		
dsPIC33EP512MC506	1024	512	48																		

Note 1: On 28-pin devices, Comparator 4 does not have external connections. Refer to **Section 25.0 "Op Amp/Comparator Module"** for details.
2: Only SPI2 is remappable.
3: INT0 is not remappable.
4: Only the PWM Faults are remappable.
5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

Pin Diagrams (Continued)

64-Pin QFN[1,2,3,4]

■ = Pins are up to 5V tolerant

Top-side pin labels (pins 64–49, left to right):
TDO/RA10 (64), RPI45/PWM2L/CTPLS/RB13 (63), RPI44/PWM2H/RB12 (62), RP43/PWM3L/RB11 (61), RP42/PWM3H/RB10 (60), RP97/RF1 (59), RPI96/RF0 (58), VDD (57), VCAP (56), RP57/RC9 (55), RD6 (54), RD5 (53), RP56/RC8 (52), RP55/RC7 (51), RP54/RC6 (50), TMS/ASDA1/RP41/RB9[5] (49)

Left-side pins (1–16):
Pin	Label
1	TDI/RA7
2	RPI46/PWM1H/T3CK/RB14
3	RPI47/PWM1L/T5CK/RB15
4	RP118/RG6
5	RPI119/RG7
6	RP120/RG8
7	MCLR
8	RPI121/RG9
9	VSS
10	VDD
11	AN10/RPI28/RA12
12	AN9/RPI27/RA11
13	AN0/OA2OUT/RA0
14	AN1/C2IN1+/RA1
15	PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
16	PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1

Device names (center):
dsPIC33EP64MC206/506
dsPIC33EP128MC206/506
dsPIC33EP256MC206/506
dsPIC33EP512MC206/506
PIC24EP64MC206
PIC24EP128MC206
PIC24EP256MC206
PIC24EP512MC206

Right-side pins (48–33):
Pin	Label
48	TCK/CVREF1O/ASCL1/RP40/T4CK/RB8
47	RC13
46	RP39/INT0/RB7
45	RPI58/RC10
44	PGEC2/ASCL2/RP38/RB6
43	PGED2/ASDA2/RP37/RB5
42	RD8
41	VSS
40	OSC2/CLKO/RC15
39	OSC1/CLKI/RC12
38	VDD
37	SCL1/RPI53/RC5
36	SDA1/RPI52/RC4
35	SCK1/RPI51/RC3
34	SDI1/RPI25/RA9
33	CVREF2O/SDO1/RP20/T1CK/RA4

Bottom-side pins (17–32, left to right):
PGEC1/AN4/C1IN1+/RPI34/RB2 (17), PGED1/AN5/C1IN1-/RP35/RB3 (18), AVDD (19), AVSS (20), AN6/OA3OUT/C4IN1+/OCFB/RC0 (21), AN7/C3IN1-/C4IN1-/RC1 (22), AN8/C3IN1+/U1RTS/BCLK1/FLT3/RC2 (23), AN11/C1IN2[3]/U1CTS/FLT4/RC11 (24), VSS (25), VDD (26), AN12/C2IN2[3]/U2RTS/BCLK2/RE12 (27), AN13/C3IN2[3]/U2CTS/RE13 (28), AN14/RPI94/RE14 (29), AN15/RPI95/RE15 (30), SDA2/RPI24/RA8 (31), FLT32/SCL2/RP36/RB4 (32)

Note
1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.
3: This pin is not available as an input when OPMODE (CMxCON<10>) = 1.
4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

- Four DMA channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode

- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU interrupt after half or full block transfer complete
- Byte or word transfers
- Fixed priority channel arbitration
- Manual (software) or automatic (peripheral DMA requests) transfer initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer is complete)
- DMA request for each channel can be selected from any supported interrupt source
- Debug support features

The peripherals that can utilize DMA are listed in Table 8-1.

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
INT0 – External Interrupt 0	00000000	—	—
IC1 – Input Capture 1	00000001	0x0144 (IC1BUF)	—
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	—
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	—
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	—
OC1 – Output Compare 1	00000010	—	0x0906 (OC1R) 0x0904 (OC1RS)
OC2 – Output Compare 2	00000110	—	0x0910 (OC2R) 0x090E (OC2RS)
OC3 – Output Compare 3	00011001	—	0x091A (OC3R) 0x0918 (OC3RS)
OC4 – Output Compare 4	00011010	—	0x0924 (OC4R) 0x0922 (OC4RS)
TMR2 – Timer2	00000111	—	—
TMR3 – Timer3	00001000	—	—
TMR4 – Timer4	00011011	—	—
TMR5 – Timer5	00011100	—	—
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	—
UART1TX – UART1 Transmitter	00001100	—	0x0224 (U1TXREG)
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	—
UART2TX – UART2 Transmitter	00011111	—	0x0234 (U2TXREG)
ECAN1 – RX Data Ready	00100010	0x0440 (C1RXD)	—
ECAN1 – TX Data Request	01000110	—	0x0442 (C1TXD)
ADC1 – ADC1 Convert Done	00001101	0x0300 (ADC1BUF0)	—

REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC4R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC3R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-8   **IC4R<6:0>:** Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

         1111001 = Input tied to RPI121

         .
         .
         .

         0000001 = Input tied to CMP1
         0000000 = Input tied to Vss

bit 7   **Unimplemented:** Read as '0'

bit 6-0   **IC3R<6:0>:** Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

         1111001 = Input tied to RPI121

         .
         .
         .

         0000001 = Input tied to CMP1
         0000000 = Input tied to Vss

NOTES:

14.1   Input Capture Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

14.1.1   KEY RESOURCES

• **"Input Capture"** (DS70352) in the *"dsPIC33/PIC24 Family Reference Manual"*
• Code Samples
• Application Notes
• Software Libraries
• Webinars
• All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
• Development Tools

REGISTER 16-12: TRGCONx: PWMx TRIGGER CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
TRGDIV<3:0>				—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TRGSTRT<5:0>[1]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **TRGDIV<3:0>:** Trigger # Output Divider bits

1111 = Trigger output for every 16th trigger event
1110 = Trigger output for every 15th trigger event
1101 = Trigger output for every 14th trigger event
1100 = Trigger output for every 13th trigger event
1011 = Trigger output for every 12th trigger event
1010 = Trigger output for every 11th trigger event
1001 = Trigger output for every 10th trigger event
1000 = Trigger output for every 9th trigger event
0111 = Trigger output for every 8th trigger event
0110 = Trigger output for every 7th trigger event
0101 = Trigger output for every 6th trigger event
0100 = Trigger output for every 5th trigger event
0011 = Trigger output for every 4th trigger event
0010 = Trigger output for every 3rd trigger event
0001 = Trigger output for every 2nd trigger event
0000 = Trigger output for every trigger event

bit 11-6 **Unimplemented:** Read as '0'

bit 5-0 **TRGSTRT<5:0>:** Trigger Postscaler Start Enable Select bits[1]

111111 = Waits 63 PWM cycles before generating the first trigger event after the module is enabled
•
•
•
000010 = Waits 2 PWM cycles before generating the first trigger event after the module is enabled
000001 = Waits 1 PWM cycle before generating the first trigger event after the module is enabled
000000 = Waits 0 PWM cycles before generating the first trigger event after the module is enabled

Note 1: The secondary PWM generator cannot generate PWMx trigger interrupts.

REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER[2]

R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD1[1]	PMOD0[1]	OVRENH	OVRENL
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PENH:** PWMxH Output Pin Ownership bit

1 = PWMx module controls PWMxH pin
0 = GPIO module controls PWMxH pin

bit 14 **PENL:** PWMxL Output Pin Ownership bit

1 = PWMx module controls PWMxL pin
0 = GPIO module controls PWMxL pin

bit 13 **POLH:** PWMxH Output Pin Polarity bit

1 = PWMxH pin is active-low
0 = PWMxH pin is active-high

bit 12 **POLL:** PWMxL Output Pin Polarity bit

1 = PWMxL pin is active-low
0 = PWMxL pin is active-high

bit 11-10 **PMOD<1:0>:** PWMx # I/O Pin Mode bits[1]

11 = Reserved; do not use
10 = PWMx I/O pin pair is in the Push-Pull Output mode
01 = PWMx I/O pin pair is in the Redundant Output mode
00 = PWMx I/O pin pair is in the Complementary Output mode

bit 9 **OVRENH:** Override Enable for PWMxH Pin bit

1 = OVRDAT<1> controls output on PWMxH pin
0 = PWMx generator controls PWMxH pin

bit 8 **OVRENL:** Override Enable for PWMxL Pin bit

1 = OVRDAT<0> controls output on PWMxL pin
0 = PWMx generator controls PWMxL pin

bit 7-6 **OVRDAT<1:0>:** Data for PWMxH, PWMxL Pins if Override is Enabled bits

If OVERENH = 1, PWMxH is driven to the state specified by OVRDAT<1>.
If OVERENL = 1, PWMxL is driven to the state specified by OVRDAT<0>.

bit 5-4 **FLTDAT<1:0>:** Data for PWMxH and PWMxL Pins if FLTMOD is Enabled bits

If Fault is active, PWMxH is driven to the state specified by FLTDAT<1>.
If Fault is active, PWMxL is driven to the state specified by FLTDAT<0>.

bit 3-2 **CLDAT<1:0>:** Data for PWMxH and PWMxL Pins if CLMOD is Enabled bits

If current-limit is active, PWMxH is driven to the state specified by CLDAT<1>.
If current-limit is active, PWMxL is driven to the state specified by CLDAT<0>.

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).

2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Quadrature Encoder Interface (QEI)"** (DS70601) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High register
- 32-Bit Position Compare Low register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

18.0 SERIAL PERIPHERAL INTERFACE (SPI)

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Serial Peripheral Interface (SPI)"** (DS70569) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with Motorola® SPI and SIOP interfaces.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X device family offers two SPI modules on a single device. These modules, which are designated as SPI1 and SPI2, are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

> **Note:** In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of the SPI2 module, but results in a lower maximum speed for SPI2. See **Section 30.0 "Electrical Characteristics"** for more information.

The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- SSx/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, SSx is not used. In 2-pin mode, neither SDOx nor SSx is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
   a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on $\overline{SSx}$.
   b) If FRMPOL = 0, use a pull-up resistor on $\overline{SSx}$.

Note:	This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode, (i.e., not using $\overline{SSx}$ from a master):
   a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on $\overline{SSx}$.
   b) If CKP = 0, always place a pull-down resistor on $\overline{SSx}$.

Note:	This will insure that during power-up and initialization the master/slave will not lose Sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the $\overline{SSx}$ pin, which indicates the start of a data frame.

Note:	Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in **Section 30.0 "Electrical Characteristics"** for details.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPIx data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

18.2.1 KEY RESOURCES

- **"Serial Peripheral Interface (SPI)"** (DS70569) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

20.3   UARTx Control Registers

REGISTER 20-1:   UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN[1]	—	USIDL	IREN[2]	RTSMD	—	UEN1	UEN0
bit 15							bit 8

R/W-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7							bit 0

Legend:		HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **UARTEN:** UARTx Enable bit[1]

    1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
    0 = UARTx is disabled; all UARTx pins are controlled by PORT latches; UARTx power consumption is minimal

bit 14   **Unimplemented:** Read as '0'

bit 13   **USIDL:** UARTx Stop in Idle Mode bit

    1 = Discontinues module operation when device enters Idle mode
    0 = Continues module operation in Idle mode

bit 12   **IREN:** IrDA® Encoder and Decoder Enable bit[2]

    1 = IrDA encoder and decoder are enabled
    0 = IrDA encoder and decoder are disabled

bit 11   **RTSMD:** Mode Selection for UxRTS Pin bit

    1 = UxRTS pin is in Simplex mode
    0 = UxRTS pin is in Flow Control mode

bit 10   **Unimplemented:** Read as '0'

bit 9-8   **UEN<1:0>:** UARTx Pin Enable bits

    11 = UxTX, UxRX and BCLKx pins are enabled and used; UxCTS pin is controlled by PORT latches[3]
    10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used[4]
    01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin is controlled by PORT latches[4]
    00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/BCLKx pins are controlled by PORT latches

bit 7   **WAKE:** Wake-up on Start bit Detect During Sleep Mode Enable bit

    1 = UARTx continues to sample the UxRX pin; interrupt is generated on the falling edge; bit is cleared in hardware on the following rising edge
    0 = No wake-up is enabled

bit 6   **LPBACK:** UARTx Loopback Mode Select bit

    1 = Enables Loopback mode
    0 = Loopback mode is disabled

Note 1: Refer to the **"UART"** (DS70582) section in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for receive or transmit operation.

    2: This feature is only available for the 16x BRG mode (BRGH = 0).

    3: This feature is only available on 44-pin and 64-pin devices.

    4: This feature is only available on 64-pin devices.

REGISTER 21-16: CxRXFnSID: ECANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	EXIDE	—	EID17	EID16
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-5 **SID<10:0>:** Standard Identifier bits

1 = Message address bit, SIDx, must be '1' to match filter
0 = Message address bit, SIDx, must be '0' to match filter

bit 4 **Unimplemented:** Read as '0'

bit 3 **EXIDE:** Extended Identifier Enable bit

If MIDE = 1:
1 = Matches only messages with Extended Identifier addresses
0 = Matches only messages with Standard Identifier addresses

If MIDE = 0:
Ignores EXIDE bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID<17:16>:** Extended Identifier bits

1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

REGISTER 22-3:   CTMUICON: CTMU CURRENT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10   **ITRIM<5:0>:** Current Source Trim bits

011111 = Maximum positive change from nominal current + 62%
011110 = Maximum positive change from nominal current + 60%

•

•

•

000010 = Minimum positive change from nominal current + 4%
000001 = Minimum positive change from nominal current + 2%
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current – 2%
111110 = Minimum negative change from nominal current – 4%

•

•

•

100010 = Maximum negative change from nominal current – 60%
100001 = Maximum negative change from nominal current – 62%

bit 9-8   **IRNG<1:0>:** Current Source Range Select bits

11 = 100 × Base Current[2]
10 = 10 × Base Current[2]
01 = Base Current Level[2]
00 = 1000 × Base Current[1,2]

bit 7-0   **Unimplemented:** Read as '0'

Note 1:   This current range is not available to be used with the internal temperature measurement diode.

   2:   Refer to the CTMU Current Source Specifications (Table 30-56) in **Section 30.0 "Electrical Characteristics"** for the current range selection values.

24.3 PTG Control Registers

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT[2]	PTGSSEN[3]	PTGIVIS
bit 15							bit 8

R/W-0	HS-0	U-0	U-0	U-0	U-0	R/W-0	
PTGSTRT	PTGWDTO	—	—	—	—	PTGITM1[1]	PTGITM0[1]
bit 7							bit 0

Legend:		HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PTGEN:** Module Enable bit

1 = PTG module is enabled
0 = PTG module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTGSIDL:** PTG Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **PTGTOGL:** PTG TRIG Output Toggle Mode bit

1 = Toggle state of the PTGOx for each execution of the PTGTRIG command
0 = Each execution of the PTGTRIG command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits

bit 11 **Unimplemented:** Read as '0'

bit 10 **PTGSWT:** PTG Software Trigger bit[2]

1 = Triggers the PTG module
0 = No action (clearing this bit will have no effect)

bit 9 **PTGSSEN:** PTG Enable Single-Step bit[3]

1 = Enables Single-Step mode
0 = Disables Single-Step mode

bit 8 **PTGIVIS:** PTG Counter/Timer Visibility Control bit

1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)
0 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those limit registers

bit 7 **PTGSTRT:** PTG Start Sequencer bit

1 = Starts to sequentially execute commands (Continuous mode)
0 = Stops executing commands

bit 6 **PTGWDTO:** PTG Watchdog Timer Time-out Status bit

1 = PTG Watchdog Timer has timed out
0 = PTG Watchdog Timer has not timed out.

bit 5-2 **Unimplemented:** Read as '0'

Note 1: These bits apply to the PTGWHI and PTGWLO commands only.

2: This bit is only used with the PTGCTRL step command software trigger option.

3: Use of the PTG Single-Step mode is reserved for debugging tools only.

REGISTER 24-2: PTGCON: PTG CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13   **PTGCLK<2:0>:** Select PTG Module Clock Source bits

111 = Reserved
110 = Reserved
101 = PTG module clock source will be T3CLK
100 = PTG module clock source will be T2CLK
011 = PTG module clock source will be T1CLK
010 = PTG module clock source will be T_{AD}
001 = PTG module clock source will be F_{OSC}
000 = PTG module clock source will be F_P

bit 12-8   **PTGDIV<4:0>:** PTG Module Clock Prescaler (divider) bits

11111 = Divide-by-32
11110 = Divide-by-31
•
•
•
00001 = Divide-by-2
00000 = Divide-by-1

bit 7-4   **PTGPWD<3:0>:** PTG Trigger Output Pulse-Width bits

1111 = All trigger outputs are 16 PTG clock cycles wide
1110 = All trigger outputs are 15 PTG clock cycles wide
•
•
•
0001 = All trigger outputs are 2 PTG clock cycles wide
0000 = All trigger outputs are 1 PTG clock cycle wide

bit 3   **Unimplemented:** Read as '0'

bit 2-0   **PTGWDT<2:0>:** Select PTG Watchdog Timer Time-out Count Value bits

111 = Watchdog Timer will time-out after 512 PTG clocks
110 = Watchdog Timer will time-out after 256 PTG clocks
101 = Watchdog Timer will time-out after 128 PTG clocks
100 = Watchdog Timer will time-out after 64 PTG clocks
011 = Watchdog Timer will time-out after 32 PTG clocks
010 = Watchdog Timer will time-out after 16 PTG clocks
001 = Watchdog Timer will time-out after 8 PTG clocks
000 = Watchdog Timer is disabled

30.0   ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings[1]

Ambient temperature under bias..-40°C to +125°C

Storage temperature ....-65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} .... -0.3V to +4.0V

Voltage on any pin that is not 5V tolerant, with respect to V_{SS}[3]..-0.3V to (V_{DD} + 0.3V)

Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 3.0V$[3].. -0.3V to +5.5V

Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} < 3.0V$[3].. -0.3V to +3.6V

Maximum current out of V_{SS} pin ....300 mA

Maximum current into V_{DD} pin[2]...300 mA

Maximum current sunk/sourced by any 4x I/O pin ....15 mA

Maximum current sunk/sourced by any 8x I/O pin ....25 mA

Maximum current sunk by all ports[2,4] ....200 mA

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

3: See the **"Pin Diagrams"** section for the 5V tolerant pins.

4: Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.
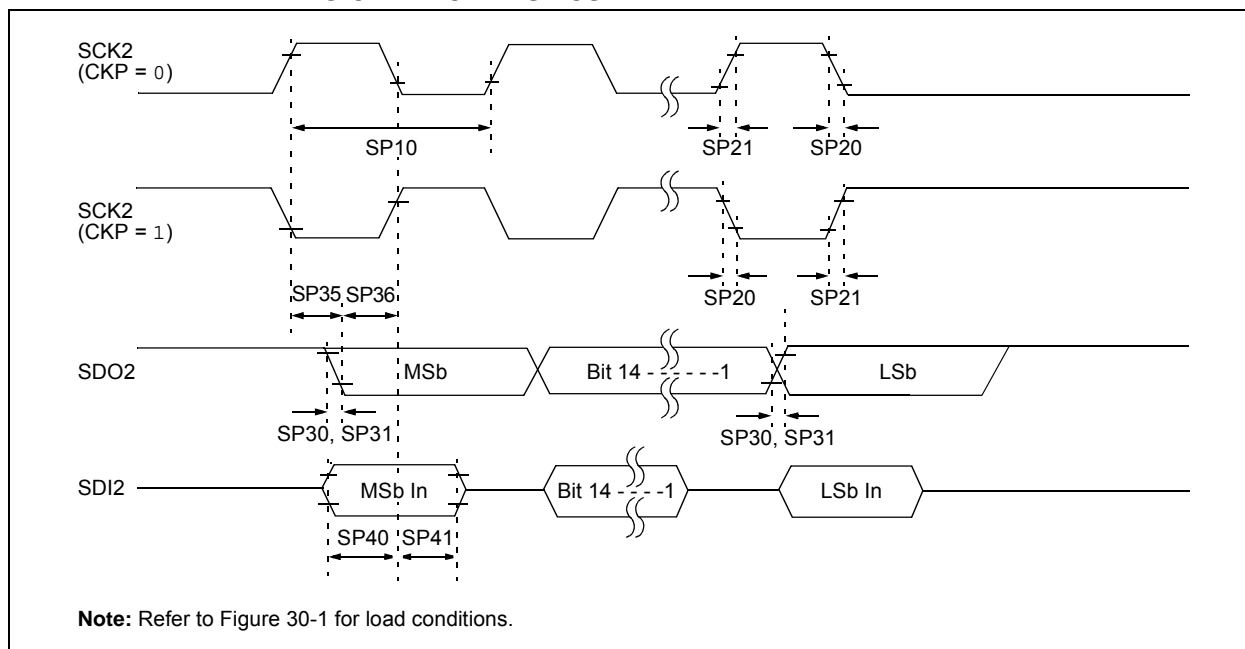

TABLE 30-6:   DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	Typ.	Max.	Units	Conditions		
Operating Current (IDD)[1]						
DC20d	9	15	mA	-40°C	3.3V	10 MIPS
DC20a	9	15	mA	+25°C		
DC20b	9	15	mA	+85°C		
DC20c	9	15	mA	+125°C		
DC22d	16	25	mA	-40°C	3.3V	20 MIPS
DC22a	16	25	mA	+25°C		
DC22b	16	25	mA	+85°C		
DC22c	16	25	mA	+125°C		
DC24d	27	40	mA	-40°C	3.3V	40 MIPS
DC24a	27	40	mA	+25°C		
DC24b	27	40	mA	+85°C		
DC24c	27	40	mA	+125°C		
DC25d	36	55	mA	-40°C	3.3V	60 MIPS
DC25a	36	55	mA	+25°C		
DC25b	36	55	mA	+85°C		
DC25c	36	55	mA	+125°C		
DC26d	41	60	mA	-40°C	3.3V	70 MIPS
DC26a	41	60	mA	+25°C		
DC26b	41	60	mA	+85°C		

Note 1:   IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:
- Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing while(1){NOP();} statement
- JTAG is disabled

FIGURE 30-17: **SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)**
TIMING CHARACTERISTICS

Note: Refer to Figure 30-1 for load conditions.

TABLE 30-36: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	-40ºC to +125ºC **(Note 3)**
SP20	TscF	SCK2 Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP21	TscR	SCK2 Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

   2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

   3: The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

   4: Assumes 50 pF load on all SPI2 pins.

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
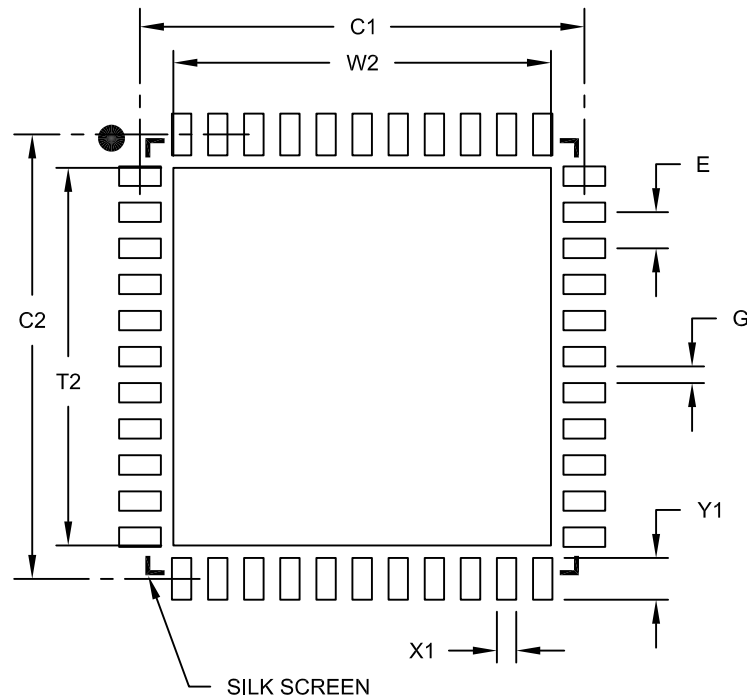
RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B