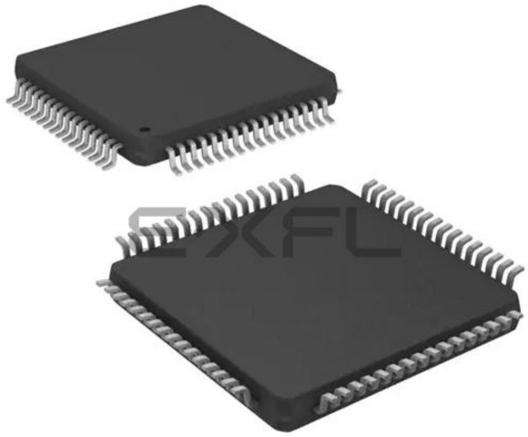
# Microchip Technology - DSPIC33EP128MC206-I/PT Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

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| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | I²C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 128KB (43K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 16x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc206-i-pt |

### 4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-6).

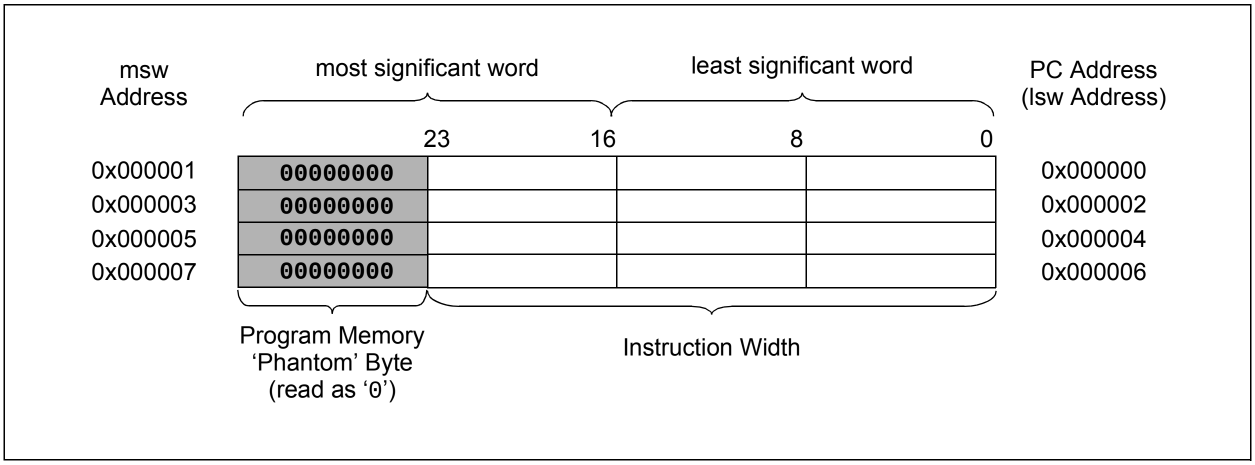
Program memory addresses are always word-aligned on the lower word and addresses are incremented, or decremented by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

### 4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A `GOTO` instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 7.1 “Interrupt Vector Table”**.

**FIGURE 4-6: PROGRAM MEMORY ORGANIZATION**



## 4.4 Special Function Register Maps

### TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND dsPIC33EPXXXGP50X DEVICES ONLY

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W0 | 0000 | W0 (WREG) | | | | | | | | | | | | | | | | xxxx |
| W1 | 0002 | W1 | | | | | | | | | | | | | | | | xxxx |
| W2 | 0004 | W2 | | | | | | | | | | | | | | | | xxxx |
| W3 | 0006 | W3 | | | | | | | | | | | | | | | | xxxx |
| W4 | 0008 | W4 | | | | | | | | | | | | | | | | xxxx |
| W5 | 000A | W5 | | | | | | | | | | | | | | | | xxxx |
| W6 | 000C | W6 | | | | | | | | | | | | | | | | xxxx |
| W7 | 000E | W7 | | | | | | | | | | | | | | | | xxxx |
| W8 | 0010 | W8 | | | | | | | | | | | | | | | | xxxx |
| W9 | 0012 | W9 | | | | | | | | | | | | | | | | xxxx |
| W10 | 0014 | W10 | | | | | | | | | | | | | | | | xxxx |
| W11 | 0016 | W11 | | | | | | | | | | | | | | | | xxxx |
| W12 | 0018 | W12 | | | | | | | | | | | | | | | | xxxx |
| W13 | 001A | W13 | | | | | | | | | | | | | | | | xxxx |
| W14 | 001C | W14 | | | | | | | | | | | | | | | | xxxx |
| W15 | 001E | W15 | | | | | | | | | | | | | | | | xxxx |
| SPLIM | 0020 | SPLIM | | | | | | | | | | | | | | | | 0000 |
| ACCAL | 0022 | ACCAL | | | | | | | | | | | | | | | | 0000 |
| ACCAH | 0024 | ACCAH | | | | | | | | | | | | | | | | 0000 |
| ACCAU | 0026 | Sign Extension of ACCA<39> | | | | | | | | ACCAU | | | | | | | | 0000 |
| ACCBL | 0028 | ACCBL | | | | | | | | | | | | | | | | 0000 |
| ACCBH | 002A | ACCBH | | | | | | | | | | | | | | | | 0000 |
| ACCBU | 002C | Sign Extension of ACCB<39> | | | | | | | | ACCBU | | | | | | | | 0000 |
| PCL | 002E | PCL<15:0> | | | | | | | | | | | | | | | — | 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | — | PCH<6:0> | | | | | | | 0000 |
| DSRPAG | 0032 | — | — | — | — | — | — | DSRPAG<9:0> | | | | | | | | | | 0001 |
| DSWPAG | 0034 | — | — | — | — | — | — | — | DSWPAG<8:0> | | | | | | | | | 0001 |
| RCOUNT | 0036 | RCOUNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| DCOUNT | 0038 | DCOUNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| DOSTARTL | 003A | DOSTARTL<15:1> | | | | | | | | | | | | | | | — | 0000 |
| DOSTARTH | 003C | — | — | — | — | — | — | — | — | — | — | DOSTARTH<5:0> | | | | | | 0000 |
| DOENDL | 003E | DOENDL<15:1> | | | | | | | | | | | | | | | — | 0000 |
| DOENDH | 0040 | — | — | — | — | — | — | — | — | — | — | DOENDH<5:0> | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

### REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CHEN | SIZE | DIR | HALF | NULLW | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | AMODE1 | AMODE0 | — | — | MODE1 | MODE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **CHEN:** DMA Channel Enable bit

1 = Channel is enabled
0 = Channel is disabled

bit 14 **SIZE:** DMA Data Transfer Size bit

1 = Byte
0 = Word

bit 13 **DIR:** DMA Transfer Direction bit (source/destination bus select)

1 = Reads from RAM address, writes to peripheral address
0 = Reads from peripheral address, writes to RAM address

bit 12 **HALF:** DMA Block Transfer Interrupt Select bit

1 = Initiates interrupt when half of the data has been moved
0 = Initiates interrupt when all of the data has been moved

bit 11 **NULLW:** Null Data Peripheral Write Mode Select bit

1 = Null data write to peripheral in addition to RAM write (DIR bit must also be clear)
0 = Normal operation

bit 10-6 **Unimplemented:** Read as ‘0’

bit 5-4 **AMODE<1:0>:** DMA Channel Addressing Mode Select bits

11 = Reserved
10 = Peripheral Indirect Addressing mode
01 = Register Indirect without Post-Increment mode
00 = Register Indirect with Post-Increment mode

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1-0 **MODE<1:0>:** DMA Channel Operating Mode Select bits

11 = One-Shot, Ping-Pong modes are enabled (one block transfer from/to each DMA buffer)
10 = Continuous, Ping-Pong modes are enabled
01 = One-Shot, Ping-Pong modes are disabled
00 = Continuous, Ping-Pong modes are disabled

## 11.5 I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 30-11, under "Injection Current", have internal protection diodes to VDD and VSS. The term, "Injection Current", is also referred to as "Clamp Current". On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device, that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '`0`', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '`0`'.

> **Note:** Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD – 0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH, and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:

   VOH = 2.4V @ IOH = -8 mA and VDD = 3.3V

   The maximum output current sourced by any 8 mA I/O pin = 12 mA.

   LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in **Section 30.0 "Electrical Characteristics"** for additional information.
6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
   a) Only one "output" function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
   b) It is possible to assign a "remappable output" function to multiple pins and externally short or tie them together for increased current drive.
   c) If any "dedicated output" function is enabled on a pin, it will take precedence over any remappable "output" function.
   d) If any "dedicated digital" (input or output) function is enabled on a pin, any number of "input" remappable functions can be mapped to the same pin.
   e) If any "dedicated analog" function(s) are enabled on a given pin, "digital input(s)" of any kind will all be disabled, although a single "digital output", at the user's cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input provided there is no external analog input, such as for a built-in self-test.
   f) Any number of "input" remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable "output".

g) The TRISx registers control *only* the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRIS setting. The TRISx register *does not* control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRIS settings, which means that the TRISx bit must be set to input for pins with only remappable input function(s) assigned

h) All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin has been disabled. Only the Analog Pin Select registers control the digital input buffer, *not* the TRISx register. The user must disable the analog function on a pin using the Analog Pin Select registers in order to use any “digital input(s)” on a corresponding pin, no exceptions.

## 11.6 I/O Ports Resources

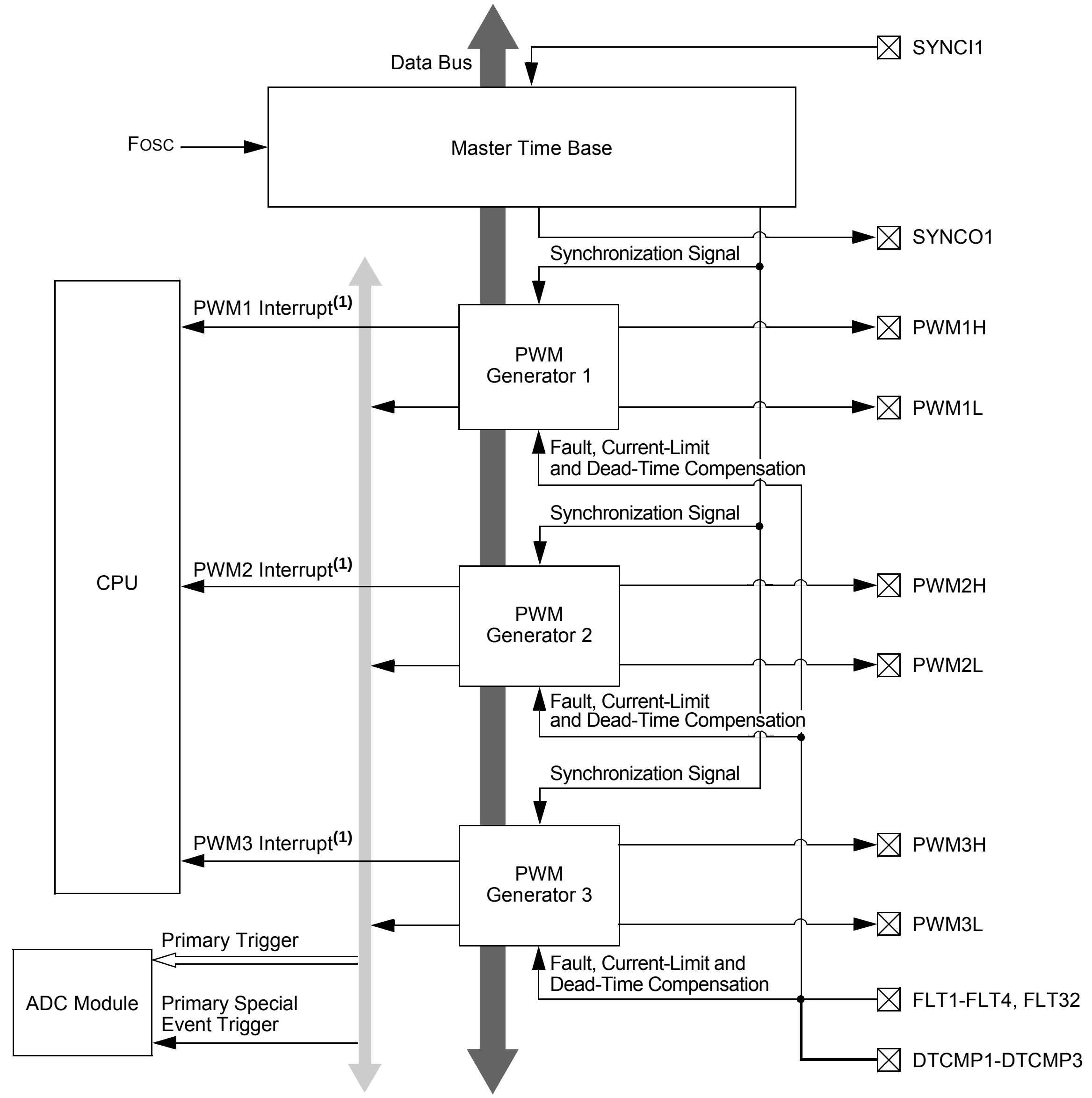
Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser:<br>http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 11.6.1 KEY RESOURCES

- **“I/O Ports”** (DS70598) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

**FIGURE 16-1: HIGH-SPEED PWMx MODULE ARCHITECTURAL OVERVIEW**



**Note 1:** The PWM interrupts are generated by logically ORing the FLTSTAT, CLSTAT and TRGSTAT status bits for the given PWM generator. Refer to the "*dsPIC33/PIC24 Family Reference Manual*", **"High-Speed PWM"** (DS70645) for more information.

## 16.3 PWMx Control Registers

### REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R/W-0 | U-0 | R/W-0 | HS/HC-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PTEN | — | PTSIDL | SESTAT | SEIEN | EIPU(1) | SYNCPOL(1) | SYNCOEN(1) |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SYNCEN(1) | SYNCSRC2(1) | SYNCSRC1(1) | SYNCSRC0(1) | SEVTPS3(1) | SEVTPS2(1) | SEVTPS1(1) | SEVTPS0(1) |
| bit 7 | | | | | | | bit 0 |

| | | | |
|---|---|---|---|
| **Legend:** | HC = Hardware Clearable bit | HS = Hardware Settable bit | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **PTEN:** PWMx Module Enable bit

1 = PWMx module is enabled
0 = PWMx module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **PTSIDL:** PWMx Time Base Stop in Idle Mode bit

1 = PWMx time base halts in CPU Idle mode
0 = PWMx time base runs in CPU Idle mode

bit 12 **SESTAT:** Special Event Interrupt Status bit

1 = Special event interrupt is pending
0 = Special event interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit

1 = Special event interrupt is enabled
0 = Special event interrupt is disabled

bit 10 **EIPU:** Enable Immediate Period Updates bit(1)

1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWMx cycle boundaries

bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit(1)

1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
0 = SYNCI1/SYNCO1 is active-high

bit 8 **SYNCOEN:** Primary Time Base Sync Enable bit(1)

1 = SYNCO1 output is enabled
0 = SYNCO1 output is disabled

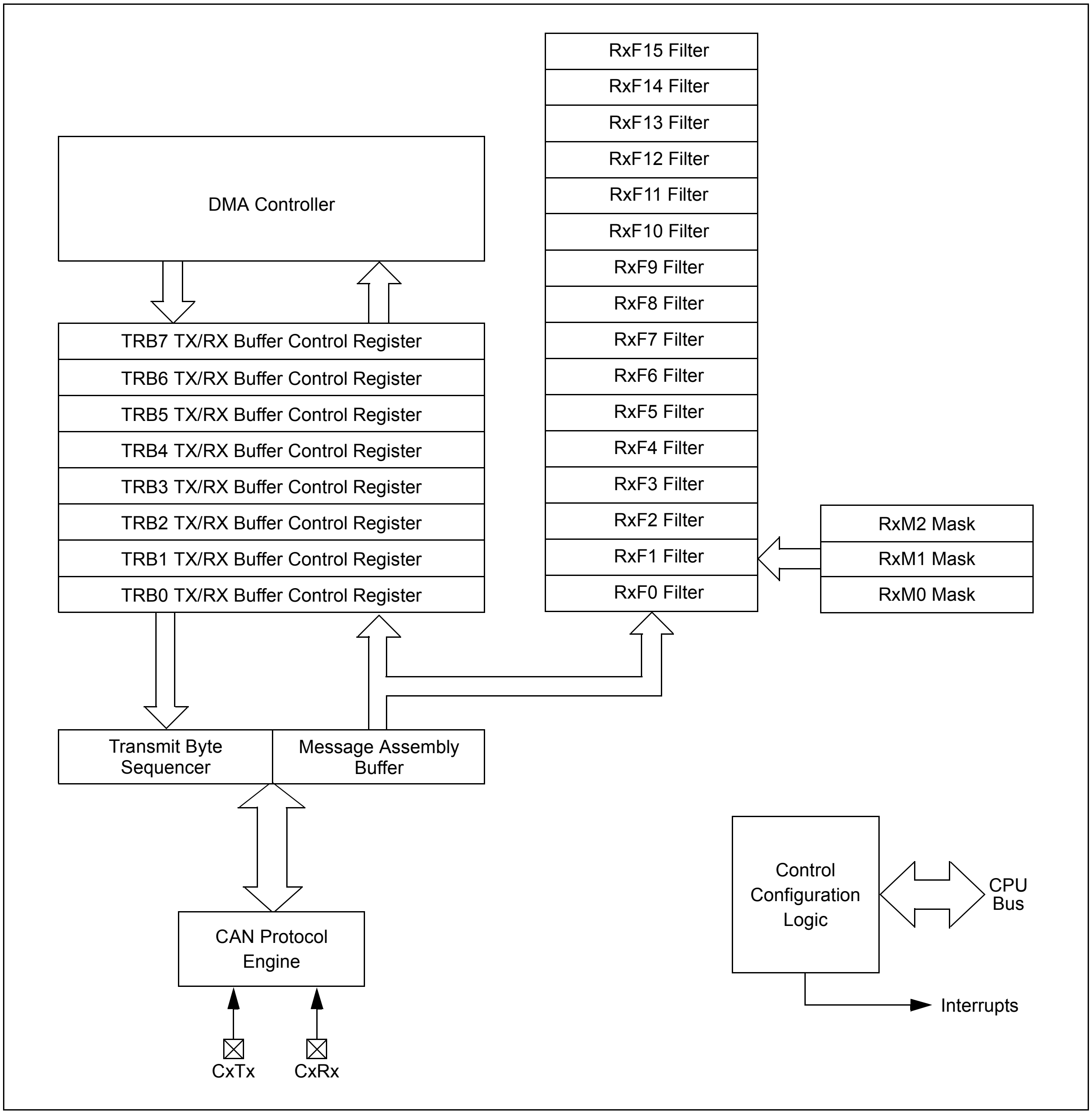
bit 7 **SYNCEN:** External Time Base Synchronization Enable bit(1)

1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

**Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.

**2:** See **Section 24.0 “Peripheral Trigger Generator (PTG) Module”** for information on this selection.

**FIGURE 21-1: ECAN™ MODULE BLOCK DIAGRAM**



## 21.2 Modes of Operation

The ECAN module can operate in one of several operation modes selected by the user. These modes include:

- Initialization mode
- Disable mode
- Normal Operation mode
- Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

## 21.3 ECAN Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser:<br>http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |
|---|---|

### 21.3.1 KEY RESOURCES

- **"Enhanced Controller Area Network (ECAN™)"** (DS70353) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

### REGISTER 23-5: AD1CHS123: ADC1 INPUT CHANNEL 1, 2, 3 SELECT REGISTER

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | CH123NB1 | CH123NB0 | CH123SB |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | CH123NA1 | CH123NA0 | CH123SA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as ‘`0`’

bit 10-9 **CH123NB<1:0>:** Channel 1, 2, 3 Negative Input Select for Sample MUXB bits

In 12-bit mode (AD21B = `1`), CH123NB is Unimplemented and is Read as ‘`0`’:

| **Value** | **ADC Channel** | | |
|---|---|---|---|
| | **CH1** | **CH2** | **CH3** |
| `11` | AN9 | AN10 | AN11 |
| `10`(1,2) | OA3/AN6 | AN7 | AN8 |
| `0x` | VREFL | VREFL | VREFL |

bit 8 **CH123SB:** Channel 1, 2, 3 Positive Input Select for Sample MUXB bit

In 12-bit mode (AD21B = `1`), CH123SB is Unimplemented and is Read as ‘`0`’:

| **Value** | **ADC Channel** | | |
|---|---|---|---|
| | **CH1** | **CH2** | **CH3** |
| `1`(2) | OA1/AN3 | OA2/AN0 | OA3/AN6 |
| `0`(1,2) | OA2/AN0 | AN1 | AN2 |

bit 7-3 **Unimplemented:** Read as ‘`0`’

bit 2-1 **CH123NA<1:0>:** Channel 1, 2, 3 Negative Input Select for Sample MUXA bits

In 12-bit mode (AD21B = `1`), CH123NA is Unimplemented and is Read as ‘`0`’:

| **Value** | **ADC Channel** | | |
|---|---|---|---|
| | **CH1** | **CH2** | **CH3** |
| `11` | AN9 | AN10 | AN11 |
| `10`(1,2) | OA3/AN6 | AN7 | AN8 |
| `0x` | VREFL | VREFL | VREFL |

**Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

**2:** The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = `1`); otherwise, the ANx input is used.

**TABLE 24-2: PTG OUTPUT DESCRIPTIONS**

| PTG Output Number | PTG Output Description |
|---|---|
| PTGO0 | Trigger/Synchronization Source for OC1 |
| PTGO1 | Trigger/Synchronization Source for OC2 |
| PTGO2 | Trigger/Synchronization Source for OC3 |
| PTGO3 | Trigger/Synchronization Source for OC4 |
| PTGO4 | Clock Source for OC1 |
| PTGO5 | Clock Source for OC2 |
| PTGO6 | Clock Source for OC3 |
| PTGO7 | Clock Source for OC4 |
| PTGO8 | Trigger/Synchronization Source for IC1 |
| PTGO9 | Trigger/Synchronization Source for IC2 |
| PTGO10 | Trigger/Synchronization Source for IC3 |
| PTGO11 | Trigger/Synchronization Source for IC4 |
| PTGO12 | Sample Trigger for ADC |
| PTGO13 | Sample Trigger for ADC |
| PTGO14 | Sample Trigger for ADC |
| PTGO15 | Sample Trigger for ADC |
| PTGO16 | PWM Time Base Synchronous Source for PWM(1) |
| PTGO17 | PWM Time Base Synchronous Source for PWM(1) |
| PTGO18 | Mask Input Select for Op Amp/Comparator |
| PTGO19 | Mask Input Select for Op Amp/Comparator |
| PTGO20 | Reserved |
| PTGO21 | Reserved |
| PTGO22 | Reserved |
| PTGO23 | Reserved |
| PTGO24 | Reserved |
| PTGO25 | Reserved |
| PTGO26 | Reserved |
| PTGO27 | Reserved |
| PTGO28 | Reserved |
| PTGO29 | Reserved |
| PTGO30 | PTG Output to PPS Input Selection |
| PTGO31 | PTG Output to PPS Input Selection |

**Note 1:** This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT ($I_{IDLE}$)**

| DC CHARACTERISTICS | | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ $T_A$ ≤ +85°C for Industrial<br>-40°C ≤ $T_A$ ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typ.** | **Max.** | **Units** | **Conditions** | | |
| **Idle Current ($I_{IDLE}$)(1)** | | | | | | |
| DC40d | 3 | 8 | mA | -40°C | 3.3V | 10 MIPS |
| DC40a | 3 | 8 | mA | +25°C | | |
| DC40b | 3 | 8 | mA | +85°C | | |
| DC40c | 3 | 8 | mA | +125°C | | |
| DC42d | 6 | 12 | mA | -40°C | 3.3V | 20 MIPS |
| DC42a | 6 | 12 | mA | +25°C | | |
| DC42b | 6 | 12 | mA | +85°C | | |
| DC42c | 6 | 12 | mA | +125°C | | |
| DC44d | 11 | 18 | mA | -40°C | 3.3V | 40 MIPS |
| DC44a | 11 | 18 | mA | +25°C | | |
| DC44b | 11 | 18 | mA | +85°C | | |
| DC44c | 11 | 18 | mA | +125°C | | |
| DC45d | 17 | 27 | mA | -40°C | 3.3V | 60 MIPS |
| DC45a | 17 | 27 | mA | +25°C | | |
| DC45b | 17 | 27 | mA | +85°C | | |
| DC45c | 17 | 27 | mA | +125°C | | |
| DC46d | 20 | 35 | mA | -40°C | 3.3V | 70 MIPS |
| DC46a | 20 | 35 | mA | +25°C | | |
| DC46b | 20 | 35 | mA | +85°C | | |

**Note 1:** Base Idle current ($I_{IDLE}$) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to $V_{SS}$
- $\overline{MCLR}$ = $V_{DD}$, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = `1` (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = `0` (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

### TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| | $I_{IL}$ | **Input Leakage Current**(1,2) | | | | | |
| DI50 | | I/O Pins 5V Tolerant(3) | -1 | — | +1 | μA | $V_{SS} \le V_{PIN} \le V_{DD}$,<br>Pin at high-impedance |
| DI51 | | I/O Pins Not 5V Tolerant(3) | -1 | — | +1 | μA | $V_{SS} \le V_{PIN} \le V_{DD}$,<br>Pin at high-impedance,<br>-40°C ≤ TA ≤ +85°C |
| DI51a | | I/O Pins Not 5V Tolerant(3) | -1 | — | +1 | μA | Analog pins shared with external reference pins,<br>-40°C ≤ TA ≤ +85°C |
| DI51b | | I/O Pins Not 5V Tolerant(3) | -1 | — | +1 | μA | $V_{SS} \le V_{PIN} \le V_{DD}$,<br>Pin at high-impedance,<br>-40°C ≤ TA ≤ +125°C |
| DI51c | | I/O Pins Not 5V Tolerant(3) | -1 | — | +1 | μA | Analog pins shared with external reference pins,<br>-40°C ≤ TA ≤ +125°C |
| DI55 | | $\overline{\text{MCLR}}$ | -5 | — | +5 | μA | $V_{SS} \le V_{PIN} \le V_{DD}$ |
| DI56 | | OSC1 | -5 | — | +5 | μA | $V_{SS} \le V_{PIN} \le V_{DD}$,<br>XT and HS modes |

**Note 1:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

**2:** Negative current is defined as current sourced by the pin.

**3:** See the **"Pin Diagrams"** section for the 5V tolerant I/O pins.

**4:** $V_{IL}$ source < ($V_{SS}$ – 0.3). Characterized but not tested.

**5:** Non-5V tolerant pins $V_{IH}$ source > ($V_{DD}$ + 0.3), 5V tolerant pins $V_{IH}$ source > 5.5V. Characterized but not tested.

**6:** Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

**7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

**8:** Any number and/or combination of I/O pins not excluded under $I_{ICL}$ or $I_{ICH}$ conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

### TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS

| **AC CHARACTERISTICS** | | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| OS50 | FPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range | 0.8 | — | 8.0 | MHz | ECPLL, XTPLL modes |
| OS51 | FVCO | On-Chip VCO System Frequency | 120 | — | 340 | MHz | |
| OS52 | TLOCK | PLL Start-up Time (Lock Time) | 0.9 | 1.5 | 3.1 | ms | |
| OS53 | DCLK | CLKO Stability (Jitter)(2) | -3 | 0.5 | 3 | % | |

**Note 1:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases, or communication clocks used by the application, use the following formula:

$$\text{Effective Jitter} = \frac{D_{CLK}}{\sqrt{\dfrac{F_{OSC}}{\text{Time Base or Communication Clock}}}}$$

For example, if FOSC = 120 MHz and the SPIx bit rate = 10 MHz, the effective jitter is as follows:

$$\text{Effective Jitter} = \frac{D_{CLK}}{\sqrt{\dfrac{120}{10}}} = \frac{D_{CLK}}{\sqrt{12}} = \frac{D_{CLK}}{3.464}$$

### TABLE 30-19: INTERNAL FRC ACCURACY

| **AC CHARACTERISTICS** | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| **Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1)** | | | | | | | |
| F20a | FRC | -1.5 | 0.5 | +1.5 | % | -40°C ≤ TA ≤ -10°C | VDD = 3.0-3.6V |
| | | -1 | 0.5 | +1 | % | -10°C ≤ TA ≤ +85°C | VDD = 3.0-3.6V |
| F20b | FRC | -2 | 1 | +2 | % | +85°C ≤ TA ≤ +125°C | VDD = 3.0-3.6V |

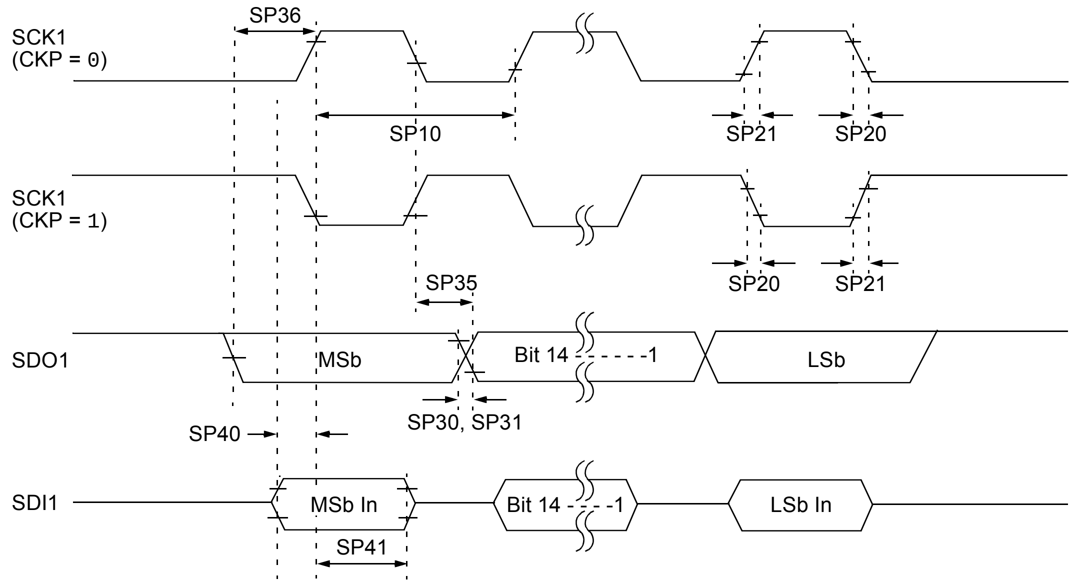
**Note 1:** Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

### TABLE 30-20: INTERNAL LPRC ACCURACY

| **AC CHARACTERISTICS** | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| **LPRC @ 32.768 kHz(1)** | | | | | | | |
| F21a | LPRC | -30 | — | +30 | % | -40°C ≤ TA ≤ -10°C | VDD = 3.0-3.6V |
| | | -20 | — | +20 | % | -10°C ≤ TA ≤ +85°C | VDD = 3.0-3.6V |
| F21b | LPRC | -30 | — | +30 | % | +85°C ≤ TA ≤ +125°C | VDD = 3.0-3.6V |

**Note 1:** The change of LPRC frequency as VDD changes.

### FIGURE 30-24: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS



**Note:** Refer to Figure 30-1 for load conditions.

### TABLE 30-43: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

| **AC CHARACTERISTICS** | | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic[1]** | **Min.** | **Typ.[2]** | **Max.** | **Units** | **Conditions** |
| SP10 | FscP | Maximum SCK1 Frequency | — | — | 10 | MHz | **(Note 3)** |
| SP20 | TscF | SCK1 Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP21 | TscR | SCK1 Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP35 | TscH2doV,<br>TscL2doV | SDO1 Data Output Valid after SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2sc,<br>TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH,<br>TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL,<br>TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

**TABLE 31-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)**

| **DC CHARACTERISTICS** | | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical** | **Max** | **Units** | **Conditions** | | |
| **Power-Down Current (IPD)** | | | | | | |
| HDC60e | 1400 | 2500 | μA | +150°C | 3.3V | Base Power-Down Current **(Notes 1, 3)** |
| HDC61c | 15 | — | μA | +150°C | 3.3V | Watchdog Timer Current: ΔIWDT **(Notes 2, 4)** |

**Note 1:** Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to VSS. WDT, etc., are all switched off and VREGS (RCON<8>) = 1.

**2:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

**3:** These currents are measured on the device containing the most memory in this family.

**4:** These parameters are characterized, but are not tested in manufacturing.

**TABLE 31-5: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)**

| **DC CHARACTERISTICS** | | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical** | **Max** | **Units** | **Conditions** | | |
| HDC44e | 12 | 30 | mA | +150°C | 3.3V | 40 MIPS |

**TABLE 31-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| **DC CHARACTERISTICS** | | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical** | **Max** | **Units** | **Conditions** | | |
| HDC20 | 9 | 15 | mA | +150°C | 3.3V | 10 MIPS |
| HDC22 | 16 | 25 | mA | +150°C | 3.3V | 20 MIPS |
| HDC23 | 30 | 50 | mA | +150°C | 3.3V | 40 MIPS |

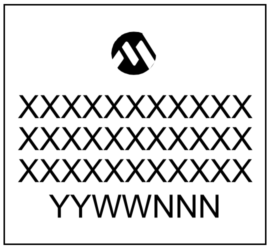
**TABLE 31-7: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)**

| **DC CHARACTERISTICS** | | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical** | **Max** | **Doze Ratio** | **Units** | **Conditions** | | |
| HDC72a | 24 | 35 | 1:2 | mA | +150°C | 3.3V | 40 MIPS |
| HDC72f(1) | 14 | — | 1:64 | mA | | | |
| HDC72g(1) | 12 | — | 1:128 | mA | | | |

**Note 1:** Parameters with Doze ratios of 1:64 and 1:128 are characterized, but are not tested in manufacturing.

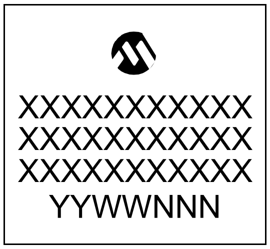
## 33.1 Package Marking Information (Continued)

48-Lead UQFN (6x6x0.5 mm)



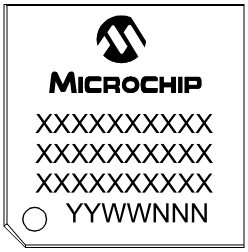
Example

64-Lead QFN (9x9x0.9 mm)

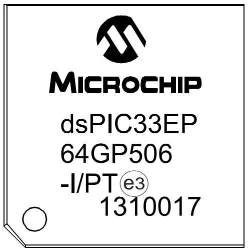


Example

64-Lead TQFP (10x10x1 mm)

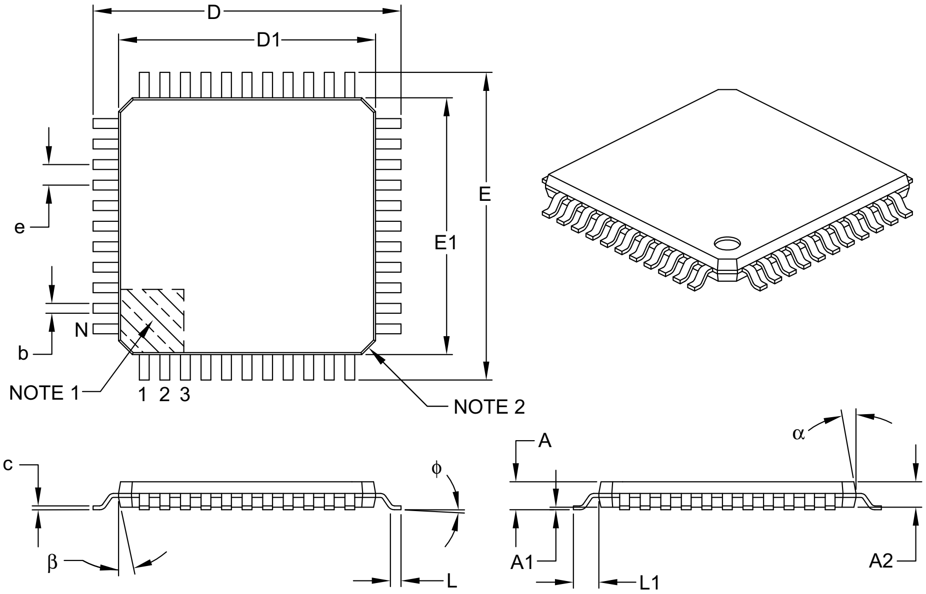


Example



## 44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | 44 | | |
| Lead Pitch | e | 0.80 BSC | | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | 1.00 REF | | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | 12.00 BSC | | |
| Overall Length | D | 12.00 BSC | | |
| Molded Package Width | E1 | 10.00 BSC | | |
| Molded Package Length | D1 | 10.00 BSC | | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.30 | 0.37 | 0.45 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

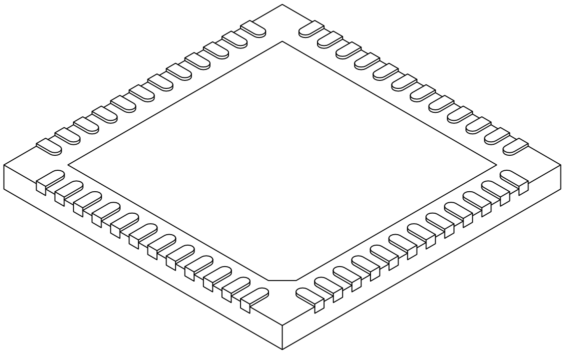
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

## 48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 48 | |
| Pitch | e | | 0.40 BSC | |
| Overall Height | A | 0.45 | 0.50 | 0.55 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.127 REF | |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 4.45 | 4.60 | 4.75 |
| Overall Length | D | | 6.00 BSC | |
| Exposed Pad Length | D2 | 4.45 | 4.60 | 4.75 |
| Contact Width | b | 0.15 | 0.20 | 0.25 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-153A Sheet 2 of 2

### TABLE A-5: MAJOR SECTION UPDATES (CONTINUED)

| Section Name | Update Description |
|---|---|
| **Section 30.0 "Electrical Characteristics"** | • Throughout: qualifies all footnotes relating to the operation of analog modules below VDDMIN (replaces "will have" with "may have")<br>• Throughout: changes all references of SPI timing parameter symbol "TscP" to "FscP"<br>• Table 30-1: changes VDD range to 3.0V to 3.6V<br>• Table 30-4: removes Parameter DC12 (RAM Retention Voltage)<br>• Table 30-7: updates Maximum values at 10 and 20 MIPS<br>• Table 30-8: adds Maximum IPD values, and removes all ∆IWDT entries<br>• Adds new Table 30-9 (Watchdog Timer Delta Current) with consolidated values removed from Table 30-8. All subsequent tables are renumbered accordingly.<br>• Table 30-10: adds footnote for all parameters for 1:2 Doze ratio<br>• Table 30-11:<br>- changes Minimum and Maximum values for D120 and D130<br>- adds Minimum and Maximum values for D131<br>- adds Minimum and Maximum values for D150 through D156, and removes Typical values<br>• Table 30-12:<br>- reformats table for readability<br>- changes IOL conditions for DO10<br>• Table 30-14: adds footnote to D135<br>• Table 30-17: changes Minimum and Maximum values for OS30<br>• Table 30-19:<br>- splits temperature range and adds new values for F20a<br>- reduces temperature range for F20b to extended temperatures only<br>• Table 30-20:<br>- splits temperature range and adds new values for F21a<br>- reduces temperature range for F20b to extended temperatures only<br>• Table 30-53:<br>- adds Maximum value to CM30<br>- adds footnote ("Parameter characterized...") to multiple parameters<br>• Table 30-55: adds Minimum and Maximum values for all CTMUI specifications, and removes Typical values<br>• Table 30-57: adds new footnote to AD09<br>• Table 30-58:<br>- removes all specifications for accuracy with external voltage references<br>- removes Typical values for AD23a and AD24a<br>- replaces Minimum and Maximum values for AD21a, AD22a, AD23a and AD24a with new values, split by Industrial and Extended temperatures<br>- removes Maximum value of AD30<br>- removes Minimum values from AD31a and AD32a<br>- adds or changes Typical values for AD30, AD31a, AD32a and AD33a<br>• Table 30-59:<br>- removes all specifications for accuracy with external voltage references<br>- removes Maximum value of AD30<br>- removes Typical values for AD23b and AD24b<br>- replaces Minimum and Maximum values for AD21b, AD22b, AD23b and AD24b with new values, split by Industrial and Extended temperatures<br>- removes Minimum and Maximum values from AD31b, AD32b, AD33b and AD34b<br>- adds or changes Typical values for AD30, AD31a, AD32a and AD33a<br>• Table 30-61: Adds footnote to AD51 |
| **Section 32.0 "DC and AC Device Characteristics Graphs"** | • Updates Figure 32-6 (Typical IDD @ 3.3V) with individual current vs. processor speed curves for the different program memory sizes |
| **Section 33.0 "Packaging Information"** | • Replaces drawing C04-149C (64-pin QFN, 7.15 x 7.15 exposed pad) with C04-154A (64-pin QFN, 5.4 x 5.4 exposed pad) |