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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc206t-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



File Name Addr. Bit 15 Bit 14 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 00 All Reset OC1CON1 0900 — — OCSIDL CCTSEL<2.0> — ENFLT8 ENFLT8 — OCFIT8 OCFIT8<		+- I U.	001	FUIC			CUGII	OUTFU			KE013		F						
OC1CON1 0900 — — ENFLTB ENFLTB ENFLTB OCFLTB OCFLTB OCFLTA TRIGMODE OCM<2:0> 0000 OC1CON2 9902 FLTMD FLTOUT FLTRIEN OCINV — — — OC32 OCTRIG TRIGSTAT OCFLTB OCFLTA TRIGMODE OCM<2:0> 0000 OC100N2 9902 FLTMD FLTRIEN OCINV — — — OC32 OCTRIG TRIGSTAT OCTRIS SYNCSEL-4:0> 0000 OC100N2 9906 — — OUDUT Compare 1 Register	File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON2 0902 FLTMD FLTNIEN OCINV — — OC22 OCTRIG TRIGSTAT OCTRIS SYNCSEL4:0> 0000 OC1RN 0906	OC1CON1	0900	_	—	OCSIDL	C	CTSEL<2:	0>	—	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>	•	0000
0C1RS 0904	OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS		SYN	NCSEL<4:0)>		000C
OC1R 096	OC1RS	0904							Outp	out Compare	e 1 Seconda	ary Register							xxxx
0C1TMR 0908	OC1R	0906								Output Co	mpare 1 Re	egister							xxxx
OC2CON1 090A — OCSIDL C_TSEL<2:> — ENFLTB ENFLTB M OCFLTB OCFLTA TRIGMODE OCM 000000000000000000000000000000000000	OC1TMR	0908								Timer V	alue 1 Regi	ster							xxxx
OC2CON2 0900 FLTMU FLTMU FLTNIEN OCINV - - OC32 OCTRIG TRIGSTAT OCTRIS SYNCSEL4:0> OOD OC2R 0906 - - OC4 Corras SYNCSEL4:0> OOD OOD OC2R OOD Corras SYNCSEL4:0> OOD OO	OC2CON1	090A		—	OCSIDL	0	CTSEL<2:	0>	—	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000
OC2RS 0906 Image: Second Windows Condows	OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS		SYN	NCSEL<4:0)>		000C
OC2R 0910 UNIC UNIC UNIC UNIC UNIC UNIC UNIC UNIC	OC2RS	090E							Outp	out Compare	e 2 Seconda	ary Register							xxxx
OC2TMR 0912 Image: Second	OC2R	0910								Output Co	mpare 2 Re	egister							xxxx
OC3CON1 0914 — — OCSIDL OCTSEL<2:> — ENFLTB ENFLTA — OCFLTB OCFLTA TRIGMODE OCM<2:>> 000000000000000000000000000000000000	OC2TMR	0912								Timer V	alue 2 Regi	ster							xxxx
OC3CON20916FLTMDFLTOUTFLTRIENOCINV———OC32OCTRIGTRIGSTATOCTRISSYNCSEL4:0>0000OC3RS09180918	OC3CON1	0914		—	OCSIDL	0	CTSEL<2:	0>	—	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000
OC3Rs 0918 Output Compare 3 Secondary Register xxxx OC3R 091A	OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS		SYN	NCSEL<4:0)>		000C
OC3R 091A	OC3RS	0918							Outp	out Compare	e 3 Seconda	ary Register							xxxx
OC3TMR 091C	OC3R	091A								Output Co	mpare 3 Re	egister							xxxx
OC4CON1 091E — OCSIDL OCTSEL<2:··· — ENFLTB ENFLTB OCFLTB OCFLTB OCFLTA TRIGMODE OCM<2:0> 000000000000000000000000000000000000	OC3TMR	091C								Timer V	alue 3 Regi	ster							xxxx
OC4CON2 0920 FLTMD FLTRIEN OCINV — — OC32 OCTRIG TRIGSTAT OCTRIS SYNCSEL<4:0> 000000000000000000000000000000000000	OC4CON1	091E	—	—	OCSIDL	0	CTSEL<2:	0>	_	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000
OC4Rs0922Output Compare 4 Secondary RegisterxxxxOC4R0924Output Compare 4 RegisterxxxxOC4TMR0926Timer Value 4 Registerxxxx	OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	_	_	_	OC32	OCTRIG	TRIGSTAT	OCTRIS		SYN	NCSEL<4:0)>		000C
OC4R 0924 Output Compare 4 Register xxxx OC4TMR 0926 Timer Value 4 Register xxxx	OC4RS	0922							Outp	out Compare	e 4 Seconda	ary Register							xxxx
OC4TMR 0926 Timer Value 4 Register xxxx	OC4R	0924								Output Co	mpare 4 Re	egister							xxxx
	OC4TMR	0926								Timer V	alue 4 Regi	ster							xxxx

TABLE 4-10: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 4 REGISTER MAP

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.6.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than, or greater than, the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note: The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed but the contents of the register remain unchanged.

4.7 Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.7.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled when all these conditions are met:

- BWMx bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is $M = 2^{N}$ bytes, the last 'N' bits of the data buffer start address must be zeros.

XBREV<14:0> is the Bit-Reversed Addressing modifier, or 'pivot point', which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note:	All bit-reversed EA calculations assume
	word-sized data (LSb of every EA is always
	clear). The XBREVx value is scaled
	accordingly to generate compatible (byte)
	addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XBREVx) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note: Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

REGISTER 5-2: NV	MADRH: NONVOLATILE MEMORY ADDRESS REGISTER HIGH
------------------	---

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	_
bit 15			•	•	•		bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMAD	R<23:16>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at F	-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown				nown		

bit 15-8 Unimplemented: Read as '0'

bit 7-0 **NVMADR<23:16>:** Nonvolatile Memory Write Address High bits Selects the upper 8 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

REGISTER 5-3: NVMADRL: NONVOLATILE MEMORY ADDRESS REGISTER LOW

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMA	DR<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown						nown	

bit 15-0 NVMADR<15:0>: Nonvolatile Memory Write Address Low bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
			NVMK	EY<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set	٤	'0' = Bit is cle	eared	x = Bit is unk	nown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 **NVMKEY<7:0>:** Key Register (write-only) bits

15.0 OUTPUT COMPARE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual" for OCxR and OCxRS register restrictions.





REGISTER 17-1: QEI1CON: QEI1 CONTROL REGISTER (CONTINUED)

bit 6-4	INTDIV<2:0>: Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select) ⁽³⁾						
	<pre>111 = 1:128 prescale value 110 = 1:64 prescale value 101 = 1:32 prescale value 100 = 1:16 prescale value 011 = 1:8 prescale value 010 = 1:4 prescale value 001 = 1:2 prescale value 000 = 1:1 prescale value</pre>						
bit 3	CNTPOL: Position and Index Counter/Timer Direction Select bit						
	 0 = Counter direction is positive unless modified by external up/down signal 						
bit 2	GATEN: External Count Gate Enable bit						
	 1 = External gate signal controls position counter operation 0 = External gate signal does not affect position counter/timer operation 						
bit 1-0	CCM<1:0>: Counter Control Mode Selection bits						
	 11 = Internal Timer mode with optional external count is selected 10 = External clock count with optional external count is selected 01 = External clock count with external up/down direction is selected 00 = Quadrature Encoder Interface (x4 mode) Count mode is selected 						
Note 1:	When CCM<1:0> = 10 or 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.						

- 2: When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.
- 3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 17-17: INT1TMRH: INTERVAL 1 TIMER HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
	INTTMR<31:24>										
bit 15	bit 15 bit 8										
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
	INTTMR<23:16>										
bit 7							bit 0				
Legend:											
R = Readable b	bit	W = Writable bi	it	U = Unimplem	nented bit, read	d as '0'					
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown							nown				

bit 15-0 INTTMR<31:16>: High Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

REGISTER 17-18: INT1TMRL: INTERVAL 1 TIMER LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
	INTTMR<15:8>										
bit 15	bit 8 bit 8										
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
	INTTMR<7:0>										
bit 7							bit 0				
Legend:											
R = Readable I	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'										
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown						nown					

bit 15-0 INTTMR<15:0>: Low Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

18.0 SERIAL PERIPHERAL INTERFACE (SPI)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Serial Peripheral Interface (SPI)" (DS70569) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with Motorola[®] SPI and SIOP interfaces.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X device family offers two SPI modules on a single device. These modules, which are designated as SPI1 and SPI2, are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of the SPI2 module, but results in a lower maximum speed for SPI2. See **Section 30.0** "**Electrical Characteristics**" for more information.

The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- SSx/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, SSx is not used. In 2-pin mode, neither SDOx nor SSx is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

20.1 UART Helpful Tips

- 1. In multi-node, direct-connect UART networks, receive inputs UART react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
 - a) If URXINV = 0, use a pull-up resistor on the RX pin.
 - b) If URXINV = 1, use a pull-down resistor on the RX pin.
- 2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UARTx module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

20.2.1 KEY RESOURCES

- "UART" (DS70582) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	F7BP	<3:0>		F6BP<3:0>					
bit 15							bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	F5BP	<3:0>			F4BI	><3:0>			
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimpleme	nted bit, rea	d as '0'			
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown						
bit 15-12	F7BP<3:0>: 1111 = Filter	RX Buffer Masl	k for Filter 7 b	its ffer					

1110 = Filter hits received in RX Buffer 14
•
•
0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0
F6BP<3:0>: RX Buffer Mask for Filter 6 bits (same values as bits<15:12>)
F5BP<3:0>: RX Buffer Mask for Filter 5 bits (same values as bits<15:12>)
F4BP<3:0>: RX Buffer Mask for Filter 4 bits (same values as bits<15:12>)

REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	F11BF	P<3:0>			F10B	P<3:0>	
bit 15							bit 8
R/W_0	R/M-0	R/M/-0	R/M-0	R/\\/_0	R/W/-0	R/M/-0	R/\/_0
10,00-0	F9BP	>	1000-0	10,00-0	F8B	P<3:0>	1477-0
bit 7	bit 7						bit 0
Legend:							
R = Readable	R = Readable bit W = Writable bit				nented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 15-12	F11BP<3:0> 1111 = Filter 1110 = Filter • • • 0001 = Filter 0000 = Filter	RX Buffer Mar hits received ir hits received ir hits received ir hits received ir	sk for Filter 1 n RX FIFO bu n RX Buffer 1 n RX Buffer 1 n RX Buffer 0	1 bits iffer 4			
bit 11-8 bit 7-4	F10BP<3:0> F9BP<3:0>:	RX Buffer Ma	sk for Filter 1 k for Filter 9 t	0 bits (same val bits (same value	lues as bits<15 s as bits<15:1	5:12>) 2>)	
bit 3-0	F8BP<3:0>:	RX Buffer Mas	k for Filter 8 k	oits (same value	s as bits<15:1	2>)	

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23.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

- **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. То complement the information in this data sheet. refer to "Analog-to-Digital Converter (ADC)" (DS70621) in the "dsPIC33/PIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have one ADC module. The ADC module supports up to 16 analog input channels.

On ADC1, the AD12B bit (AD1CON1<10>) allows the ADC module to be configured by the user as either a 10-bit, 4 Sample-and-Hold (S&H) ADC (default configuration) or a 12-bit, 1 S&H ADC.

Note: The ADC module needs to be disabled before modifying the AD12B bit.

23.1 Key Features

23.1.1 10-BIT ADC CONFIGURATION

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) conversion
- · Conversion speeds of up to 1.1 Msps
- · Up to 16 analog input pins
- Connections to three internal op amps
- Connections to the Charge Time Measurement Unit (CTMU) and temperature measurement diode
- Channel selection and triggering can be controlled by the Peripheral Trigger Generator (PTG)
- External voltage reference input pins
- · Simultaneous sampling of:
 - Up to four analog input pins
 - Three op amp outputs
 - Combinations of analog inputs and op amp outputs
- Automatic Channel Scan mode
- Selectable conversion Trigger source
- · Selectable Buffer Fill modes
- Four result alignment options (signed/unsigned, fractional/integer)
- Operation during CPU Sleep and Idle modes

23.1.2 12-BIT ADC CONFIGURATION

The 12-bit ADC configuration supports all the features listed above, with the exception of the following:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only one S&H amplifier in the 12-bit configuration; therefore, simultaneous sampling of multiple channels is not supported.

Depending on the particular device pinout, the ADC can have up to 16 analog input pins, designated AN0 through AN15. These analog inputs are shared with op amp inputs and outputs, comparator inputs, and external voltage references. When op amp/comparator functionality is enabled, or an external voltage reference is used, the analog input that shares that pin is no longer available. The actual number of analog input pins, op amps and external voltage reference input configuration depends on the specific device.

A block diagram of the ADC module is shown in Figure 23-1. Figure 23-2 provides a diagram of the ADC conversion clock period.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ADRC	—	—	SAMC4 ⁽¹⁾	SAMC3 ⁽¹⁾	SAMC2 ⁽¹⁾	SAMC1 ⁽¹⁾	SAMC0 ⁽¹⁾	
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ADCS7(2	²⁾ ADCS6 ⁽²⁾	ADCS5 ⁽²⁾	ADCS4 ⁽²⁾	ADCS3 ⁽²⁾	ADCS2 ⁽²⁾	ADCS1 ⁽²⁾	ADCS0 ⁽²⁾	
bit 7							bit 0	
Legend:								
R = Reada		vv = vvritable t	DIT		nented bit, read			
-n = value	at POR	"1" = Bit is set		$0^{\circ} = Bit is cle$	ared	x = Bit is unkr	nown	
bit 15	ADRC: ADC1 1 = ADC inter 0 = Clock deri	Conversion Cl nal RC clock ved from syste	ock Source bit m clock	:				
bit 14-13	Unimplement	ted: Read as '0	3					
bit 12-8	SAMC<4:0>:	Auto-Sample T	ime bits ⁽¹⁾					
	11111 = 31 TAD • • • • • • • •							
h:+ 7 0	00000 = 0 IA			at h:ta(2)				
bit 7-0 ADCS<7:0>: ADC1 Conversion Clock Select bits ⁽²⁾ 11111111 = TP • (ADCS<7:0> + 1) = TP • 256 = TAD •								
Note 1: 2:	This bit is only use This bit is not used	d if SSRC<2:0> if ADRC (AD10	· (AD1CON1< CON3<15>) =	7:5>) = 111 ar 1.	nd SSRCG (AD	1CON1<4>) =	0.	

REGISTER 23-3: AD1CON3: ADC1 CONTROL REGISTER 3

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
CSS31	CSS30	_	_	_	CSS26 ⁽²⁾	CSS25 ⁽²⁾	CSS24 ⁽²⁾
bit 15				-			bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_			_				
bit 7							bit 0
Legend:							
R = Readabl	e bit	W = Writable b	bit	U = Unimple	mented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	CSS31: ADC	1 Input Scan Se	election bit				
	1 = Selects C	TMU capacitive	and time me	asurement for	input scan (Ope	en)	
	0 = Skips CTI	MU capacitive a	nd time meas	surement for in	put scan (Open)	
bit 14	CSS30: ADC	1 Input Scan Se	election bit				
	1 = Selects C 0 = Skips CTI	TMU on-chip te MU on-chip tem	mperature mea	easurement fo surement for i	r input scan (CT nput scan (CTM	MU TEMP) IU TEMP)	
bit 13-11	Unimplemen	ted: Read as '0	,				
bit 10	CSS26: ADC	1 Input Scan Se	election bit ⁽²⁾				
	1 = Selects O	A3/AN6 for inpu	ut scan				
	0 = Skips OA	3/AN6 for input	scan				
bit 9	CSS25: ADC	1 Input Scan Se	election bit ⁽²⁾				
	1 = Selects O	A2/AN0 for inpu	ut scan				
	0 = Skips OA	2/AN0 for input	scan				
bit 8	CSS24: ADC	1 Input Scan Se	election bit ⁽²⁾				
	1 = Selects O 0 = Skips OA	A1/AN3 for input 1/AN3 for input	ut scan scan				
bit 7-0	Unimplemen	ted: Read as 'o	,				
Note 1: A	II AD1CSSH bits prresponding inpu	can be selected ut on the device	l by user softw , convert VRE	vare. However _{FL.}	r, inputs selecte	d for scan, with	out a

REGISTER 23-7: AD1CSSH: ADC1 INPUT SCAN SELECT REGISTER HIGH⁽¹⁾

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

24.2 PTG Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

24.2.1 KEY RESOURCES

- "Peripheral Trigger Generator" (DS70669) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0	
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	
PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, reac	l as '0'		
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown	
bit 15-13 bit 12-8	bit 15-13 PTGCLK<2:0>: Select PTG Module Clock Source bits 111 = Reserved 110 = Reserved 101 = PTG module clock source will be T3CLK 100 = PTG module clock source will be T2CLK 011 = PTG module clock source will be T1CLK 010 = PTG module clock source will be TAD 001 = PTG module clock source will be Fosc 000 = PTG module clock source will be FP							
	11111 = Divide-by-32 11110 = Divide-by-31 • • • • • • • • • • • • •							
bit 7-4	PTGPWD<3:0	0>: PTG Trigge	er Output Pulse	e-Width bits				
	<pre>1111 = All trigger outputs are 16 PTG clock cycles wide 1110 = All trigger outputs are 15 PTG clock cycles wide</pre>							
bit 3	Unimplemen	ted: Read as '	0'					
bit 2-0	PTGWDT<2:0	0>: Select PTG	Watchdog Tir	mer Time-out	Count Value bits	3		
	PTGWDT<2:0>: Select PTG Watchdog Timer Time-out Count Value bits 111 = Watchdog Timer will time-out after 512 PTG clocks 110 = Watchdog Timer will time-out after 256 PTG clocks 101 = Watchdog Timer will time-out after 128 PTG clocks 100 = Watchdog Timer will time-out after 64 PTG clocks 011 = Watchdog Timer will time-out after 32 PTG clocks 010 = Watchdog Timer will time-out after 16 PTG clocks 001 = Watchdog Timer will time-out after 8 PTG clocks 001 = Watchdog Timer will time-out after 8 PTG clocks 000 = Watchdog Timer is disabled							

REGISTER 24-2: PTGCON: PTG CONTROL REGISTER

29.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

29.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent[®] and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika[®]

DC CH	ARACTE	RISTICS	$\label{eq:conditions: 3.0V to 3.6V} \begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$						
Param No.	Symbol	Characteristic	Min. Typ. Max. Units Conditions						
DI60a	licl	Input Low Injection Current	0	_	₋₅ (4,7)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP and RB7		
DI60b	Іісн	Input High Injection Current	0	_	+5 ^(5,6,7)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB7 and all 5V tolerant pins ⁽⁶⁾		
DI60c	∑lict	Total Input Injection Current (sum of all I/O and control pins)	-20 ⁽⁸⁾	_	+20(8)	mA	Absolute instantaneous sum of all \pm input injection cur- rents from all I/O pins (IICL + IICH) $\leq \sum$ IICT		

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.

4: VIL source < (Vss – 0.3). Characterized but not tested.

5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.



FIGURE 30-13: QEI MODULE INDEX PULSE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

TABLE 30-32: QEI INDEX PULSE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			Standard Op (unless othe Operating te	perating erwise st mperatur	Conditio ated) e -40°(-40°(ns: 3.0V to 3.6V C \leq TA \leq +85°C for Industrial C \leq TA \leq +125°C for Extended
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Max.	Units	Conditions
TQ50	TqiL	Filter Time to Recognize Low, with Digital Filter	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)
TQ51	TqiH	Filter Time to Recognize High, with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)
TQ55	Tqidxr	Index Pulse Recognized to Position Counter Reset (ungated index)	3 TCY	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Alignment of index pulses to QEA and QEB is shown for position counter Reset timing only. Shown for forward direction only (QEA leads QEB). Same timing applies for reverse direction (QEA lags QEB) but index pulse recognition occurs on the falling edge.

AC CHARACTERISTICS			Standar (unless Operatir	d Opera otherwi ng tempe	ting Cor se stated rature	ditions: 1) ⁽¹⁾ -40°C ≤ [°] -40°C ≤ [°]	: 3.0V to 3.6V TA \leq +85°C for Industrial TA \leq +125°C for Extended
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
		ADC /	Accuracy	/ (12-Bit	Mode)		
AD20a	Nr	Resolution	12	2 Data Bi	its	bits	
AD21a	INL	Integral Nonlinearity	-2.5		2.5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-5.5	_	5.5	LSb	+85°C < TA \leq +125°C (Note 2)
AD22a	DNL	Differential Nonlinearity	-1		1	LSb	-40°C \leq TA \leq +85°C (Note 2)
			-1		1	LSb	+85°C < TA \leq +125°C (Note 2)
AD23a	Gerr	Gain Error ⁽³⁾	-10		10	LSb	-40°C \leq TA \leq +85°C (Note 2)
			-10		10	LSb	+85°C < TA \leq +125°C (Note 2)
AD24a	EOFF	Offset Error	-5		5	LSb	$-40^{\circ}C \le TA \le +85^{\circ}C$ (Note 2)
			-5		5	LSb	+85°C < TA \leq +125°C (Note 2)
AD25a	—	Monotonicity	_			—	Guaranteed
		Dynamic	Performa	ance (12	-Bit Mod	e)	
AD30a	THD	Total Harmonic Distortion ⁽³⁾	_	75		dB	
AD31a	SINAD	Signal to Noise and Distortion ⁽³⁾	_	68	-	dB	
AD32a	SFDR	Spurious Free Dynamic Range ⁽³⁾		80	_	dB	
AD33a	Fnyq	Input Signal Bandwidth ⁽³⁾	_	250		kHz	
AD34a	ENOB	Effective Number of Bits ⁽³⁾	11.09	11.3	_	bits	

TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.



44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note:

Microchip Technology Drawing C04-103C Sheet 1 of 2