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Details

•XFI

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	•
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc502-e-mm

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

FIGURE 2-7: INTERLEAVED PFC









REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits ^(2,3) 111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8)
bit 4	RA: REPEAT Loop Active bit 1 = REPEAT loop in progress 0 = REPEAT loop not in progress
bit 3	N: MCU ALU Negative bit 1 = Result was negative 0 = Result was non-negative (zero or positive)
bit 2	 OV: MCU ALU Overflow bit This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred
bit 1	 Z: MCU ALU Zero bit 1 = An operation that affects the Z bit has set it at some time in the past 0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)
bit 0	C: MCU ALU Carry/Borrow bit 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred
Note 1: 2:	This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only. The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority

- Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- 4: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre-modified and post-modified Effective Addresses (EA). The upper half of the base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Read Page register (DSRPAG) or the 9-bit Write Page register (DSWPAG), to form an Extended Data Space (EDS) address or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

Construction of the EDS address is shown in Example 4-1. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when base address bit, EA<15> = 1, DSWPAG<8:0> are concatenated onto EA<14:0> to form the 24-bit EDS write address.





4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
 - In Word mode, this instruction maps the lower word of the Program Space location (P<15:0>) to a data address (D<15:0>)

- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.
- TBLRDH (Table Read High):
 - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. The 'phantom' byte (D<15:8>) is always '0'.
 - In Byte mode, this instruction maps the upper or lower byte of the program word to D<7:0> of the data address in the TBLRDL instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.



FIGURE 4-23: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS

5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory and to program two instruction words at a time. See the General Purpose and Motor Control Family tables (Table 1 and Table 2, respectively) for the page sizes of each device.

For more information on erasing and programming Flash memory, refer to "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual".

5.3 **Programming Operations**

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time) in Table 30-14 in **Section 30.0 "Electrical Characteristics"**.

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS.

Refer to **Flash Programming**" (DS70609) in the "*dsPIC33/PIC24 Family Reference Manual*" for details and codes examples on programming using RTSP.

5.4 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

5.4.1 KEY RESOURCES

- "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

5.5 Control Registers

Four SFRs are used to erase and write the program Flash memory: NVMCON, NVMKEY, NVMADRH and NVMADRL.

The NVMCON register (Register 5-1) enables and initiates Flash memory erase and write operations.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRH and NVMADRL. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations or the selected page for erase operations.

The NVMADRH register is used to hold the upper 8 bits of the EA, while the NVMADRL register is used to hold the lower 16 bits of the EA.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

		11.0	11.0		11.0		
		0-0	0-0	VREGSE	0-0		VREGS
hit 15		—		VREGGE	—	Civi	bit 8
bit 10							bit 0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
bit 7						.1	bit 0
Legend:							
R = Reada	able bit	W = Writable I	oit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	TRAPR: Trap	Reset Flag bit					
	$1 = A \operatorname{Trap} Co$	onflict Reset ha	s occurred	d			
hit 11			s not occurre		ot Elog bit		
DIL 14	1 = An illega	l oncode deter	viinniiaiizeu	v Access Res	et Flay Dit ode or Uninitial	lized W registe	er used as an
	Address	Pointer caused	a Reset			ized w regiote	
	0 = An illegal	l opcode or Uni	nitialized W r	egister Reset h	as not occurred	t	
bit 13-12	Unimplemen	ted: Read as 'o)'				
bit 11	VREGSF: Fla	ish Voltage Reg	ulator Stand	by During Slee	p bit		
	1 = Flash vol	tage regulator i	s active durin	ng Sleep			
bit 10		tage regulator (naby mode dui	ing Sleep		
bit Q	CM: Configur	ation Mismatch	, Elac bit				
bit 5	1 = A Configur	ration Mismatch	h Reset has	occurred			
	0 = A Configu	ration Mismatc	h Reset has	not occurred			
bit 8	VREGS: Volta	age Regulator S	Standby Durii	ng Sleep bit			
	1 = Voltage r	egulator is activ	e during Sle	ер			
	0 = Voltage r	egulator goes in	nto Standby i	mode during SI	еер		
bit 7	EXTR: Extern	nal Reset (MCL	R) Pin bit				
	\perp = A Master 0 = A Master	Clear (pin) Res Clear (pin) Res	et has occur et has not or	rea ccurred			
bit 6	SWR: Softwa	re RESET (Instr	uction) Flag	bit			
	1 = A reset	instruction has	been execut	ed			
	0 = A RESET	instruction has	not been exe	ecuted			
bit 5	SWDTEN: So	oftware Enable/	Disable of W	DT bit ⁽²⁾			
	1 = WDT is er	nabled					
bit 4		ISADIEU hdog Timor Tim	o out Elog b	:+			
DIL 4	1 = WDT time		e-oul Flay D	IL			
	0 = WDT time	e-out has not oc	curred				
Note 1.	All of the Peset sta	itus hits can bo	set or cleare	d in software S	Setting one of th	ese hits in soft	vara does not
	cause a device Re	set.					
2:	If the FWDTEN Co SWDTEN bit settin	onfiguration bit i	s '1' (unprog	rammed), the V	VDT is always e	enabled, regard	less of the

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
_				IC4R<6:0>						
bit 15							bit 8			
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
_				IC3R<6:0>						
bit 7							bit 0			
Legend:										
R = Readat	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'				
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown			
bit 15	Unimpleme	ented: Read as '	0'							
bit 14-8	IC4R<6:0>: (see Table 2	IC4R<6:0>: Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)								
	1111001 =	1111001 = Input tied to RPI121								
	•									
	•									
	0000001 =	Input tied to CM	P1							
bit 7		nput tied to vss	, 0,							
bit 6-0		Assign Input Ca	o unture 3 (IC3)) to the Correspo	ondina RPn P	in hits				
bit 0 0	(see Table 1	(see Table 11-2 for input pin selection numbers)								
	1111001 =	Input tied to RPI	121	,						
	•									
	0000001 =	Input tied to CM	P1							
	0000000 =	Input tied to Vss	5							

REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				U1RXR<6:0	>		
bit 7							bit 0

REGISTER 11-10: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 Unimplemented: Read as '0' bit 6-0 U1RXR<6:0>: Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121

REGISTER 11-11: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_		_	—	_	—	_
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				U2RXR<6:0>	>		
bit 7							bit 0
Legend:							

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-7 Unimplemented: Read as '0'

^{0000000 =} Input tied to Vss

13.0 TIMER2/3 AND TIMER4/5

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter
- They also support these features:
- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (32-bit timer pairs, and Timer3 and Timer5 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw); Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

Note: For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note: Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

HS/HC-	0 HS/HC-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTSTAT	-(1) CLSTAT ⁽¹⁾	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB ⁽²⁾	MDCS ⁽²⁾
bit 15							bit 8
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
DTC1	DTC0	DTCP ⁽³⁾	<u> </u>	MTBS	CAM ^(2,4)	XPRES ⁽⁵⁾	IUE ⁽²⁾
bit 7							bit 0
Legend:		HC = Hardware	Clearable bit	HS = Hardwa	are Settable bit		
R = Reada	able bit	W = Writable bi	t	U = Unimplei	mented bit, rea	d as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unk	nown
bit 15	FLTSTAT: Fai 1 = Fault inter 0 = No Fault i This bit is clea	ult Interrupt Statu rrupt is pending interrupt is pendi	us bit ⁽¹⁾ ng LTIEN = 0				
hit 14	CI STAT. Cur	rent-l imit Interru	nt Status hit(1)				
	1 = Current-lin 0 = No curren This bit is clea	mit interrupt is pentitienter interrupt is pentitienter interrupt is ared by setting C	ending s pending CLIEN = 0.				
bit 13	TRGSTAT: Tr	igger Interrupt S	tatus bit				
	1 = Trigger in 0 = No trigger This bit is clea	terrupt is pending r interrupt is pend ared by setting T	g ding RGIEN = 0.				
bit 12	FLTIEN: Faul	t Interrupt Enabl	e bit				
	1 = Fault inter 0 = Fault inter	rrupt is enabled rrupt is disabled	and the FLTST	AT bit is cleare	ed		
bit 11	CLIEN: Curre	ent-Limit Interrup	t Enable bit				
	1 = Current-lii 0 = Current-lii	mit interrupt is er mit interrupt is di	nabled sabled and the	CLSTAT bit is	cleared		
bit 10	TRGIEN: Trig	ger Interrupt Ena	able bit				
	1 = A trigger e 0 = Trigger ev	event generates /ent interrupts ar	an interrupt rec	quest the TRGSTAT	bit is cleared		
bit 9	ITB: Independ	dent Time Base	Mode bit ⁽²⁾				
	1 = PHASEx (0 = PTPER re	register provides egister provides f	time base peri timing for this F	iod for this PW WM generato	/M generator r		
bit 8	MDCS: Maste	er Duty Cycle Re	gister Select bi	it(2)			
	1 = MDC regi 0 = PDCx reg	ster provides du ister provides du	ty cycle informa ity cycle inform	ation for this P ation for this F	WM generator WM generator		
Note 1:	Software must clea	ar the interrupt st	atus here and	in the correspo	onding IFSx bit	in the interrup	ot controller.
2:	These bits should	not be changed	after the PWM	, is enabled (P	PTEN = 1).	•	
3:	DTC<1:0> = 11 for	r DTCP to be eff	ective; otherwis	se, DTCP is ig	nored.		
4:	The Independent T CAM bit is ignored	Time Base (ITB =	1) mode must	be enabled to	use Center-Ali	igned mode. If	TTB = 0, the
-	T		· · · · · · · · · · · · · · · · · · ·				

REGISTER 16-7: PWMCONx: PWMx CONTROL REGISTER

5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-2: CxC1	RL2: ECANx CON	TROL REGISTER 2
---------------------	----------------	-----------------

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
	_	_	_	_	_	_	_	
bit 15							bit 8	
							,	
U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0	
—	—	—	DNCNT4	DNCNT3	DNCNT2	DNCNT1	DNCNT0	
bit 7							bit 0	
Legend:								
R = Readable I	bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		
bit 15-5	Unimplemen	ted: Read as '	0'					
bit 4-0	DNCNT<4:0>	: DeviceNet™	Filter Bit Num	ber bits				
	10010-1111	1 = Invalid sele	ection					
	10001 = Com	pares up to Da	ata Byte 3, bit	6 with EID<17	>			
	•							
	•							
	•							
00001 = Compares up to Data Byte 1, bit 7 with EID<0> 00000 = Does not compare data bytes								

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8
bit 15							bit 8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
bit 7							bit 0
Legend:							

REGISTER 21-11: CxFEN1: ECANx ACCEPTANCE FILTER ENABLE REGISTER 1

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0

FLTEN<15:0>: Enable Filter n to Accept Messages bits

1 = Enables Filter n

0 = Disables Filter n

REGISTER 21-12: CxBUFPNT1: ECANx FILTER 0-3 BUFFER POINTER REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
F3BP<3:0>				F2BP<3:0>				
		·			bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
F1BP<3:0>			F0BP<3:0>					
bit 7					bit 0			
W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'				
'1' = Bit is se	t	'0' = Bit is cleared		x = Bit is unknown				
RX Buffer Mas	k for Filter 3 b	vits						
1111 = Filter hits received in RX FIFO buffer								
er hits received i	n RX Buffer 14	4						
•								
0000 = Filter hits received in RX Buller 1								
• DV Duffor Moo	k for Eiltor 2 b	ita (aama valua	a aa hita<15:1	221				
F2BF<3:U>: RX BUTTER MASK FOR FILTER 2 DITS (same values as DITS<15:12>)								
F1BP<3:0>: RX Buffer Mask for Filter 1 bits (same values as bits<15:12>)								
RX Buffer Mas	k for Filter 0 b	its (same value	s as bits<15:1	2>)				
	RX Buffer Mas RX Buffer Mas RX Buffer Mas	RX Buffer Mask for Filter 1 b RX Buffer Mask for Filter 0 b	RX Buffer Mask for Filter 1 bits (same value RX Buffer Mask for Filter 1 bits (same value RX Buffer Mask for Filter 0 bits (same value	RX Buffer Mask for Filter 1 bits (same values as bits<15:1 RX Buffer Mask for Filter 1 bits (same values as bits<15:1 RX Buffer Mask for Filter 0 bits (same values as bits<15:1	RX Buffer Mask for Filter 1 bits (same values as bits<15:12>) RX Buffer Mask for Filter 1 bits (same values as bits<15:12>) RX Buffer Mask for Filter 0 bits (same values as bits<15:12>)			

24.2 PTG Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

24.2.1 KEY RESOURCES

- "Peripheral Trigger Generator" (DS70669) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

NOTES:

27.6 JTAG Interface

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface is provided in future revisions of the document.

Note:	Refer to "Programming and Diagnostics"
	(DS70608) in the "dsPIC33/PIC24 Family
	Reference Manual" for further information
	on usage, configuration and operation of the
	JTAG interface.

27.7 In-Circuit Serial Programming

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits" (DS70663) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

27.8 In-Circuit Debugger

When MPLAB[®] ICD 3 or REAL ICE[™] is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to \overline{MCLR} , VDD, Vss and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins (PGECx and PGEDx).

27.9 Code Protection and CodeGuard™ Security

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X, and PIC24EPXXXGP/MC20X devices offer basic implementation of CodeGuard Security that supports only General Segment (GS) security. This feature helps protect individual Intellectual Property.

Note: Refer to "CodeGuard[™] Security" (DS70634) in the "dsPIC33/PIC24 Family Reference Manual" for further information on usage, configuration and operation of CodeGuard Security.

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C < TA \le +125^{\circ}C$ for Extended				
Parameter No.	Тур.	Max.	Units	Cond	itions		
Power-Down	Current (IPD) ⁽¹⁾ -	dsPIC33EP32GI	P50X, dsPIC33EF	P32MC20X/50X and PIC2	24EP32GP/MC20X		
DC60d	30	100	μA	-40°C			
DC60a	35	100	μA	+25°C	2 2)/		
DC60b	150	200	μA	+85°C	3.3V		
DC60c	250	500	μA	+125°C	1		
Power-Down	Current (IPD) ⁽¹⁾ -	dsPIC33EP64GI	P50X, dsPIC33EI	P64MC20X/50X and PIC2	24EP64GP/MC20X		
DC60d	25	100	μA	-40°C			
DC60a	30	100	μA	+25°C	2.21/		
DC60b	150	350	μA	+85°C	3.3V		
DC60c	350	800	μA	+125°C			
Power-Down	Current (IPD) ⁽¹⁾ –	dsPIC33EP128G	P50X, dsPIC33E	P128MC20X/50X and PI	C24EP128GP/MC20X		
DC60d	30	100	μA	-40°C			
DC60a	35	100	μA	+25°C	3 3//		
DC60b	150	350	μA	+85°C	5.50		
DC60c	550	1000	μA	+125°C			
Power-Down	Current (IPD) ⁽¹⁾ –	dsPIC33EP256G	P50X, dsPIC33E	P256MC20X/50X and PIC	C24EP256GP/MC20X		
DC60d	35	100	μA	-40°C			
DC60a	40	100	μA	+25°C	3 3//		
DC60b	250	450	μA	+85°C	5.5 V		
DC60c	1000	1200	μA	+125°C	1		
Power-Down Current (IPD) ⁽¹⁾ – dsPIC33EP512GP50X, dsPIC33EP512MC20X/50X and PIC24EP512GP/MC20X							
DC60d	40	100	μA	-40°C	3.3V		
DC60a	45	100	μA	+25°C			
DC60b	350	800	μA	+85°C			
DC60c	1100	1500	μA	+125°C			

TABLE 30-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

Note 1: IPD (Sleep) current is measured as follows:

• CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all set)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



TABLE 30-36:SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial					
	i	<i>"</i>		(0)	-40°	$^{\circ}C \leq TA \leq$	+125°C for Extended	
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	-40°C to +125°C (Note 3)	
SP20	TscF	SCK2 Output Fall Time	_	_		ns	See Parameter DO32 (Note 4)	
SP21	TscR	SCK2 Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO2 Data Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO2 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_		ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30			ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30			ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPI2 pins.



FIGURE 30-26: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

NOTES: