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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc502-e-sp

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

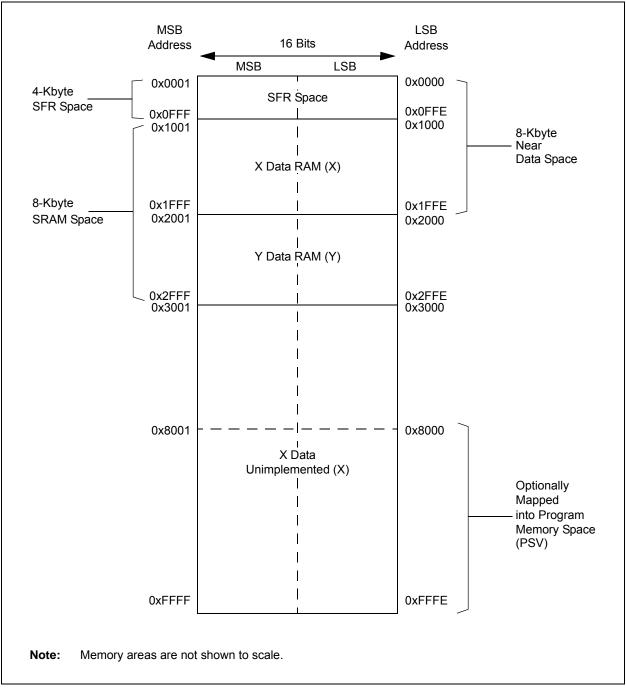


FIGURE 4-8: DATA MEMORY MAP FOR dsPIC33EP64MC20X/50X AND dsPIC33EP64GP50X DEVICES

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 4	MATHERR: Math Error Status bit
	1 = Math error trap has occurred
	0 = Math error trap has not occurred
bit 3	ADDRERR: Address Error Trap Status bit
	1 = Address error trap has occurred0 = Address error trap has not occurred
bit 2	STKERR: Stack Error Trap Status bit
	1 = Stack error trap has occurred
	0 = Stack error trap has not occurred
bit 1	OSCFAIL: Oscillator Failure Trap Status bit
	1 = Oscillator failure trap has occurred
	0 = Oscillator failure trap has not occurred
bit 0	Unimplemented: Read as '0'

Note 1: These bits are available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

REGISTER	<u>R 10-2: PMD</u> 2	2: PERIPHER	AL MODULE	DISABLE C	ONTROL RE	GISTER 2				
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0			
_		—		IC4MD	IC3MD	IC2MD	IC1MD			
bit 15							bit			
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0			
				OC4MD	OC3MD	OC2MD	OC1MD			
bit 7							bit			
Legend:	1.1.1									
R = Readab		W = Writable b	Dit	•	nented bit, rea					
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown			
bit 15-12	Unimplemen	ted: Read as '0	,							
bit 11	-	t Capture 4 Mod								
	•	ture 4 module is								
	0 = Input Cap	oture 4 module is	s enabled							
bit 10	IC3MD: Input Capture 3 Module Disable bit									
	1 = Input Capture 3 module is disabled									
		oture 3 module is								
bit 9		Capture 2 Mod								
		oture 2 module is oture 2 module is								
bit 8	IC1MD: Input	C1MD: Input Capture 1 Module Disable bit								
	1 = Input Cap	oture 1 module is oture 1 module is	s disabled							
bit 7-4		ted: Read as '0								
bit 3	OC4MD: Out	put Compare 4	Module Disable	e bit						
	1 = Output Compare 4 module is disabled									
	-	ompare 4 modu								
bit 2	OC3MD: Output Compare 3 Module Disable bit									
	•	 1 = Output Compare 3 module is disabled 0 = Output Compare 3 module is enabled 								
L:1 4	-	-		. h.:4						
bit 1		put Compare 2								
	\perp – Output Co	ompare 2 modu								
	0 = Output Co	ompare 2 modul	le is enabled							
bit 0		ompare 2 modul put Compare 1		e bit						
bit 0	OC1MD: Out	ompare 2 modul put Compare 1 l ompare 1 modul	Module Disable	e bit						

~

14.0 INPUT CAPTURE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Input Capture" (DS70352) in the "dsPIC33/dsPIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices support four input capture channels.

Key features of the input capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 19 user-selectable Trigger/Sync sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- Configurable interrupt generation
- Up to six clock sources available for each module, driving a separate internal 16-bit counter





14.1 Input Capture Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

14.1.1 KEY RESOURCES

- "Input Capture" (DS70352) in the "dsPIC33/ PIC24 Family Reference Manual"
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

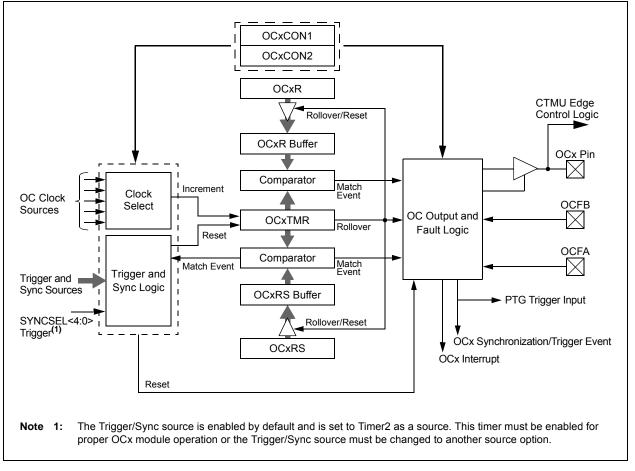
15.0 OUTPUT COMPARE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual" for OCxR and OCxRS register restrictions.





15.2 Output Compare Control Registers

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	0-0	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0		ENFLTB
 bit 15		COOIDE		OUTOLLI	OUTOLLU		bit 8
Sit 10							bit 0
R/W-0	U-0	R/W-0, HSC	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0
ENFLT		OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0
bit 7							bit 0
Legend:		HSC = Hardw	are Settable/Cl	earable bit			
R = Read	able bit	W = Writable I	oit	U = Unimplem	nented bit, read	as '0'	
-n = Value	e at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own
bit 15-14	Unimplemen	ted: Read as 'o)'				
bit 13	OCSIDL: Out	tput Compare x	Stop in Idle Mo	de Control bit			
		ompare x Halts					
	•	compare x conti	•		ode		
bit 12-10)>: Output Com	pare x Clock S	elect bits			
	111 = Periph 110 = Reserv	eral clock (FP)					
	101 = PTGO						
		is the clock so			hronous clock	is supported)	
		is the clock so					
		(is the clock so (is the clock so					
		is the clock so					
bit 9	Unimplemen	ted: Read as '0)'				
bit 8	ENFLTB: Fau	ult B Input Enab	le bit				
		compare Fault B compare Fault B					
bit 7	-	ult A Input Enab					
	1 = Output C	ompare Fault A compare Fault A	input (OCFA)				
bit 6	•	ted: Read as '0	• • •				
bit 5	OCFLTB: PW	M Fault B Con	dition Status bit				
		ult B condition of Fault B condition					
bit 4		/M Fault A Cond	•				
		ult A condition o					
Note 1:	OCxR and OCxF	29 are double h	uffered in D\\//	/ mode only			
Note 1. 2:	Each Output Cor			-	irce. See Secti	on 24.0 "Perin	heral Trigger
2.	Generator (PTG					5.1 2 7.0 1 611p	
	PTGO4 = OC1	-					
	PTGO5 = OC2						
	PTGO6 = OC3 PTGO7 = OC4						

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
CHPCLKEN	—	—	—	—	—	CHOPC	LK<9:8>
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			CHOPC	LK<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimplei	mented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown
bit 15 bit 14-10 bit 9-0	1 = Chop clos 0 = Chop clos Unimplemen CHOPCLK<9 The frequence	Enable Chop ck generator is ck generator is ted: Read as ' 9:0>: Chop Clo y of the chop c ncy = (FP/PCL)	enabled disabled 0' ck Divider bits lock signal is g	given by the fo	ollowing expressi + 1)	on:	

REGISTER 16-5: CHOP: PWMx CHOP CLOCK GENERATOR REGISTER

REGISTER 16-6: MDC: PWMx MASTER DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MDC	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MD	C<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	e bit U = Unimplemented bit, read as '0'				
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown

bit 15-0 MDC<15:0>: PWMx Master Duty Cycle Value bits

REGISTER 17-13: QEI1LECH: QEI1 LESS THAN OR EQUAL COMPARE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
			QEILE	C<31:24>							
bit 15 bit 8											
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
			QEILE	C<23:16>							
bit 7							bit 0				
Legend:											
R = Readable	bit	W = Writable b	bit	U = Unimplem	ented bit, rea	d as '0'					
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown							

bit 15-0 QEILEC<31:16>: High Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

REGISTER 17-14: QEI1LECL: QEI1 LESS THAN OR EQUAL COMPARE LOW WORD REGISTER

R = Readable t		W = Writable '1' = Bit is set		U = Unimplemented bit, read as '0' '0' = Bit is cleared x = Bit is unknowr			
Legend:							
bit 7							bit
			QEIL	EC<7:0>			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
bit 15							bit
			QEILE	EC<15:8>			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

bit 15-0 QEILEC<15:0>: Low Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

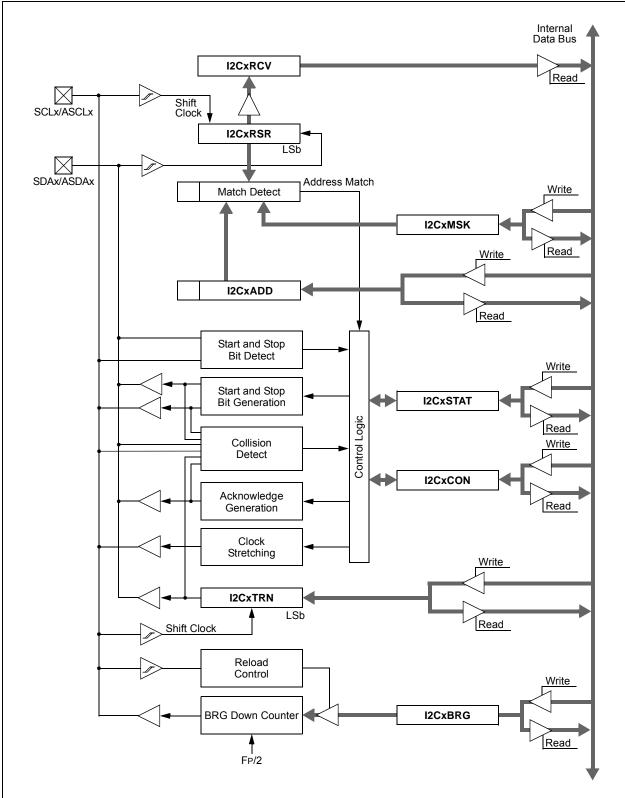


FIGURE 19-1: I2Cx BLOCK DIAGRAM (X = 1 OR 2)

Legend:C = Writable bit, but only '0' can be written to clear the bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'							
bit 7							bit 0
IVRIF	WAKIF	ERRIF	_	FIFOIF	RBOVIF	RBIF	TBIF
R/C-0	R/C-0	R/C-0	U-0	R/C-0	R/C-0	R/C-0	R/C-0
							2 0
bit 15							bit 8
_	—	ТХВО	TXBP	RXBP	TXWAR	RXWAR	EWARN
U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0

'0' = Bit is cleared

x = Bit is unknown

REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER

'1' = Bit is set

bit 15-14	Unimplemented: Read as '0'
bit 13	TXBO: Transmitter in Error State Bus Off bit
	1 = Transmitter is in Bus Off state
	0 = Transmitter is not in Bus Off state
bit 12	TXBP: Transmitter in Error State Bus Passive bit
	1 = Transmitter is in Bus Passive state0 = Transmitter is not in Bus Passive state
bit 11	RXBP: Receiver in Error State Bus Passive bit
	1 = Receiver is in Bus Passive state 0 = Receiver is not in Bus Passive state
bit 10	TXWAR: Transmitter in Error State Warning bit
	1 = Transmitter is in Error Warning state 0 = Transmitter is not in Error Warning state
bit 9	RXWAR: Receiver in Error State Warning bit
	1 = Receiver is in Error Warning state 0 = Receiver is not in Error Warning state
bit 8	EWARN: Transmitter or Receiver in Error State Warning bit
	 1 = Transmitter or receiver is in Error Warning state 0 = Transmitter or receiver is not in Error Warning state
bit 7	IVRIF: Invalid Message Interrupt Flag bit
	 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 6	WAKIF: Bus Wake-up Activity Interrupt Flag bit
	1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 5	ERRIF: Error Interrupt Flag bit (multiple sources in CxINTF<13:8>)
	 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 4	Unimplemented: Read as '0'
bit 3	FIFOIF: FIFO Almost Full Interrupt Flag bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 2	RBOVIF: RX Buffer Overflow Interrupt Flag bit
	1 = Interrupt request has occurred

-n = Value at POR

22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Charge Time Measurement Unit (CTMU)" (DS70661) in the "dsPIC33/PIC24 Family Reference Manual", which is available on the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Charge Time Measurement Unit is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Four Edge Input Trigger Sources
- Polarity Control for Each Edge Source
- Control of Edge Sequence
- Control of Response to Edges
- · Precise Time Measurement Resolution of 1 ns
- Accurate Current Source Suitable for Capacitive Measurement
- On-Chip Temperature Measurement using a Built-in Diode

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

24.0 PERIPHERAL TRIGGER GENERATOR (PTG) MODULE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Peripheral Trigger Generator (PTG)" (DS70669) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

24.1 Module Introduction

The Peripheral Trigger Generator (PTG) provides a means to schedule complex high-speed peripheral operations that would be difficult to achieve using software. The PTG module uses 8-bit commands, called "Steps", that the user writes to the PTG Queue registers (PTGQUE0-PTGQUE7), which perform operations, such as wait for input signal, generate output trigger and wait for timer.

The PTG module has the following major features:

- Multiple clock sources
- Two 16-bit general purpose timers
- Two 16-bit general limit counters
- Configurable for rising or falling edge triggering
- Generates processor interrupts to include:
 - Four configurable processor interrupts
 - Interrupt on a Step event in Single-Step modeInterrupt on a PTG Watchdog Timer time-out
- Able to receive trigger signals from these peripherals:
 - ADC
 - PWM
 - Output Compare
 - Input Capture
 - Op Amp/Comparator
 - INT2
- Able to trigger or synchronize to these peripherals:
 - Watchdog Timer
 - Output Compare
 - Input Capture
 - ADC
 - PWM
- Op Amp/Comparator

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
ADCTS4	ADCTS3	ADCTS2	ADCTS1	IC4TSS	IC3TSS	IC2TSS	IC1TSS				
bit 15							bit 8				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
OC4CS		OC2CS	OC1CS	OC4TSS	OC3TSS	OC2TSS	OC1TSS				
bit 7		00100					bit (
Legend:											
R = Reada	ble bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'					
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle		x = Bit is unkr	nown				
bit 15	ADCTS4: Sa	mple Trigger P	TGO15 for AE	OC bit							
	1 = Generate	es Trigger wher	the broadcas	t command is	executed						
	0 = Does not	generate Trigg	er when the b	roadcast com	mand is execute	ed					
bit 14		mple Trigger P									
		es Trigger wher				al					
bit 13					mand is execute	a					
DIE 13		mple Trigger P es Trigger wher			evecuted						
					mand is execute	ed					
bit 12		mple Trigger P									
	1 = Generate	es Trigger wher	the broadcas	t command is	executed						
					mand is execute	ed					
bit 11	-	C4TSS: Trigger/Synchronization Source for IC4 bit									
					ast command is broadcast con		ited				
bit 10	IC3TSS: Trig	ger/Synchroniz	ation Source f	for IC3 bit							
					ast command is broadcast con		ited				
bit 9	IC2TSS: Trig	ger/Synchroniz	ation Source f	for IC2 bit							
					ast command is broadcast con		ited				
bit 8		ger/Synchroniz									
					ast command is broadcast con		ited				
bit 7		 Does not generate Trigger/Synchronization when the broadcast command is executed OC4CS: Clock Source for OC4 bit 									
		es clock pulse v generate clock				cuted					
bit 6		 Does not generate clock pulse when the broadcast command is executed OC3CS: Clock Source for OC3 bit 									
		es clock pulse v aenerate clock			d is executed command is exe	cuted					
bit 5		ck Source for C	-								
	1 = Generate	es clock pulse v	when the broad		d is executed command is exe	cuted					
	This register is rea PTGSTRT = 1).	-					and				
	This register is on	lv used with the	PTGCTRI. OI	PTION = 1111	Step command	L					
		.,			c.op commune	•					

REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER^(1,2)

27.6 JTAG Interface

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface is provided in future revisions of the document.

Note:	Refer to "Programming and Diagnostics"
	(DS70608) in the "dsPIC33/PIC24 Family
	Reference Manual" for further information
	on usage, configuration and operation of the
	JTAG interface.

27.7 In-Circuit Serial Programming

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits" (DS70663) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

27.8 In-Circuit Debugger

When MPLAB[®] ICD 3 or REAL ICE[™] is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to \overline{MCLR} , VDD, Vss and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins (PGECx and PGEDx).

27.9 Code Protection and CodeGuard™ Security

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X, and PIC24EPXXXGP/MC20X devices offer basic implementation of CodeGuard Security that supports only General Segment (GS) security. This feature helps protect individual Intellectual Property.

Note: Refer to "CodeGuard[™] Security" (DS70634) in the "dsPIC33/PIC24 Family Reference Manual" for further information on usage, configuration and operation of CodeGuard Security.

DC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.0(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
Operati	ng Voltag	e					
DC10	Vdd	Supply Voltage	3.0		3.6	V	
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	-	_	Vss	V	
DC17	Svdd	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.03	_	—	V/ms	0V-1V in 100 ms

TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

	d Operating g temperati	$\begin{array}{llllllllllllllllllllllllllllllllllll$	ustrial):			
Param No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Comments
	Cefc	External Filter Capacitor Value ⁽¹⁾	4.7	10		μF	Capacitor must have a low series resistance (< 1 Ohm)

Note 1: Typical VCAP voltage = 1.8 volts when VDD \geq VDDMIN.

FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



TABLE 30-36:SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)TIMING REQUIREMENTS

AC CHARACTERISTICS			(unless c	l Operatin otherwise g temperat	stated) :ure -40	°C ≤ Ta ≤	/ to 3.6V +85°C for Industrial +125°C for Extended
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK2 Frequency		—	9	MHz	-40°C to +125°C (Note 3)
SP20	TscF	SCK2 Output Fall Time	_	—	_	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK2 Output Rise Time	_	—	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	_	—	_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	_	—	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	_	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—		ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPI2 pins.

TABLE 30-48:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Op (unless othe Operating ter	erwise st	ated) e -40°	C ≤ TA ≤	V to 3.6V +85°C for Industrial +125°C for Extended
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—		11	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	_	ns	
SP50	TssL2scH, TssL2scL	SS1 ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	_	ns	
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 TCY + 40	—		ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

33.0 PACKAGING INFORMATION

33.1 Package Marking Information

28-Lead SPDIP



28-Lead SOIC (.300")



28-Lead SSOP



Example dsPIC33EP64GP 502-I/SP@3 1310017

Example



Example



28-Lead QFN-S (6x6x0.9 mm)



Example



Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	be carried	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available of or customer-specific information.

DMAxSTAH (DMA Channel x	
Start Address A, High)	144
DMAxSTAL (DMA Channel x	
Start Address A, Low)	144
DMAxSTBH (DMA Channel x	
Start Address B, High)	145
DMAxSTBL (DMA Channel x	
Start Address B, Low)	145
DSADRH (DMA Most Recent RAM	4 4 7
High Address)	147
DSADRL (DMA Most Recent RAM	1 4 7
Low Address) DTRx (PWMx Dead-Time)	
FCLCONx (PWMx Fault Current-Limit Control)	
I2CxCON (I2Cx Control)	
I2CxMSK (I2Cx Slave Mode Address Mask)	280
I2CxSTAT (I2Cx Status)	
ICxCON1 (Input Capture x Control 1)	
ICxCON2 (Input Capture x Control 2)	
INDX1CNTH (Index Counter 1 High Word)	
INDX1CNTL (Index Counter 1 Low Word)	259
INDX1HLD (Index Counter 1 Hold)	
INT1HLDH (Interval 1 Timer Hold High Word)	
INT1HLDL (Interval 1 Timer Hold Low Word)	
INT1TMRH (Interval 1 Timer High Word)	
INT1TMRL (Interval 1 Timer Low Word)	263
INTCON1 (Interrupt Control 1)	
INTCON2 (Interrupt Control 2)	136
INTCON2 (Interrupt Control 3)	
INTCON4 (Interrupt Control 4)	
INTTREG (Interrupt Control and Status)	
IOCONx (PWMx I/O Control)	240
LEBCONx (PWMx Leading-Edge	- · -
Blanking Control)	245
Blanking Control) LEBDLYx (PWMx Leading-Edge	
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay)	246
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle)	246 234
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High)	246 234 122
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low)	246 234 122 122
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Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1)	246 234 122 122 121 122 221
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2)	246 234 122 122 121 122 221 223
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control)	246 234 122 122 121 122 221 223 156
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning)	246 234 122 122 121 122 221 223 156 161
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle)	246 234 122 122 121 221 223 156 161 237
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning)	246 234 122 121 121 221 223 156 161 237 237
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift)	246 234 122 121 122 221 223 156 161 237 237 237 237
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PLLFBD (PLL Feedback Divisor)	246 234 122 121 122 221 223 156 161 237 237 237 160 166
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PLLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 2) PMD3 (Peripheral Module Disable Control 3)	246 234 122 121 122 221 223 156 161 237 237 237 160 166 168 169
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PLLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 2) PMD3 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 4)	246 234 122 121 122 221 223 156 161 237 237 237 160 166 168 169 169 169
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Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PLLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 2) PMD3 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 4) PMD6 (Peripheral Module Disable Control 6)	246 234 122 121 122 221 223 156 161 237 160 166 168 169 169 170 171
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Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PHLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 1) PMD3 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 4) PMD6 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 7) POS1CNTH (Position Counter 1 High Word)	246 234 122 121 122 221 223 156 161 237 160 166 168 169 169 170 171 258 258
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Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) OSCCUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PHLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 1) PMD2 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 3) PMD7 (Peripheral Module Disable Control 4) PMD7 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 7) POS1CNTH (Position Counter 1 High Word) POS1CNTL (Position Counter 1 Hold) PTCON (PWMx Time Base Control) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable)	246 234 122 122 121 223 156 161 237 160 161 160 160 168 169 169 170 171 258 258 258 230 232 348 343
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PTGL0 (PTG Literal 0)	
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PTGQUEx (PTG Step Queue x)	
PTGSDLIM (PTG Step Delay Limit)	
PTGT0LIM (PTG Timer0 Limit)	
PTGT1LIM (PTG Timer1 Limit)	345
PTPER (PWMx Primary Master Time	
Base Period)	233
PWMCONx (PWMx Control)	
QEI1CON (QEI1 Control)	252
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Compare High Word)	262
QEI1GECL (QEI1 Greater Than or Equal	
Compare Low Word)	262
QEI1ICH (QEI1 Initialization/Capture	
High Word)	260
QEI1ICL (QEI1 Initialization/Capture	
Low Word)	260
QEI1IOC (QEI1 I/O Control)	254
QEI1LECH (QEI1 Less Than or Equal	004
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QEI1LECL (QEI1 Less Than or Equal	061
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RCON (Reset Control) REFOCON (Reference Oscillator Control)	
RPINR0 (Peripheral Pin Select Input 0)	
RPINR1 (Peripheral Pin Select Input 0)	
RPINR1 (Peripheral Pin Select Input 1)	
RPINR12 (Peripheral Pin Select Input 12)	
RPINR14 (Peripheral Pin Select Input 12)	
RPINR15 (Peripheral Pin Select Input 15)	
RPINR18 (Peripheral Pin Select Input 18)	
RPINR19 (Peripheral Pin Select Input 19)	
RPINR22 (Peripheral Pin Select Input 22)	
RPINR23 (Peripheral Pin Select Input 23)	
RPINR26 (Peripheral Pin Select Input 26)	
RPINR3 (Peripheral Pin Select Input 3)	
RPINR37 (Peripheral Pin Select Input 37)	
RPINR38 (Peripheral Pin Select Input 38)	
RPINR39 (Peripheral Pin Select Input 39)	
RPINR7 (Peripheral Pin Select Input 7)	
RPINR8 (Peripheral Pin Select Input 8)	
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RPOR1 (Peripheral Pin Select Output 1)	
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RPOR5 (Peripheral Pin Select Output 5)	199
RPOR6 (Peripheral Pin Select Output 6)	200
RPOR7 (Peripheral Pin Select Output 7)	200
RPOR8 (Peripheral Pin Select Output 8)	
RPOR9 (Peripheral Pin Select Output 9)	201
SEVTCMP (PWMx Primary Special	
Event Compare)	
SPIxCON1 (SPIx Control 1)	
SPIxCON2 (SPIx Control 2)	
SPIxSTAT (SPIx Status and Control)	
SR (CPU STATUS) 40,	
T1CON (Timer1 Centrel)	
T1CON (Timer1 Control)	205
TRGCONx (PWMx Trigger Control)	205 239
	205 239 242