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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	·
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc502-h-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



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FIGURE 2-7: INTERLEAVED PFC





Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read, and configuring the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages, by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address prior to modification addresses an EDS or PSV page
- The EA calculation uses Pre-Modified or Post-Modified Register Indirect Addressing; however, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSxPAG register is incremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-61 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- · Register Indirect with Register Offset Addressing
- Modulo Addressing
- · Bit-Reversed Addressing

			Before		After			
0/U, R/W	Operation	DSxPAG	DS EA<15>	Page Description	DSxPAG	DS EA<15>	Page Description	
O, Read		DSRPAG = 0x1FF	1	EDS: Last page	DSRPAG = 0x1FF	0	See Note 1	
O, Read	[++\Wn]	DSRPAG = 0x2FF	1	PSV: Last lsw page	DSRPAG = 0x300	1	PSV: First MSB page	
O, Read	[Wn++]	DSRPAG = 0x3FF	1	PSV: Last MSB page	DSRPAG = 0x3FF	0	See Note 1	
O, Write		DSWPAG = 0x1FF	1	EDS: Last page	DSWPAG = 0x1FF	0	See Note 1	
U, Read		DSRPAG = 0x001	1	PSV page	DSRPAG = 0x001	0	See Note 1	
U, Read	[Wn] Or	DSRPAG = 0x200	1	PSV: First Isw page	DSRPAG = 0x200	0	See Note 1	
U, Read	[WII —]	DSRPAG = 0x300	1	PSV: First MSB page	DSRPAG = 0x2FF	1	PSV: Last Isw page	

TABLE 4-61: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS and PSV SPACE BOUNDARIES^(2,3,4)

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: The Register Indirect Addressing now addresses a location in the base Data Space (0x0000-0x8000).

2: An EDS access with DSxPAG = 0x000 will generate an address error trap.

- **3:** Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.
- 4: Pseudo-Linear Addressing is not supported for large offsets.

5.0 FLASH PROGRAM MEMORY

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP/MC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows for a dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data a single program memory word, and erase program memory in blocks or 'pages' of 1024 instructions (3072 bytes) at a time.

5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

INE OID LEN											
U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0				
	—	—	—	—	CMPMD	—	—				
bit 15							bit 8				
R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0				
CRCMD	—	—	—	—	—	I2C2MD	—				
bit 7		•				•	bit 0				
Legend:											
R = Readable	e bit	W = Writable I	bit	U = Unimplem	nented bit, read	l as '0'					
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown								
bit 15-11	Unimplement	ted: Read as 'o)'								

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

bit 10	CMPMD: Comparator Module Disable bit
	1 = Comparator module is disabled
	0 = Comparator module is enabled
bit 9-8	Unimplemented: Read as '0'
bit 7	CRCMD: CRC Module Disable bit
	1 = CRC module is disabled
	0 = CRC module is enabled
bit 6-2	Unimplemented: Read as '0'
bit 1	I2C2MD: I2C2 Module Disable bit
	1 = I2C2 module is disabled
	0 = I2C2 module is enabled
bit 0	Unimplemented: Read as '0'

REGISTER 10-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—		—	—
						bit 8
U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
	—	—	REFOMD	CTMUMD	—	—
		•	•			bit 0
	U-0 — U-0 —	U-0 U-0 — — U-0 U-0 — —	U-0 U-0 U-0 — — — — U-0 U-0 U-0 — — — —	U-0 U-0 U-0 U-0 	U-0 U-0 U-0 U-0 - - - - - U-0 U-0 U-0 U-0 - U-0 U-0 U-0 R/W-0 R/W-0 - - - REFOMD CTMUMD	U-0 U-0 U-0 U-0 U-0 - - - - - - U-0 U-0 U-0 U-0 U-0 - U-0 U-0 U-0 R/W-0 U-0 - U-0 U-0 R/W-0 R/W-0 U-0 - - - REFOMD CTMUMD -

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4	Unimplemented: Read as '0'
bit 3	REFOMD: Reference Clock Module Disable bit
	1 = Reference clock module is disabled
	0 = Reference clock module is enabled
bit 2	CTMUMD: CTMU Module Disable bit
	1 = CTMU module is disabled
	0 = CTMU module is enabled
bit 1-0	Unimplemented: Read as '0'

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11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, "RPn" or "RPIn", in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs. In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C^{TM} and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and nonremappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheralselectable pin is handled in two different ways, depending on whether an input or output is being mapped.

15.0 OUTPUT COMPARE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual" for OCxR and OCxRS register restrictions.





REGISTER 16-2: PTCON2: PWMx PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER
--

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
—	—	—	_	_	—	—	—			
bit 15							bit 8			
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0			
	_	—	—	—	PCLKDIV2 ⁽¹⁾	PCLKDIV1 ⁽¹⁾	PCLKDIV0(1)			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'						
-n = Value at POR		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown				
bit 15 2	hit 15.2 Unimplemented, Dood op (o)									

bit 15-3 Unimplemented: Read as '0'

bit 2-0 PCLKDIV<2:0>: PWMx Input Clock Prescaler (Divider) Select bits⁽¹⁾

- 111 = Reserved 110 = Divide-by-64 101 = Divide-by-32
- 100 = Divide-by-32100 = Divide-by-16
- 011 = Divide-by-8
- 010 = Divide-by-4
- 001 = Divide-by-2
- 000 = Divide-by-1, maximum PWMx timing resolution (power-on default)
- **Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
—	_		DTRx<13:8>							
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
			DTR	2x<7:0>						
bit 7							bit 0			
Legend:										
R = Readable bit W = Writable bit U = Unimplemented bit, read a				d as '0'						
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is un					x = Bit is unkr	nown				

REGISTER 16-10: DTRx: PWMx DEAD-TIME REGISTER

bit 15-14 Unimplemented: Read as '0'

bit 13-0 DTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 16-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
—	—		ALTDTRx<13:8>							
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
			ALTDT	Rx<7:0>						
bit 7							bit 0			
Legend:										
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'						
-n = Value at POR		'1' = Bit is set	'1' = Bit is set		ared	x = Bit is unknown				

bit 15-14 Unimplemented: Read as '0'

bit 13-0 ALTDTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL ⁽²⁾	CLMOD		
bit 15		•	•				bit 8		
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0		
FLTSRC4	TSRC4 FLTSRC3 FLTSRC2 FLTSRC1 FLTSRC0 FLTPOL ⁽²⁾			FLTPOL ⁽²⁾	FLTMOD1	FLTMOD0			
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, read	l as '0'			
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown		
bit 15	Unimplemen	ted: Read as '	0'						
bit 14-10	CLSRC<4:0>	Current-Limit	Control Signa	al Source Sele	ct for PWM Ger	nerator # bits			
	11111 = Fau	lt 32							
	11110 = Res	served							
	•								
	•	anyod							
	01100 = Res 01011 = Con	nparator 4							
	01010 = Op	Amp/Comparat	or 3						
	01001 = Op	Amp/Comparat	or 2						
	01000 = Op	Amp/Comparat	or 1						
	00111 = Res	erved							
	00101 = Res	erved							
	00100 = Res	erved							
	00011 = Fau	lt 4							
	00010 = Fau	lt 3							
	00000 = Fau	It 1 (default)							
bit 9	CLPOL: Curr	rent-Limit Polar	ity for PWM G	enerator # bit	2)				
	1 = The selec	cted current-lim	it source is ac	tive-low					
	0 = The selec	cted current-lim	it source is ac	tive-high					
bit 8	CLMOD: Cur	rent-Limit Mode	e Enable for P	WM Generato	er # bit				
	1 = Current-L	imit mode is er	nabled						
	0 = Current-L	imit mode is di	sabled						
Note 1: If the	he PWMLOCK	Configuration b	it (FOSCSEL·	<6>) is a '1', th	ne IOCONx regi	ster can only be	e written after		
the	the unlock sequence has been executed.								

REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾

2: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

21.4 ECAN Control Registers

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0		
		CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0		
bit 15				·			bit 8		
R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0		
OPMODE2	OPMODE1	OPMODE0		CANCAP	—		WIN		
bit 7							bit 0		
Legend: $P = Poolohilo hit \qquad W = Writeblo hit \qquad U = Unimplemented hit road as '0'$									
		'1' = Bit is set	JIL	$0^{\circ} = \text{Bit is closed}$	ared	v – Bitis unkr			
	UK	I - DILIS SEL			aleu		IOWIT		
bit 15-14	Unimplemen	ted: Read as '()'						
bit 13	CSIDL: ECAN	Nx Stop in Idle I	Mode bit						
	1 = Discontin	ues module ope	eration when	device enters I	dle mode				
	0 = Continues	s module opera	tion in Idle m	ode					
bit 12	ABAT: Abort	All Pending Tra	nsmissions b	it					
	1 = Signals al	I transmit buffe	rs to abort tra when all tran	ansmission smissions are a	aborted				
bit 11		CANx Module C	lock (ECAN) S	Source Select b	bit				
2	1 = FCAN is e	qual to 2 * FP							
	0 = FCAN is e	qual to FP							
bit 10-8	REQOP<2:0>	Request Ope	ration Mode	bits					
	111 = Set Lis	ten All Messag	es mode						
	101 = Reserv	red							
	100 = Set Co	nfiguration mod	le						
	011 = Set Lis	ten Only mode							
	001 = Set Dis	able mode							
	000 = Set No	rmal Operation	mode						
bit 7-5	OPMODE<2:	0> : Operation N	/lode bits						
	111 = Module	e is in Listen All	Messages m	node					
	110 = Reserv 101 = Reserv	red red							
	100 = Module	e is in Configura	ation mode						
	011 = Module	e is in Listen Or	ly mode						
	010 = Module	e is in Loopback s is in Disable n	k mode node						
	000 = Module	e is in Normal C	peration mod	de					
bit 4	Unimplemen	ted: Read as 'd)'						
bit 3	CANCAP: CA	AN Message Re	eceive Timer	Capture Event	Enable bit				
	1 = Enables in 0 = Disables (nput capture ba CAN capture	sed on CAN	message recei	ive				
bit 2-1	Unimplemen	ted: Read as '()'						
bit 0	WIN: SFR Ma	ap Window Sele	ect bit						
	1 = Uses filter	r window							
	0 = Uses buff	er window							

NOTES:

NOTES:

Field	Description
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions \in {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 working registers ∈ {W0W15}
Wnd	One of 16 destination working registers ∈ {W0W15}
Wns	One of 16 source working registers ∈ {W0W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}

TABLE 28-1:	SYMBOLS USED IN OPCODE DESCRIPTIONS ((CONTINUED)

DC CH	ARACTE	RISTICS	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
	VIL	Input Low Voltage					
DI10		Any I/O Pin and MCLR	Vss	—	0.2 VDD	V	
DI18		I/O Pins with SDAx, SCLx	Vss	_	0.3 VDD	V	SMBus disabled
DI19		I/O Pins with SDAx, SCLx	Vss	—	0.8	V	SMBus enabled
	Vih	Input High Voltage					
DI20		I/O Pins Not 5V Tolerant	0.8 VDD	—	Vdd	V	(Note 3)
		I/O Pins 5V Tolerant and MCLR	0.8 VDD	—	5.5	V	(Note 3)
		I/O Pins with SDAx, SCLx	0.8 VDD	—	5.5	V	SMBus disabled
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled
	ICNPU	Change Notification Pull-up Current					
DI30			150	250	550	μA	VDD = 3.3V, VPIN = VSS
	ICNPD	Change Notification Pull-Down Current ⁽⁴⁾					
DI31			20	50	100	μA	VDD = 3.3V, VPIN = VDD

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (VSS 0.3). Characterized but not tested.

5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.



FIGURE 30-12: QEA/QEB INPUT CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

TABLE 30-31: QUADRATURE DECODER TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$			
Param No.	Symbol	Characteristic ⁽¹⁾	Тур. ⁽²⁾	Max.	Units	Conditions
TQ30	TQUL	Quadrature Input Low Time	6 Tcy		ns	
TQ31	ΤουΗ	Quadrature Input High Time	6 Tcy	—	ns	
TQ35	ΤουΙΝ	Quadrature Input Period	12 Tcy	—	ns	
TQ36	ΤουΡ	Quadrature Phase Period	3 Tcy	—	ns	
TQ40	TQUFL	Filter Time to Recognize Low, with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)
TQ41	TQUFH	Filter Time to Recognize High, with Digital Filter	3 * N * Tcy		ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: N = Index Channel Digital Filter Clock Divide Select bits. Refer to "Quadrature Encoder Interface (QEI)" (DS70601) in the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip web site for the latest family reference manual sections.

TABLE 30-39:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param.	Symbol	Characteristic ⁽¹⁾	Min. Typ. ⁽²⁾ Max. Units Condition					
SP70	FscP	Maximum SCK2 Input Frequency			15	MHz	(Note 3)	
SP72	TscF	SCK2 Input Fall Time	—		_	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK2 Input Rise Time	—		_	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO2 Data Output Fall Time	—		—	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO2 Data Output Rise Time	—		_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30		_	ns		
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120		_	ns		
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)	
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

DC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)(1)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial							
			$-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended						
Param No.	Param No. Symbol Characteristic			Тур. ⁽²⁾	Max.	Units	Conditions		
Compa	rator AC Ch	naracteristics							
CM10	Tresp	Response Time ⁽³⁾	_	19	_	ns	V+ input step of 100 mV, V- input held at VDD/2		
CM11	Тмс2о∨	Comparator Mode Change to Output Valid		_	10	μs			
Compa	rator DC Ch	naracteristics							
CM30	VOFFSET	Comparator Offset Voltage	—	±10	40	mV			
CM31	VHYST	Input Hysteresis Voltage ⁽³⁾	_	30	—	mV			
CM32	Trise/ Tfall	Comparator Output Rise/ Fall Time ⁽³⁾	—	20	—	ns	1 pF load capacitance on input		
CM33	Vgain	Open-Loop Voltage Gain ⁽³⁾	—	90	—	db			
CM34	VICM	Input Common-Mode Voltage	AVss	—	AVdd	V			
Op Am	p AC Chara	cteristics							
CM20	SR	Slew Rate ⁽³⁾		9		V/µs	10 pF load		
CM21a	Рм	Phase Margin (Configuration A) ^(3,4)	_	55	—	Degree	G = 100V/V; 10 pF load		
CM21b	Рм	Phase Margin (Configuration B) ^(3,5)	—	40	_	Degree	G = 100V/V; 10 pF load		
CM22	Gм	Gain Margin ⁽³⁾	—	20	—	db	G = 100V/V; 10 pF load		
CM23a	GBW	Gain Bandwidth (Configuration A) ^(3,4)	_	10	—	MHz	10 pF load		
CM23b	Gвw	Gain Bandwidth (Configuration B) ^(3,5)	—	6	_	MHz	10 pF load		

TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
- 3: Parameter is characterized but not tested in manufacturing.
- 4: See Figure 25-6 for configuration information.
- 5: See Figure 25-7 for configuration information.
- 6: Resistances can vary by ±10% between op amps.

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	N	ILLIMETER	S	
Dimension	MIN	NOM	MAX	
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B