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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc502-i-mm">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc502-i-mm</a>

## 4.2 Data Address Space

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU has a separate 16-bit-wide data memory space. The Data Space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps, which are presented by device family and memory size, are shown in Figure 4-7 through Figure 4-16.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This arrangement gives a base Data Space address range of 64 Kbytes (32K words).

The base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space, which has a total address range of 16 Mbytes.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement up to 52 Kbytes of data memory (4 Kbytes of data memory for Special Function Registers and up to 48 Kbytes of data memory for RAM). If an EA points to a location outside of this area, an all-zero word or byte is returned.

### 4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte-addressable, 16-bit-wide blocks. Data is aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

### 4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® MCU devices and improve Data Space memory usage efficiency, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB. The MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

### 4.2.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X core and peripheral modules for controlling the operation of the device.

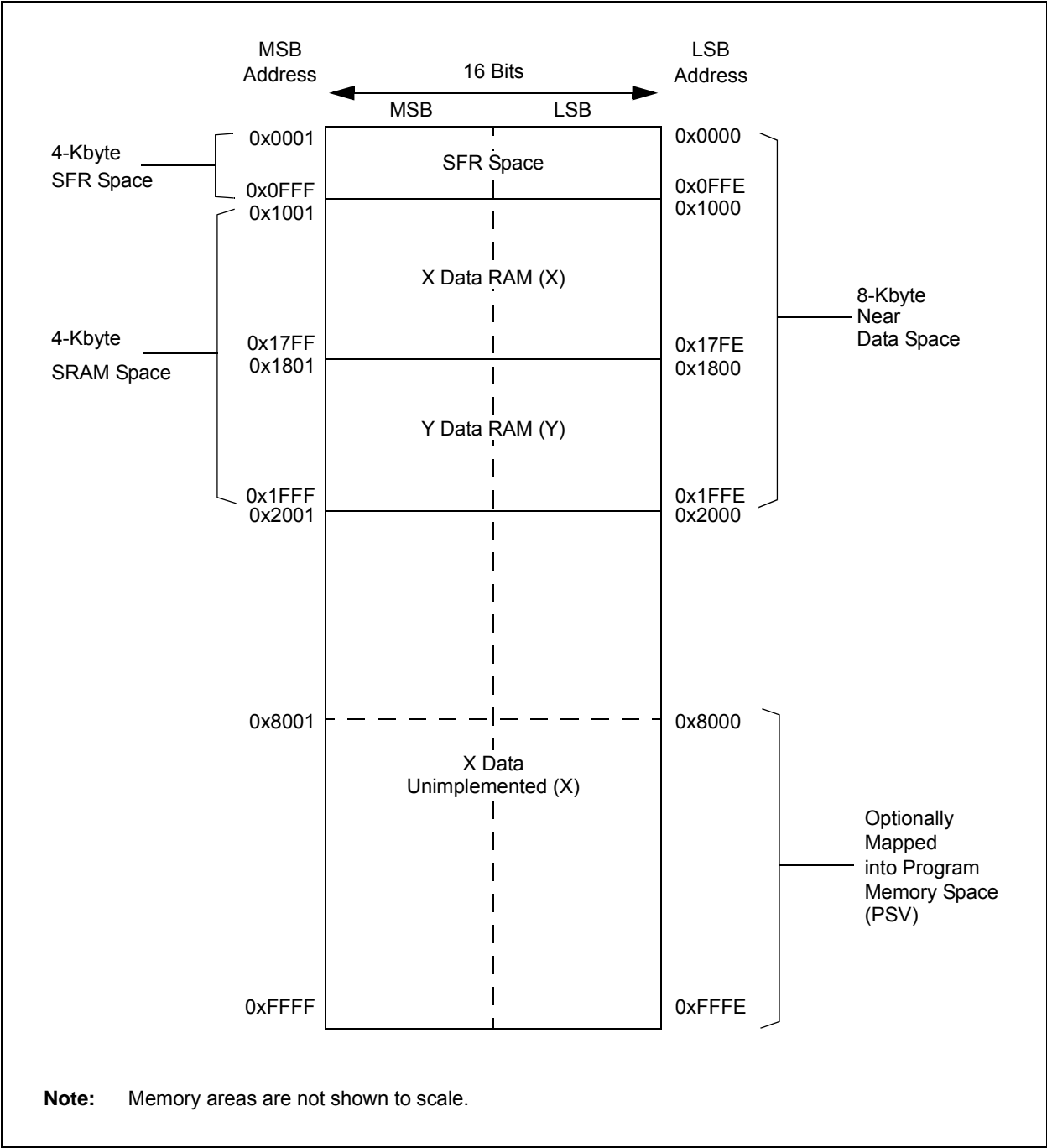
SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

**Note:** The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

### 4.2.4 NEAR DATA SPACE

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a working register as an Address Pointer.

FIGURE 4-7: DATA MEMORY MAP FOR dsPIC33EP32MC20X/50X AND dsPIC33EP32GP50X DEVICES



**FIGURE 7-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X INTERRUPT VECTOR TABLE**

<div>Decreasing Natural Order Priority</div> <div>IVT</div>	Reset – GOTO Instruction	0x000000
	Reset – GOTO Address	0x000002
	Oscillator Fail Trap Vector	0x000004
	Address Error Trap Vector	0x000006
	Generic Hard Trap Vector	0x000008
	Stack Error Trap Vector	0x00000A
	Math Error Trap Vector	0x00000C
	DMAC Error Trap Vector	0x00000E
	Generic Soft Trap Vector	0x000010
	Reserved	0x000012
	Interrupt Vector 0	0x000014
	Interrupt Vector 1	0x000016
	:	:
	:	:
	:	:
	Interrupt Vector 52	0x00007C
	Interrupt Vector 53	0x00007E
	Interrupt Vector 54	0x000080
	:	:
	:	:
	:	:
	Interrupt Vector 116	0x0000FC
	Interrupt Vector 117	0x0000FE
	Interrupt Vector 118	0x000100
	Interrupt Vector 119	0x000102
	Interrupt Vector 120	0x000104
	:	:
:	:	
:	:	
Interrupt Vector 244	0x0001FC	
Interrupt Vector 245	0x0001FE	
START OF CODE	0x000200	

See Table 7-1 for  
Interrupt Vector Details

### 7.3 Interrupt Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

#### 7.3.1 KEY RESOURCES

- “**Interrupts**” (DS70600) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

### 7.4 Interrupt Control and Status Registers

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- INTTREG

#### 7.4.1 INTCON1 THROUGH INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS), as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior and also contains the Global Interrupt Enable bit (GIE).

INTCON3 contains the status flags for the DMA and DO stack overflow status trap sources.

The INTCON4 register contains the software generated hard trap status bit (SGHT).

#### 7.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

#### 7.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

#### 7.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

#### 7.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number bits (VECNUM<7:0>) and Interrupt Priority Level bits (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP bits in the first position of IPC0 (IPC0<2:0>).

#### 7.4.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers refer to “**CPU**” (DS70359) in the “*dsPIC33/PIC24 Family Reference Manual*”.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-3 through Register 7-7 in the following pages.

**REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER**

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE2 <sup>(1)</sup>	DOZE1 <sup>(1)</sup>	DOZE0 <sup>(1)</sup>	DOZEN <sup>(2,3)</sup>	FRCDIV2	FRCDIV1	FRCDIV0
bit 15							bit 8

R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPOST1	PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15                      **ROI:** Recover on Interrupt bit  
                                  1 = Interrupts will clear the DOZEN bit  
                                  0 = Interrupts have no effect on the DOZEN bit
- bit 14-12                      **DOZE<2:0>:** Processor Clock Reduction Select bits<sup>(1)</sup>  
                                  111 = Fcy divided by 128  
                                  110 = Fcy divided by 64  
                                  101 = Fcy divided by 32  
                                  100 = Fcy divided by 16  
                                  011 = Fcy divided by 8 (default)  
                                  010 = Fcy divided by 4  
                                  001 = Fcy divided by 2  
                                  000 = Fcy divided by 1
- bit 11                      **DOZEN:** Doze Mode Enable bit<sup>(2,3)</sup>  
                                  1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks  
                                  0 = Processor clock and peripheral clock ratio is forced to 1:1
- bit 10-8                      **FRCDIV<2:0>:** Internal Fast RC Oscillator Postscaler bits  
                                  111 = FRC divided by 256  
                                  110 = FRC divided by 64  
                                  101 = FRC divided by 32  
                                  100 = FRC divided by 16  
                                  011 = FRC divided by 8  
                                  010 = FRC divided by 4  
                                  001 = FRC divided by 2  
                                  000 = FRC divided by 1 (default)
- bit 7-6                      **PLLPOST<1:0>:** PLL VCO Output Divider Select bits (also denoted as 'N2', PLL postscaler)  
                                  11 = Output divided by 8  
                                  10 = Reserved  
                                  01 = Output divided by 4 (default)  
                                  00 = Output divided by 2
- bit 5                      **Unimplemented:** Read as '0'

- Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
- 2:** This bit is cleared when the ROI bit is set and an interrupt occurs.
- 3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

**REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSSLP	ROSEL	RODIV3 <sup>(1)</sup>	RODIV2 <sup>(1)</sup>	RODIV1 <sup>(1)</sup>	RODIV0 <sup>(1)</sup>
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15            **ROON:** Reference Oscillator Output Enable bit  
                   1 = Reference oscillator output is enabled on the REFCLK pin<sup>(2)</sup>  
                   0 = Reference oscillator output is disabled
- bit 14            **Unimplemented:** Read as '0'
- bit 13            **ROSSLP:** Reference Oscillator Run in Sleep bit  
                   1 = Reference oscillator output continues to run in Sleep  
                   0 = Reference oscillator output is disabled in Sleep
- bit 12            **ROSEL:** Reference Oscillator Source Select bit  
                   1 = Oscillator crystal is used as the reference clock  
                   0 = System clock is used as the reference clock
- bit 11-8        **RODIV<3:0>:** Reference Oscillator Divider bits<sup>(1)</sup>  
                   1111 = Reference clock divided by 32,768  
                   1110 = Reference clock divided by 16,384  
                   1101 = Reference clock divided by 8,192  
                   1100 = Reference clock divided by 4,096  
                   1011 = Reference clock divided by 2,048  
                   1010 = Reference clock divided by 1,024  
                   1001 = Reference clock divided by 512  
                   1000 = Reference clock divided by 256  
                   0111 = Reference clock divided by 128  
                   0110 = Reference clock divided by 64  
                   0101 = Reference clock divided by 32  
                   0100 = Reference clock divided by 16  
                   0011 = Reference clock divided by 8  
                   0010 = Reference clock divided by 4  
                   0001 = Reference clock divided by 2  
                   0000 = Reference clock
- bit 7-0        **Unimplemented:** Read as '0'

- Note 1:** The reference oscillator output must be disabled (ROON = 0) before writing to these bits.  
**Note 2:** This pin is remappable. See **Section 11.4 “Peripheral Pin Select (PPS)”** for more information.

REGISTER 11-12: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SCK2INR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SDI2R<6:0>						
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **SCK2INR<6:0>:** Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **SDI2R<6:0>:** Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss



### 13.0 TIMER2/3 AND TIMER4/5

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Timers**” (DS70362) of the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

- 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (32-bit timer pairs, and Timer3 and Timer5 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsb); Timer3 and Timer5 are the most significant word (msb) of the 32-bit timers.

**Note:** For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

**Note:** Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

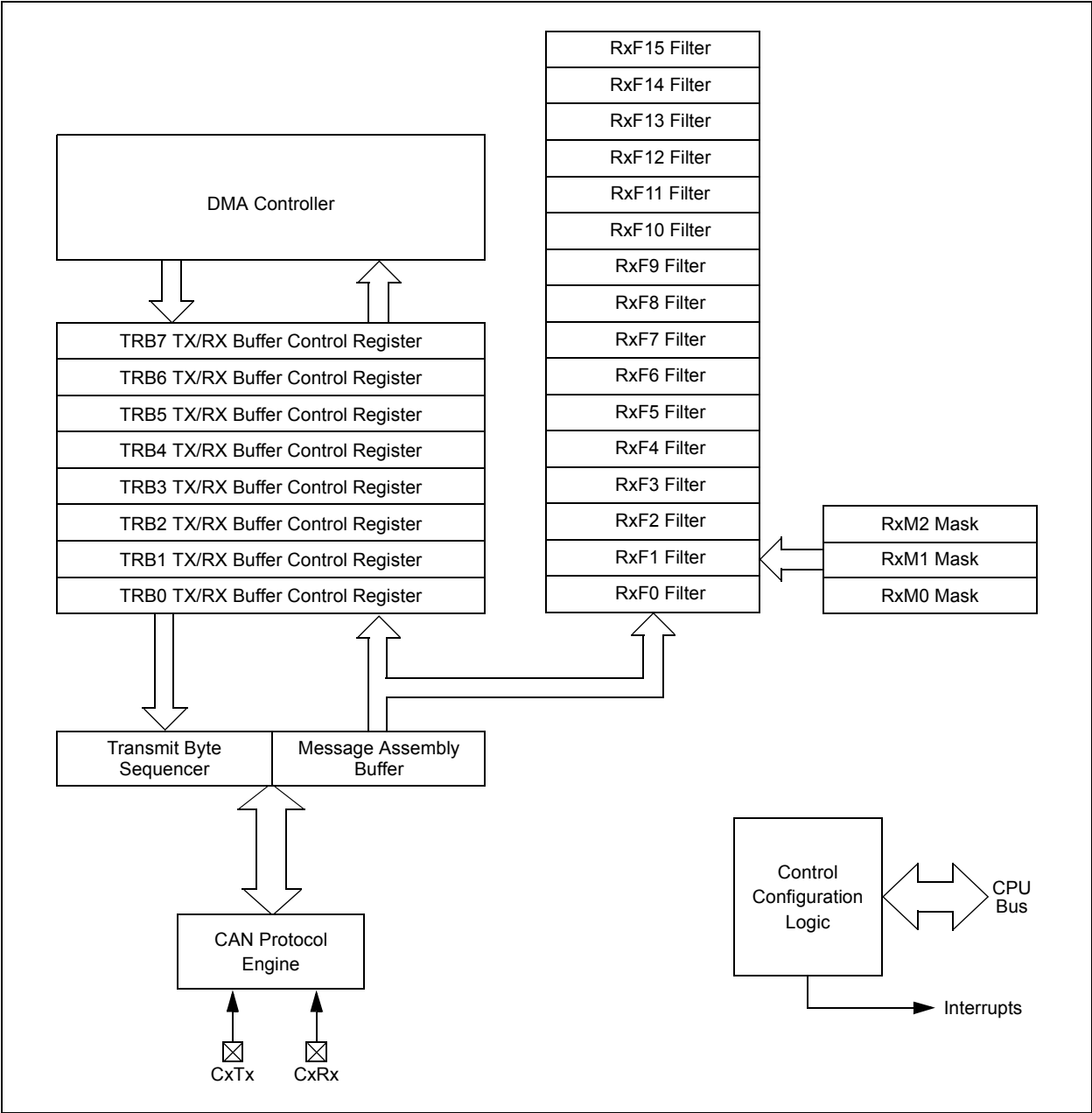
**REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)**

bit 4-0 **SYNCSEL<4:0>**: Input Source Select for Synchronization and Trigger Operation bits<sup>(4)</sup>

11111 = No Sync or Trigger source for ICx  
 11110 = Reserved  
 11101 = Reserved  
 11100 = CTMU module synchronizes or triggers ICx  
 11011 = ADC1 module synchronizes or triggers ICx<sup>(5)</sup>  
 11010 = CMP3 module synchronizes or triggers ICx<sup>(5)</sup>  
 11001 = CMP2 module synchronizes or triggers ICx<sup>(5)</sup>  
 11000 = CMP1 module synchronizes or triggers ICx<sup>(5)</sup>  
 10111 = Reserved  
 10110 = Reserved  
 10101 = Reserved  
 10100 = Reserved  
 10011 = IC4 module synchronizes or triggers ICx  
 10010 = IC3 module synchronizes or triggers ICx  
 10001 = IC2 module synchronizes or triggers ICx  
 10000 = IC1 module synchronizes or triggers ICx  
 01111 = Timer5 synchronizes or triggers ICx  
 01110 = Timer4 synchronizes or triggers ICx  
 01101 = Timer3 synchronizes or triggers ICx **(default)**  
 01100 = Timer2 synchronizes or triggers ICx  
 01011 = Timer1 synchronizes or triggers ICx  
 01010 = PTGOx module synchronizes or triggers ICx<sup>(6)</sup>  
 01001 = Reserved  
 01000 = Reserved  
 00111 = Reserved  
 00110 = Reserved  
 00101 = Reserved  
 00100 = OC4 module synchronizes or triggers ICx  
 00011 = OC3 module synchronizes or triggers ICx  
 00010 = OC2 module synchronizes or triggers ICx  
 00001 = OC1 module synchronizes or triggers ICx  
 00000 = No Sync or Trigger source for ICx

- Note 1:** The IC32 bit in both the Odd and Even IC must be set to enable Cascade mode.
- 2:** The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
- 3:** This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set and cleared in software.
- 4:** Do not use the ICx module as its own Sync or Trigger source.
- 5:** This option should only be selected as a trigger source and not as a synchronization source.
- 6:** Each Input Capture x (ICx) module has one PTG input source. See **Section 24.0 “Peripheral Trigger Generator (PTG) Module”** for more information.
- PTGO8 = IC1  
 PTGO9 = IC2  
 PTGO10 = IC3  
 PTGO11 = IC4

FIGURE 21-1: ECAN™ MODULE BLOCK DIAGRAM



## 21.4 ECAN Control Registers

**REGISTER 21-1: CxCTRL1: ECANx CONTROL REGISTER 1**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0
bit 15				bit 8			

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE2	OPMODE1	OPMODE0	—	CANCAP	—	—	WIN
bit 7				bit 0			

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-14      **Unimplemented:** Read as '0'
- bit 13      **CSIDL:** ECANx Stop in Idle Mode bit  
1 = Discontinues module operation when device enters Idle mode  
0 = Continues module operation in Idle mode
- bit 12      **ABAT:** Abort All Pending Transmissions bit  
1 = Signals all transmit buffers to abort transmission  
0 = Module will clear this bit when all transmissions are aborted
- bit 11      **CANCKS:** ECANx Module Clock (FCAN) Source Select bit  
1 = FCAN is equal to 2 \* FP  
0 = FCAN is equal to FP
- bit 10-8      **REQOP<2:0>:** Request Operation Mode bits  
111 = Set Listen All Messages mode  
110 = Reserved  
101 = Reserved  
100 = Set Configuration mode  
011 = Set Listen Only mode  
010 = Set Loopback mode  
001 = Set Disable mode  
000 = Set Normal Operation mode
- bit 7-5      **OPMODE<2:0>:** Operation Mode bits  
111 = Module is in Listen All Messages mode  
110 = Reserved  
101 = Reserved  
100 = Module is in Configuration mode  
011 = Module is in Listen Only mode  
010 = Module is in Loopback mode  
001 = Module is in Disable mode  
000 = Module is in Normal Operation mode
- bit 4      **Unimplemented:** Read as '0'
- bit 3      **CANCAP:** CAN Message Receive Timer Capture Event Enable bit  
1 = Enables input capture based on CAN message receive  
0 = Disables CAN capture
- bit 2-1      **Unimplemented:** Read as '0'
- bit 0      **WIN:** SFR Map Window Select bit  
1 = Uses filter window  
0 = Uses buffer window

## 21.5 ECAN Message Buffers

ECAN Message Buffers are part of RAM memory. They are not ECAN Special Function Registers. The user application must directly write into the RAM area that is configured for ECAN Message Buffers. The location and size of the buffer area is defined by the user application.

### BUFFER 21-1: ECAN™ MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	SID10	SID9	SID8	SID7	SID6
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID5	SID4	SID3	SID2	SID1	SID0	SRR	IDE
bit 7							bit 0

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-13      **Unimplemented:** Read as '0'  
 bit 12-2      **SID<10:0>:** Standard Identifier bits  
 bit 1      **SRR:** Substitute Remote Request bit  
             When IDE = 0:  
             1 = Message will request remote transmission  
             0 = Normal message  
             When IDE = 1:  
             The SRR bit must be set to '1'.  
 bit 0      **IDE:** Extended Identifier bit  
             1 = Message will transmit Extended Identifier  
             0 = Message will transmit Standard Identifier

### BUFFER 21-2: ECAN™ MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	EID17	EID16	EID15	EID14
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID13	EID12	EID11	EID10	EID9	EID8	EID7	EID6
bit 7							bit 0

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-12      **Unimplemented:** Read as '0'  
 bit 11-0      **EID<17:6>:** Extended Identifier bits

**BUFFER 21-3: ECAN™ MESSAGE BUFFER WORD 2**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15							bit 8

U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 15-10      **EID<5:0>**: Extended Identifier bits
- bit 9      **RTR**: Remote Transmission Request bit  
When IDE = 1:  
1 = Message will request remote transmission  
0 = Normal message  
When IDE = 0:  
The RTR bit is ignored.
- bit 8      **RB1**: Reserved Bit 1  
User must set this bit to '0' per CAN protocol.
- bit 7-5      **Unimplemented**: Read as '0'
- bit 4      **RB0**: Reserved Bit 0  
User must set this bit to '0' per CAN protocol.
- bit 3-0      **DLC<3:0>**: Data Length Code bits

**BUFFER 21-4: ECAN™ MESSAGE BUFFER WORD 3**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 1							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 0							
bit 7							bit 0

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 15-8      **Byte 1<15:8>**: ECAN Message Byte 1 bits
- bit 7-0      **Byte 0<7:0>**: ECAN Message Byte 0 bits

## 24.3 PTG Control Registers

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT <sup>(2)</sup>	PTGSSEN <sup>(3)</sup>	PTGIVIS
bit 15							bit 8

R/W-0	HS-0	U-0	U-0	U-0	U-0	R/W-0	
PTGSTRT	PTGWDTO	—	—	—	—	PTGITM1 <sup>(1)</sup>	PTGITM0 <sup>(1)</sup>
bit 7							bit 0

<b>Legend:</b>	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15      **PTGEN:** Module Enable bit  
1 = PTG module is enabled  
0 = PTG module is disabled
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **PTGSIDL:** PTG Stop in Idle Mode bit  
1 = Discontinues module operation when device enters Idle mode  
0 = Continues module operation in Idle mode
- bit 12      **PTGTOGL:** PTG TRIG Output Toggle Mode bit  
1 = Toggle state of the PTGOx for each execution of the PTGTRIG command  
0 = Each execution of the PTGTRIG command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits
- bit 11      **Unimplemented:** Read as '0'
- bit 10      **PTGSWT:** PTG Software Trigger bit<sup>(2)</sup>  
1 = Triggers the PTG module  
0 = No action (clearing this bit will have no effect)
- bit 9      **PTGSSEN:** PTG Enable Single-Step bit<sup>(3)</sup>  
1 = Enables Single-Step mode  
0 = Disables Single-Step mode
- bit 8      **PTGIVIS:** PTG Counter/Timer Visibility Control bit  
1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)  
0 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those limit registers
- bit 7      **PTGSTRT:** PTG Start Sequencer bit  
1 = Starts to sequentially execute commands (Continuous mode)  
0 = Stops executing commands
- bit 6      **PTGWDTO:** PTG Watchdog Timer Time-out Status bit  
1 = PTG Watchdog Timer has timed out  
0 = PTG Watchdog Timer has not timed out.
- bit 5-2      **Unimplemented:** Read as '0'

- Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.
- Note 2:** This bit is only used with the PTGCTRL step command software trigger option.
- Note 3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

**NOTES:**



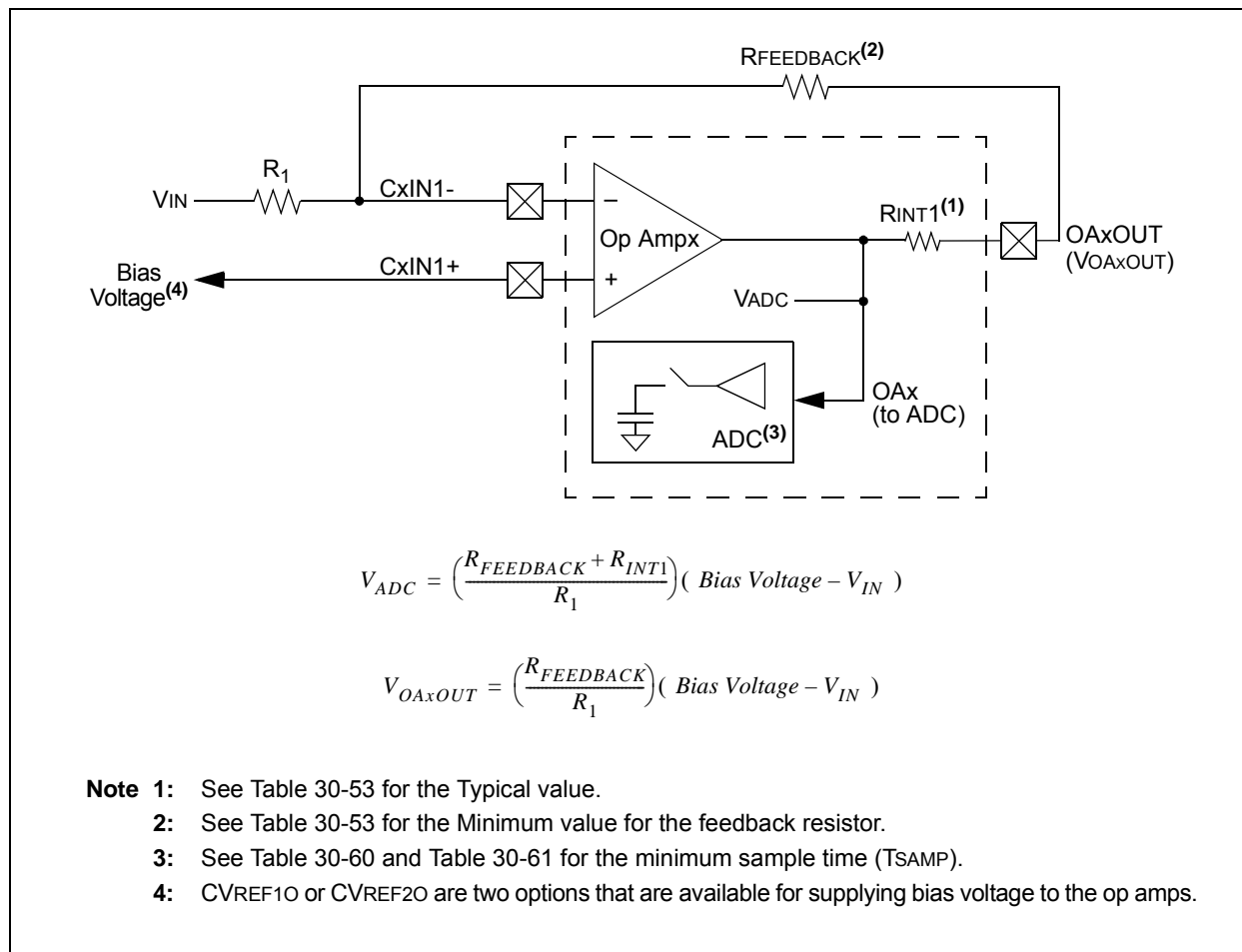
## 25.1 Op Amp Application Considerations

There are two configurations to take into consideration when designing with the op amp modules that are available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices. Configuration A (see Figure 25-6) takes advantage of the internal connection to the ADC module to route the output of the op amp directly to the ADC for measurement. Configuration B (see Figure 25-7) requires that the designer externally route the output of the op amp (OAxOUT) to a separate analog input pin (ANy) on the device. Table 30-55 in **Section 30.0 “Electrical Characteristics”** describes the performance characteristics for the op amps, distinguishing between the two configuration types where applicable.

### 25.1.1 OP AMP CONFIGURATION A

Figure 25-6 shows a typical inverting amplifier circuit taking advantage of the internal connections from the op amp output to the input of the ADC. The advantage of this configuration is that the user does not need to consume another analog input (ANy) on the device, and allows the user to simultaneously sample all three op amps with the ADC module, if needed. However, the presence of the internal resistance, RINT1, adds an error in the feedback path. Since RINT1 is an internal resistance, in relation to the op amp output (VOAxOUT) and ADC internal connection (VADC), RINT1 must be included in the numerator term of the transfer function. See Table 30-53 in **Section 30.0 “Electrical Characteristics”** for the typical value of RINT1. Table 30-60 and Table 30-61 in **Section 30.0 “Electrical Characteristics”** describe the minimum sample time (TSAMP) requirements for the ADC module in this configuration. Figure 25-6 also defines the equations that should be used when calculating the expected voltages at points, VADC and VOAxOUT.

FIGURE 25-6: OP AMP CONFIGURATION A



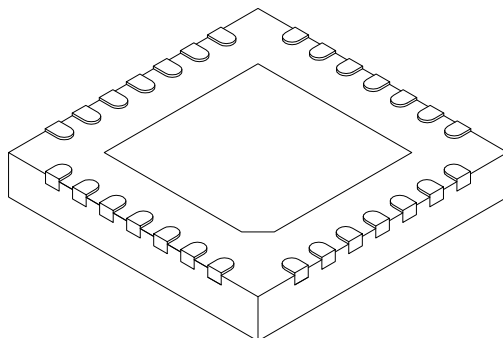
**TABLE 30-40: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)  
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	—	—	11	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS2}$ ↑ to SDO2 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	Tsch2ssH, TscL2ssH	$\overline{SS2}$ ↑ after SCK2 Edge	1.5 TCY + 40	—	—	ns	(Note 4)

- Note 1:** These parameters are characterized, but are not tested in manufacturing.
- 2:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.
- 3:** The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.
- 4:** Assumes 50 pF load on all SPI2 pins.

## 28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.70
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.70
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K	0.20	-	-

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

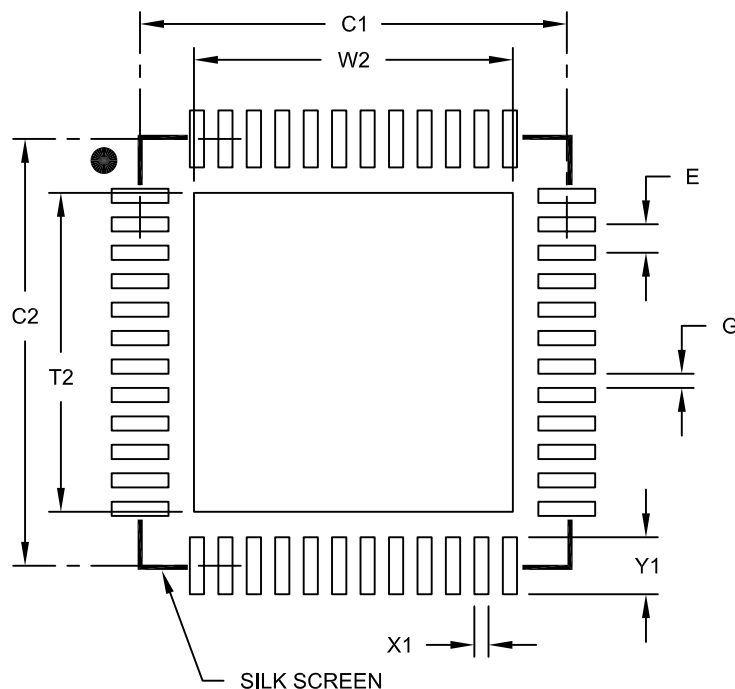
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124C Sheet 2 of 2

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]  
With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	W2			4.45
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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