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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc502t-e-so

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC35	0886	_		JTAGIP<2:()>	—		ICDIP<2:0	>	_	—	—	—	—	_	—	—	4400
IPC36	0888			PTG0IP<2:0)>	—	PT	GWDTIP<	2:0>		P	TGSTEPIP<2	:0>	—	—		—	4440
IPC37	088A		_		_	—	F	PTG3IP<2:)>			PTG2IP<2:0	>	—	F	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	_	_				—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4		—		_	_	_				—	DAE	DOOVR	—	—		—	0000
INTCON4	08C6		—		_	_	_				—	—	—	—	—		SGHT	0000
INTTREG	08C8	_	_	_	_		ILR<	3:0>		VECNUM<7:0> 0/					0000			

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: CRC REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON1	0640	CRCEN	—	CSIDL		VWORD<4:0>			CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	-	—	0000	
CRCCON2	0642	_	- <u> </u>								0000							
CRCXORL	0644		X<15:1>00										0000					
CRCXORH	0646		X<31:16> 0									0000						
CRCDATL	0648								CRC Data	Input Low V	Vord							0000
CRCDATH	064A		CRC Data Input High Word 001									0000						
CRCWDATL	064C		CRC Result Low Word 00									0000						
CRCWDATH	064E		CRC Result High Word 001										0000					

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

TABLE 4-25: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC202/502 AND PIC24EPXXXGP/MC202 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	_	—			RP35F	R<5:0>			—	—			RP20F	R<5:0>			0000
RPOR1	0682	_	_	RP37R<5:0>					—	_	RP36R<5:0> 00						0000	
RPOR2	0684	_	_		RP39R<5:0>				—	_			RP38F	२<5:0>			0000	
RPOR3	0686	_	_		RP41R<5:0>				—	_			RP40F	२<5:0>			0000	
RPOR4	0688	_	—			RP43F	R<5:0>			_	_			RP42F	२<5:0>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC203/503 AND PIC24EPXXXGP/MC203 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	_		RP35R<5:0>					_	_			RP20	R<5:0>			0000
RPOR1	0682	_	_			RP37	२<5:0>			_	_			RP36	२<5:0>			0000
RPOR2	0684	_	_		RP39R<5:0>					_	_			RP38	२<5:0>			0000
RPOR3	0686	_	_			RP41	२<5:0>			_	_	— RP40R<5:0>					0000	
RPOR4	0688	_	_			RP43	२<5:0>			_	_	RP42R<5:0>					0000	
RPOR5	068A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
RPOR6	068C			-	—	_		—			_			RP56	R<5:0>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

		11.0	11.0		11.0		
		0-0	0-0	VREGSE	0-0		VREGS
hit 15		—		VREGGE	—	Civi	bit 8
bit 10							bit 0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
bit 7						.1	bit 0
Legend:							
R = Reada	able bit	W = Writable I	oit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	TRAPR: Trap	Reset Flag bit					
	$1 = A \operatorname{Trap} Co$	onflict Reset ha	s occurred	d			
hit 11			s not occurre		ot Elog bit		
DIL 14	1 = An illega	l oncode deter	viinniiaiizeu	v Access Res	et Flay Dit ode or Uninitial	lized W registe	er used as an
	Address	Pointer caused	a Reset			ized w regiote	
	0 = An illegal	l opcode or Uni	nitialized W r	egister Reset h	as not occurred	t	
bit 13-12	Unimplemen	ted: Read as 'o)'				
bit 11	VREGSF: Fla	ish Voltage Reg	ulator Stand	by During Slee	p bit		
	1 = Flash vol	tage regulator i	s active durin	ng Sleep			
bit 10		tage regulator (naby mode dui	ing Sleep		
bit Q	CM: Configur	ation Mismatch	, Elac bit				
bit 5	1 = A Configur	ration Mismatch	h Reset has	occurred			
	0 = A Configu	ration Mismatc	h Reset has	not occurred			
bit 8	VREGS: Volta	age Regulator S	Standby Durii	ng Sleep bit			
	1 = Voltage r	egulator is activ	e during Sle	ер			
	0 = Voltage r	egulator goes in	nto Standby i	mode during SI	еер		
bit 7	EXTR: Extern	nal Reset (MCL	R) Pin bit				
	\perp = A Master 0 = A Master	Clear (pin) Res Clear (pin) Res	et has occur et has not or	rea ccurred			
bit 6	SWR: Softwa	re RESET (Instr	uction) Flag	bit			
	1 = A reset	instruction has	been execut	ed			
	0 = A RESET	instruction has	not been exe	ecuted			
bit 5	SWDTEN: So	oftware Enable/	Disable of W	DT bit ⁽²⁾			
	1 = WDT is er	nabled					
bit 4		ISADIEU hdog Timor Tim	o out Elog b	:+			
DIL 4	1 = WDT time		e-oul Flay D	IL			
	0 = WDT time	e-out has not oc	curred				
Note 1.	All of the Peset sta	itus hits can bo	set or cleare	d in software S	Setting one of th	ese hits in soft	vara does not
	cause a device Re	set.					
2:	If the FWDTEN Co SWDTEN bit settin	onfiguration bit i	s '1' (unprog	rammed), the V	VDT is always e	enabled, regard	less of the

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 7-5	INTCON3 INTERRUPT CONTROL REGISTER 3	

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15			•				bit 8
U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	—	DAE	DOOVR	—	—	—	—
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at I	POR	'1' = Bit is set	:	'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-6	Unimplemen	ted: Read as	'0'				
bit 5	DAE: DMA A	ddress Error S	oft Trap Status	s bit			
	1 = DMA add	ress error soft	trap has occur	red			
	0 = DMA add	ress error soft	trap has not o	ccurred			
bit 4	DOOVR: DO	Stack Overflow	/ Soft Trap Stat	tus bit			
	1 = DO stack	overflow soft tr	ap has occurre	ed			

	0 = DO stack overflow soft trap has not occurred
~ ~	

REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	_
bit 15			•		•		bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SGHT
bit 7			•		•		bit 0
Legend:							

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 0

SGHT: Software Generated Hard Trap Status bit

1 = Software generated hard trap has occurred

0 = Software generated hard trap has not occurred

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0			
—	—	—	—	ILR3	ILR2	ILR1	ILR0			
bit 15	·					•	bit 8			
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
VECNUM7	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown			
bit 15-12	Unimplemen	ted: Read as '	0'							
bit 11-8	ILR<3:0>: Ne	w CPU Interru	pt Priority Lev	el bits						
	1111 = CPU	Interrupt Priori	y Level is 15							
	•									
	•									
	0001 = CPU 0000 = CPU	Interrupt Priorif Interrupt Priorif	y Level is 1 y Level is 0							
bit 7-0	VECNUM<7:0	D>: Vector Nun	- nber of Pendin	g Interrupt bits						
	11111111 = 2	255, Reserved	; do not use	0 1						
	•									
	•									
	•									
	00001001 =	9, IC1 – Input (Capture 1							
	00001000 =	8, INT0 – Exte	rnal Interrupt ()						
	00000111 = 00000110 = 00000110 = 00000110 = 00000110 = 00000100000000	7, Reserved; d	o not use							
	00000101 = 5 DMAC error trap									
	00000100 =	4, Math error tr	ap							
	00000011 =	3, Stack error t	rap							
	00000010 = 2	2, Generic har	d trap							
	00000001 =	1, Address erro	or trap							
	0000000000	o, Oscillator la	nuap							

REGISTER 7-7: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

- Four DMA channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode

- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU interrupt after half or full block transfer complete
- Byte or word transfers
- · Fixed priority channel arbitration
- Manual (software) or automatic (peripheral DMA requests) transfer initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer is complete)
- DMA request for each channel can be selected from any supported interrupt source
- Debug support features

The peripherals that can utilize DMA are listed in Table 8-1.

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
INT0 – External Interrupt 0	00000000	—	—
IC1 – Input Capture 1	0000001	0x0144 (IC1BUF)	—
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	_
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	—
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	—
OC1 – Output Compare 1	00000010	_	0x0906 (OC1R) 0x0904 (OC1RS)
OC2 – Output Compare 2	00000110	_	0x0910 (OC2R) 0x090E (OC2RS)
OC3 – Output Compare 3	00011001	_	0x091A (OC3R) 0x0918 (OC3RS)
OC4 – Output Compare 4	00011010	_	0x0924 (OC4R) 0x0922 (OC4RS)
TMR2 – Timer2	00000111	—	—
TMR3 – Timer3	00001000	-	—
TMR4 – Timer4	00011011	_	—
TMR5 – Timer5	00011100	—	—
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	—
UART1TX – UART1 Transmitter	00001100	—	0x0224 (U1TXREG)
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	—
UART2TX – UART2 Transmitter	00011111	—	0x0234 (U2TXREG)
ECAN1 – RX Data Ready	00100010	0x0440 (C1RXD)	
ECAN1 – TX Data Request	01000110	—	0x0442 (C1TXD)
ADC1 – ADC1 Convert Done	00001101	0x0300 (ADC1BUF0)	_

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ROON		ROSSLP	ROSEL	RODIV3 ⁽¹⁾	RODIV2 ⁽¹⁾	RODIV1 ⁽¹⁾	RODIV0 ⁽¹⁾	
bit 15				•		•	bit 8	
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
		<u> </u>				<u> </u>		
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown	
bit 15	ROON: Refer	ence Oscillato	Output Enab	ole bit				
	1 = Reference 0 = Reference	e oscillator outr e oscillator outr	but is enabled	on the REFCL	.K pin ⁽²⁾			
bit 14	Unimplemen	ted: Read as '	o'					
bit 13	ROSSLP: Re	ference Oscilla	tor Run in Sle	ep bit				
	1 = Reference	e oscillator outp	out continues	to run in Sleep				
	0 = Reference	e oscillator outp	out is disabled	l in Sleep				
bit 12	ROSEL: Refe	erence Oscillato	or Source Sel	ect bit				
	1 = Oscillator	crystal is used	as the refere	nce clock				
hit 11_8		Peference Os	cillator Divide	r hite(1)				
Dit 11-0	1111 = Refer	ence clock divi	ded by 32 76	R				
	1110 = Refer	ence clock divi	ded by 16,384	4				
	1101 = Refer	ence clock divi	ded by 8,192					
	1100 = Refer	ence clock divi	ded by 4,096					
	1011 = Refer	ence clock divi	ded by 2,048					
	1010 = Relef	ence clock divi	ded by 1,024 ded by 512					
	1000 = Refer	ence clock divi	ded by 256					
	0111 = Refer	ence clock divi	ded by 128					
	0110 = Reference clock divided by 64 0101 = Reference clock divided by 32							
	$0 \pm 0 = \text{Reference clock divided by } 10$							
	$0011 = \text{Reference clock divided by } \delta$							
	0001 = Refer	ence clock divi	ded by 2					
	0000 = Refer	ence clock	-					
bit 7-0	Unimplemen	ted: Read as '	כ'					

REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

- **Note 1:** The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
 - 2: This pin is remappable. See Section 11.4 "Peripheral Pin Select (PPS)" for more information.

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
_				IC4R<6:0>						
bit 15							bit 8			
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
_				IC3R<6:0>						
bit 7							bit 0			
Legend:										
R = Readat	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'				
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown				
bit 15	Unimpleme	ented: Read as '	0'							
bit 14-8	IC4R<6:0>: (see Table 2	Assign Input Ca	pture 4 (IC4) selection nu) to the Correspo mbers)	onding RPn P	in bits				
	1111001 =	Input tied to RPI	121							
	•									
	•									
	0000001 =	Input tied to CM	P1							
bit 7		nput tied to vss	, 0,							
bit 6-0		Assign Input Ca	o unture 3 (IC3)) to the Correspo	ondina RPn P	in hits				
bit 0 0	(see Table 1	(see Table 11-2 for input pin selection numbers)								
	1111001 =	Input tied to RPI	121	,						
	•									
	0000001 =	Input tied to CM	P1							
	0000000 =	Input tied to Vss	5							

REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP43	R<5:0>		
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R<5:0>					

REGISTER 11-22: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

bit	7

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	RP43R<5:0>: Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP42R<5:0>: Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-23: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP55	SR<5:0>		
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—		RP54R<5:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	RP55R<5:0>: Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP54R<5:0>: Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 0

16.2 PWM Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

16.2.1 KEY RESOURCES

- "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

19.1 I²C Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

19.1.1 KEY RESOURCES

- "Inter-Integrated Circuit (I²C)" (DS70330) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5	 ADDEN: Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect 0 = Address Detect mode is disabled
bit 4	RIDLE: Receiver Idle bit (read-only) 1 = Receiver is Idle 0 = Receiver is active
bit 3	PERR: Parity Error Status bit (read-only) 1 = Parity error has been detected for the current character (character at the top of the receive FIFO) 0 = Parity error has not been detected
bit 2	<pre>FERR: Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character (character at the top of the receive FIFO) 0 = Framing error has not been detected</pre>
bit 1	 OERR: Receive Buffer Overrun Error Status bit (clear/read-only) 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receiver buffer and the UxRSR to the empty state
bit 0	 URXDA: UARTx Receive Buffer Data Available bit (read-only) 1 = Receive buffer has data, at least one more character can be read 0 = Receive buffer is empty

Note 1: Refer to the "**UART**" (DS70582) section in the "*dsPIC33/PIC24 Family Reference Manual*" for information on enabling the UARTx module for transmit operation.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
CSS31	CSS30		—	_	CSS26 ⁽²⁾	CSS25 ⁽²⁾	CSS24 ⁽²⁾
bit 15				•			bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_				—			
bit 7							bit 0
Legend:							
R = Readabl	e bit	W = Writable b	pit	U = Unimple	mented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	CSS31: ADC	1 Input Scan Se	election bit				
	1 = Selects C	TMU capacitive	and time me	asurement for	input scan (Ope	en)	
	0 = Skips CTI	MU capacitive a	ind time meas	surement for in	put scan (Open)	
bit 14	CSS30: ADC	1 Input Scan Se	election bit				
	1 = Selects C 0 = Skips CTI	TMU on-chip te MU on-chip tem	mperature mea	easurement fo surement for i	r input scan (CT nput scan (CTM	MU TEMP) IU TEMP)	
bit 13-11	Unimplemen	ted: Read as '0)'				
bit 10	CSS26: ADC	1 Input Scan Se	election bit ⁽²⁾				
	1 = Selects O	A3/AN6 for inpu	ut scan				
	0 = Skips OA	3/AN6 for input	scan				
bit 9	CSS25: ADC	1 Input Scan Se	election bit ⁽²⁾				
	1 = Selects O	A2/AN0 for inpu	ut scan				
	0 = Skips OA	2/AN0 for input	scan				
bit 8	CSS24: ADC	1 Input Scan Se	election bit ⁽²⁾				
	1 = Selects O 0 = Skips OA	A1/AN3 for input 1/AN3 for input	ut scan scan				
bit 7-0	Unimplemen	ted: Read as 'o)'				
Note 1: A	II AD1CSSH bits prresponding inpu	can be selected ut on the device	d by user softw , convert VRE	vare. However _{FL.}	r, inputs selecte	d for scan, with	out a

REGISTER 23-7: AD1CSSH: ADC1 INPUT SCAN SELECT REGISTER HIGH⁽¹⁾

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

NOTES:

27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a То comprehensive reference source. complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Familv Reference Manual', which is available from the Microchip web site (www.microchip.com).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard[™] Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming[™] (ICSP[™])
- In-Circuit Emulation

27.1 Configuration Bits

In dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored in at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

Note:	Configuration data is reloaded on all types
	of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be '1111 1111 1111 1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
72	SL	SL	f	f = Left Shift f	1	1	C,N,OV,Z
		SL	f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL	Ws,Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
73	SUB	SUB	_{Acc} (1)	Subtract Accumulators	1	1	OA,OB,OAB, SA,SB,SAB
		SUB	f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB	f,WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB	#lit10,Wn	Wn = Wn - lit10	1	1	C,DC,N,OV,Z
		SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
74	SUBB	SUBB	f	$f = f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	f,WREG	WREG = $f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	#lit10,Wn	Wn = Wn – lit10 – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB	Wb,Ws,Wd	$Wd = Wb - Ws - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	Wb,#lit5,Wd	$Wd = Wb - lit5 - (\overline{C})$	1	1	C,DC,N,OV,Z
75	SUBR	SUBR	f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	f,WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
76	SUBBR	SUBBR	f	$f = WREG - f - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	f,WREG	WREG = WREG – f – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR	Wb,Ws,Wd	$Wd = Ws - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	Wb,#lit5,Wd	$Wd = lit5 - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
77	SWAP	SWAP.b	Wn	Wn = nibble swap Wn	1	1	None
		SWAP	Wn	Wn = byte swap Wn	1	1	None
78	TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	5	None
79	TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	5	None
80	TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
81	TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
82	ULNK	ULNK		Unlink Frame Pointer	1	1	SFA
83	XOR	XOR	f	f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
84	ZE	ZE	Ws,Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.





FIGURE 30-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)



TABLE 30-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			Standa (unless Operati	rd Opera otherwis ng tempe	ting Con se stated rature	ditions: 3) -40°C ≤ T -40°C ≤ T	3.0V to 3.6V $A \le +85^{\circ}C$ for Industrial $A \le +125^{\circ}C$ for Extended
Param No. Symbol Characteristic ⁽¹⁾ Min. Typ. Max. Units						Conditions	
MP10	TFPWM	PWMx Output Fall Time	_	—		ns	See Parameter DO32
MP11	TRPWM	PWMx Output Rise Time	—	_		ns	See Parameter DO31
MP20	TFD	Fault Input ↓ to PWMx I/O Change	-		15	ns	
MP30	Tfh	Fault Input Pulse Width	15	—		ns	

Note 1: These parameters are characterized but not tested in manufacturing.

31.1 High-Temperature DC Characteristics

TABLE 31-1: OPERATING MIPS VS. VOLTAGE

			Max MIPS		
Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X		
HDC5	3.0 to 3.6V ⁽¹⁾	-40°C to +150°C	40		

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules, such as the ADC, may have degraded performance. Device functionality is tested but not characterized.

TABLE 31-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit
High-Temperature Devices					
Operating Junction Temperature Range	TJ	-40		+155	°C
Operating Ambient Temperature Range	TA	-40	—	+150	°C
Power Dissipation: Internal Chip Power Dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ I/O Pin Power Dissipation: $I/O = \Sigma (\{VDD - VOH\} x IOH) + \Sigma (VOL x IOL)$	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJ	IA	W

TABLE 31-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARA	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$								
Parameter No.	Symbol	Characteristic	Min Typ Max Units Conditions						
Operating Voltage									
HDC10	Supply Voltage								
	Vdd	_	3.0 3.3 3.6 V -40°C to +150°C						

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	MILLIMETERS					
Dimension	l Limits	MIN	NOM	MAX		
Number of Pins	Ν		28			
Pitch	е		1.27 BSC			
Overall Height	Α	-	-	2.65		
Molded Package Thickness	A2	2.05	-	-		
Standoff §	A1	0.10	-	0.30		
Overall Width	E	10.30 BSC				
Molded Package Width	E1	7.50 BSC				
Overall Length	D		17.90 BSC			
Chamfer (Optional)	h	0.25	-	0.75		
Foot Length	L	0.40	-	1.27		
Footprint	L1	1.40 REF				
Lead Angle	Θ	0°	-	-		
Foot Angle	φ	0°	-	8°		
Lead Thickness	С	0.18	-	0.33		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5°	-	15°		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

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48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing C04-153A Sheet 1 of 2