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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc504t-e-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Internut Course	Vector	IRQ		Interrupt Bit Location		
Interrupt Source	#	#	IVI Address	Flag	Enable	Priority
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
IC1 – Input Capture 1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
OC1 – Output Compare 1	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
T1 – Timer1	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
IC2 – Input Capture 2	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>
OC2 – Output Compare 2	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
T2 – Timer2	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
T3 – Timer3	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1E – SPI1 Error	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 – SPI1 Transfer Done	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
AD1 – ADC1 Convert Done	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
DMA1 – DMA Channel 1	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
Reserved	23	15	0x000032	_	_	_
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
CM – Comparator Combined Event	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
CN – Input Change Interrupt	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
INT1 – External Interrupt 1	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
Reserved	29-31	21-23	0x00003E-0x000042	_	_	_
DMA2 – DMA Channel 2	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
OC3 – Output Compare 3	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
OC4 – Output Compare 4	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
T4 – Timer4	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
T5 – Timer5	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
SPI2E – SPI2 Error	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 – SPI2 Transfer Done	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>
C1RX – CAN1 RX Data Ready ⁽¹⁾	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
C1 – CAN1 Event ⁽¹⁾	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
DMA3 – DMA Channel 3	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
IC3 – Input Capture 3	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
IC4 – Input Capture 4	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
Reserved	47-56	39-48	0x000062-0x000074	—	—	_
SI2C2 – I2C2 Slave Event	57	49	0x000076	IFS3<1>	IEC3<1>	IPC12<6:4>
MI2C2 – I2C2 Master Event	58	50	0x000078	IFS3<2>	IEC3<2>	IPC12<10:8>
Reserved	59-64	51-56	0x00007A-0x000084			
PSEM – PWM Special Event Match ⁽²⁾	65	57	0x000086	IFS3<9>	IEC3<9>	IPC14<6:4>

TABLE 7-1: INTERRUPT VECTOR DETAILS

Note 1: This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

2: This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR ⁽¹⁾	OVBERR ⁽¹⁾	COVAERR ⁽¹⁾	COVBERR ⁽¹⁾	OVATE ⁽¹⁾	OVBTE ⁽¹⁾	COVTE ⁽¹⁾
bit 15							bit 8
r							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR ⁽¹) DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0
[
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpleme	ented bit, read a	as '0'	
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is clea	red	x = Bit is unk	nown
bit 15	NSTDIS: Inte	errupt Nesting	Disable bit				
	\perp = Interrupt	nesting is disa	ibled				
bit 14	OVAFRR: A	ccumulator A (Overflow Trap F	lag bit(1)			
2	1 = Trap was	s caused by ov	erflow of Accur	nulator A			
	0 = Trap was	s not caused b	y overflow of A	ccumulator A			
bit 13	OVBERR: A	ccumulator B (Overflow Trap F	lag bit ⁽¹⁾			
	1 = Trap was	s caused by ow	erflow of Accur	nulator B			
	0 = Irap was	s not caused b	y overflow of A	ccumulator B	(1)		
bit 12	COVAERR:	Accumulator A	Catastrophic (Jverflow Trap FI	ag bit("		
	1 = Trap was 0 = Trap was	s not caused by ca	v catastrophic over	overflow of Accu	mulator A		
bit 11	COVBERR:	Accumulator E	Catastrophic (Overflow Trap Fl	ag bit ⁽¹⁾		
	1 = Trap was	s caused by ca	tastrophic over	flow of Accumul	ator B		
	0 = Trap was	s not caused b	y catastrophic o	overflow of Accu	mulator B		
bit 10	OVATE: Acc	umulator A Ov	erflow Trap En	able bit ⁽¹⁾			
	1 = Trap ove	rflow of Accun	nulator A				
hit 0			orflow Tran En	able bit(1)			
DIL 9	1 = Tran ove	rflow of Accun	nulator B				
	0 = Trap is d	isabled					
bit 8	COVTE: Cat	astrophic Ove	rflow Trap Enat	ole bit ⁽¹⁾			
	1 = Trap on o	catastrophic ov	erflow of Accu	mulator A or B is	s enabled		
	0 = Trap is d	isabled					
bit 7	SFTACERR:	Shift Accumu	lator Error Statu	us bit ⁽¹⁾			
	1 = Math erro	or trap was ca or trap was po	used by an inva t caused by an	alid accumulator	shift ator shift		
hit 6		ivide-hv-Zero	Error Status bit				
bit o	1 = Math erro	or trap was ca	used by a divide	e-bv-zero			
	0 = Math erro	or trap was no	t caused by a d	ivide-by-zero			
bit 5	DMACERR:	DMAC Trap F	lag bit				
	1 = DMAC tr	ap has occurre	ed				
	0 = DMAC tr	ap has not occ	curred				
Note 1: The	ese bits are ava	ailable on dsPl	C33EPXXXMC	20X/50X and de	PIC33EPXXX	GP50X devices	s only.

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

8.0 DIRECT MEMORY ACCESS (DMA)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Direct Memory Access (DMA)" (DS70348) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The DMA Controller transfers data between Peripheral Data registers and Data Space SRAM

In addition, DMA can access the entire data memory space. The Data Memory Bus Arbiter is utilized when either the CPU or DMA attempts to access SRAM, resulting in potential DMA or CPU stalls.

The DMA Controller supports 4 independent channels. Each channel can be configured for transfers to or from selected peripherals. Some of the peripherals supported by the DMA Controller include:

- ECAN[™]
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI)
- UART
- Input Capture
- Output Compare

Refer to Table 8-1 for a complete list of supported peripherals.

FIGURE 8-1: DMA CONTROLLER MODULE



NOTES:

11.5 I/O Helpful Tips

- 1. In some cases, certain pins, as defined in Table 30-11, under "Injection Current", have internal protection diodes to VDD and Vss. The term, "Injection Current", is also referred to as "Clamp Current". On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the Vss and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device, that is clamped internally by the VDD and Vss power rails, may affect the ADC accuracy by four to six counts.
- 2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.
- **Note:** Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.
- 3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
- 4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD - 0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.

5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH, and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:

VOH = 2.4V @ IOH = -8 mA and VDD = 3.3VThe maximum output current sourced by any 8 mA I/O pin = 12 mA.

LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in Section 30.0 "Electrical Characteristics" for additional information.

- 6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
 - a) Only one "output" function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
 - b) It is possible to assign a "remappable output" function to multiple pins and externally short or tie them together for increased current drive.
 - c) If any "dedicated output" function is enabled on a pin, it will take precedence over any remappable "output" function.
 - d) If any "dedicated digital" (input or output) function is enabled on a pin, any number of "input" remappable functions can be mapped to the same pin.
 - e) If any "dedicated analog" function(s) are enabled on a given pin, "digital input(s)" of any kind will all be disabled, although a single "digital output", at the user's cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input provided there is no external analog input, such as for a built-in self-test.
 - f) Any number of "input" remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable "output".

12.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

12.1.1 KEY RESOURCES

- "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

15.2 Output Compare Control Registers

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0		
		OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	_	ENFLTB		
bit 15							bit 8		
R/W-0	U-0	R/W-0, HSC	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0		
ENFLTA		OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0		
bit 7							bit 0		
Legend:		HSC = Hardw	are Settable/Cl	earable bit					
R = Reada	ible bit	W = Writable I	bit	U = Unimplem	nented bit, read	as '0'			
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown		
bit 15-14	Unimplemen	ted: Read as '0)'						
bit 13	OCSIDL: Out	tput Compare x	Stop in Idle Mo	de Control bit					
	1 = Output C	compare x Halts	in CPU Idle me	ode via CDU Idia m	odo				
bit 12 10			nues lo operale		oue				
DIL 12-10	111 = Perinh	eral clock (Ep)	pare x Clock S						
	110 = Reserv	/ed							
	101 = PTGO	x clock ⁽²⁾							
	100 = T1CLK	is the clock so	urce of the OC	k (only the sync	hronous clock	is supported)			
	011 = 15CLK	is the clock sou	urce of the OC	Х У					
	001 = T3CLK	is the clock so	urce of the OC	x X					
	000 = T2CLK	is the clock so	urce of the OC	ĸ					
bit 9	Unimplemen	ted: Read as '0)'						
bit 8	ENFLTB: Fau	ult B Input Enab	le bit						
	1 = Output C 0 = Output C	ompare Fault B compare Fault B	input (OCFB) input (OCFB)	is enabled is disabled					
bit 7	ENFLTA: Fau	ult A Input Enabl	le bit						
	1 = Output C	ompare Fault A	input (OCFA)	is enabled					
	0 = Output C	ompare Fault A	input (OCFA)	is disabled					
bit 6	Unimplemen	ted: Read as '0)'						
bit 5	OCFLTB: PW	M Fault B Cond	dition Status bit						
	1 = PWM Fa 0 = No PWM	ult B condition of Fault B condition	on OCFB pin ha on on OCFB pi	as occurred n has occurred					
bit 4	OCFLTA: PW	/M Fault A Cond	dition Status bit						
	1 = PWM Fa	ult A condition of	on OCFA pin ha	as occurred					
	0 = No PWM	I Fault A condition	on on OCFA pi	n has occurred					
Note 1:	OCxR and OCxF	RS are double-b	ouffered in PWN	A mode only.					
2:	Each Output Cor	mpare x module	(OCx) has one	PTG clock sou	urce. See Secti	on 24.0 "Perip	oheral Trigger		
	Generator (PTG PTGO4 = OC1) wodule" for r	nore informatio	n.					
	PTGO5 = OC2								
	PTGO6 = OC3								
	PTGO7 = OC4	PTG07 = 0C4							

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	TRGDIV<3:0>			—	—	—	—
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			TRGSTF	RT<5:0>(1)		
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own
bit 15-12	TRGDIV<3:0)>: Trigger # Ou	tput Divider b	vits			
	1111 = Trigg	er output for ev	ery 16th trigg	er event			
	1110 = Trigg	er output for ev	ery 15th trigg	er event			
	1101 = Trigg	er output for ev	ery 14th trigg	er event			
	1100 = Trigg	er output for ev	ery 13th trigg	er event			
	1011 = Irigg	er output for ev	ery 12th trigg	er event			
	1010 = Trigg	per output for ev	ery 11th trigge	er event			
	1001 - Trigg	er output for ev	ery 9th triage	r event			
	0111 = Trigg	er output for ev	erv 8th triage	r event			
	0110 = Trigg	er output for ev	erv 7th triage	r event			
	0101 = Trigg	er output for ev	ery 6th trigge	r event			
	0100 = Trigg	jer output for ev	ery 5th trigge	r event			
	0011 = Trigg	er output for ev	ery 4th trigge	r event			
	0010 = Trigg	er output for ev	ery 3rd trigge	r event			
	0001 = Trigg	er output for ev	ery 2nd trigge	erevent			
	0000 = Trigg	ger output for ev	ery trigger ev	ent			
bit 11-6	Unimplemer	nted: Read as '	0'				
bit 5-0	TRGSTRT<5	5:0>: Trigger Po	stscaler Start	Enable Select	bits ⁽¹⁾		
	111111 = W	aits 63 PWM cy	cles before g	enerating the fir	rst trigger event	after the modu	le is enabled
	•						
	•						
	•						
	000010 = W	aits 2 PWM cyc	les before ge	nerating the firs	t trigger event a	after the module	e is enabled
	000001 = W	aits 1 PWM cyc	le before gen	erating the first	trigger event a	fter the module	is enabled
	000000 = W	aits 0 PWM cyc	les before ge	nerating the firs	t trigger event	after the module	e is enabled

REGISTER 16-12: TRGCONx: PWMx TRIGGER CONTROL REGISTER



17.1 QEI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

17.1.1 KEY RESOURCES

- "Quadrature Encoder Interface" (DS70601) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 21-8:	CxEC: ECANx TRANSMIT/RECEIVE ERROR COUNT REGISTER
REGISTER 21-8:	CXEC: ECANX TRANSMIT/RECEIVE ERROR COUNT REGISTE

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			TERR	CNT<7:0>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			RERR	CNT<7:0>			
bit 7							bit 0
Legend:							
R = Readable bi	t	W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at PC	R	'1' = Bit is set		'0' = Bit is clear	red	x = Bit is unknowr	า

bit 15-8	TERRCNT<7:0>:	Transmit Error	Count bits
DIL 10-0	IERRGNI < 1.0>.	Hanshill Enoi	Count bits

bit 7-0 **RERRCNT<7:0>:** Receive Error Count bits

REGISTER 21-9: CxCFG1: ECANx BAUD RATE CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 |
| bit 7 | | | • | • | | | bit 0 |

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-8	Unimplemented: Read as '0'
----------	----------------------------

bit 7-6	SJW<1:0>: Synchronization Jump Width bits
	11 = Length is 4 x TQ
	$10 = \text{Length is } 3 \times \text{Tq}$
	01 = Length is 2 x TQ
	00 = Length is 1 x TQ

```
bit 5-0 BRP<5:0>: Baud Rate Prescaler bits
```

```
11 1111 = TQ = 2 x 64 x 1/FCAN
```

•

- 00 0010 = TQ = 2 x 3 x 1/FCAN 00 0001 = TQ = 2 x 2 x 1/FCAN
- 00 0000 = Tq = 2 x 1 x 1/FCAN

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	F15B	P<3:0>			F14B	R/W-0 R/W-1 IP<3:0> R/W-0 R/W-0 R/W-1 IP<3:0> Image: state	
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
-	F13B	P<3:0>			F12B	P<3:0>	
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		U = Unimpler	nented bit, rea	d as '0'			
-n = Value a	t POR	'1' = Bit is set	t	'0' = Bit is cle	ared	x = Bit is unki	nown
L							
bit 15-12	F15BP<3:0	>: RX Buffer Ma	sk for Filter 1	5 bits			
	1111 = Filte	er hits received in	n RX FIFO bu	uffer			
	1110 = Filte	r hits received in	n RX Buffer 1	4			
	•						
	•						
	•	n hito no ocivio d iv					
	0001 = Filte	r hits received ii					
h:+ 44 0				4 h:ta (a a ma a ma)			
DIT 11-8	F14BP<3:0	>: RX Buffer Ma	SK for Fliter 1	4 bits (same va	iues as bits<15):12>)	
bit 7-4	F13BP<3:0	>: RX Buffer Ma	sk for Filter 1	3 bits (same va	lues as bits<15	5:12>)	
bit 3-0	F12BP<3:0	RX Buffer Ma	sk for Filter 1	2 bits (same va	lues as bits<15	5:12>)	

REGISTER 21-15: CxBUFPNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-22: CxRXFUL1: ECANx RECEIVE BUFFER FULL REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8
bit 15							bit 8

| R/C-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| RXFUL7 | RXFUL6 | RXFUL5 | RXFUL4 | RXFUL3 | RXFUL2 | RXFUL1 | RXFUL0 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 **RXFUL<15:0>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

REGISTER 21-23: CxRXFUL2: ECANx RECEIVE BUFFER FULL REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL31 | RXFUL30 | RXFUL29 | RXFUL28 | RXFUL27 | RXFUL26 | RXFUL25 | RXFUL24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL23 | RXFUL22 | RXFUL21 | RXFUL20 | RXFUL19 | RXFUL18 | RXFUL17 | RXFUL16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 **RXFUL<31:16>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

NOTES:



dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 23-5: AD1CHS123: ADC1 INPUT CHANNEL 1, 2, 3 SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CH123NB1	CH123NB0	CH123SB
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0

0-0	0-0	0-0	0-0	0-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CH123NA1	CH123NA0	CH123SA
bit 7							bit 0

Legend:

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 Unimplemented: Read as '0'

bit 10-9

CH123NB<1:0>: Channel 1, 2, 3 Negative Input Select for Sample MUXB bits

In 12-bit mode (AD21B = 1), CH123NB is Unimplemented and is Read as '0':

Value	ADC Channel				
	CH1	CH2	CH3		
11	AN9	AN10	AN11		
10 (1,2)	OA3/AN6	AN7	AN8		
0x	VREFL	VREFL	VREFL		

bit 8 **CH123SB:** Channel 1, 2, 3 Positive Input Select for Sample MUXB bit In 12-bit mode (AD21B = 1), CH123SB is Unimplemented and is Read as '0':

Value	ADC Channel				
value	CH1	CH2	СНЗ		
1 (2)	OA1/AN3	OA2/AN0	OA3/AN6		
0 (1,2)	OA2/AN0	AN1	AN2		

bit 7-3 Unimplemented: Read as '0'

bit 2-1 **CH123NA<1:0>:** Channel 1, 2, 3 Negative Input Select for Sample MUXA bits In 12-bit mode (AD21B = 1), CH123NA is Unimplemented and is Read as '<u>0</u>':

Value	ADC Channel				
value	CH1	CH2	CH3		
11	AN9	AN10	AN11		
10 (1,2)	OA3/AN6	AN7	AN8		
0x	VREFL	VREFL	VREFL		

- **Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
 - 2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3) (CONTINUED)

bit 7-6	EVPOL<1:0>: Trigger/Event/Interrupt Polarity Select bits
	 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0) 10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
	If CPOL = 1 (inverted polarity): Low-to-high transition of the comparator output.
	If CPOL = 0 (non-inverted polarity): High-to-low transition of the comparator output.
	01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity-selected comparator output (while CEVT = 0)
	If CPOL = 1 (inverted polarity): High-to-low transition of the comparator output.
	If CPOL = 0 (non-inverted polarity): Low-to-high transition of the comparator output
	00 = Trigger/event/interrupt generation is disabled
bit 5	Unimplemented: Read as '0'
bit 4	CREF: Comparator Reference Select bit (VIN+ input) ⁽¹⁾
	 1 = VIN+ input connects to internal CVREFIN voltage⁽²⁾ 0 = VIN+ input connects to CxIN1+ pin
bit 3-2	Unimplemented: Read as '0'
bit 1-0	CCH<1:0>: Op Amp/Comparator Channel Select bits ⁽¹⁾
	 11 = Unimplemented 10 = Unimplemented 01 = Inverting input of the comparator connects to the CxIN2- pin⁽²⁾ 00 = Inverting input of the op amp/comparator connects to the CxIN1- pin

- **Note 1:** Inputs that are selected and not available will be tied to Vss. See the "**Pin Diagrams**" section for available inputs for each package.
 - 2: This output is not available when OPMODE (CMxCON<10>) = 1.

Base Instr #	Assembly Mnemonic	/ Assembly Syntax		Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	С
26	DEC	DEC f f=f-1		1	1	C,DC,N,OV,Z	
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws - 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws - 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF	Wm, Wn ⁽¹⁾	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO	#lit15,Expr ⁽¹⁾	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO	Wn,Expr ⁽¹⁾	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd ⁽¹⁾	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC	Wm*Wm,Acc,Wx,Wy,Wxd ⁽¹⁾	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
34	EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL	Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	С
36	FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	С
37	FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	С
38	GOTO	GOTO	Expr	Go to address	2	4	None
		GOTO	Wn	Go to indirect	1	4	None
		GOTO.L	Wn	Go to indirect (long address)	1	4	None
39	INC	INC	f	f = f + 1	1	1	C,DC,N,OV,Z
		INC	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2	f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2	f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2	Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR	f	f = f .IOR. WREG	1	1	N,Z
		IOR	f,WREG	WREG = f.IOR. WREG	1	1	N,Z
		IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC	Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
43	LNK	LNK	#lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR	f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
	LSR Wb, Wns, Wnd Wnd = Logical Right Shift Wb b		Wnd = Logical Right Shift Wb by Wns	1	1	N,Z	
		LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB ⁽¹⁾	Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd ⁽¹⁾	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 30-47:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	15	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	—	-	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time			_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	-	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120		—	ns	
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	_	ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.



1:128

70

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Contact Pitch E		0.40 BSC		
Optional Center Pad Width	W2	4.45		
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A