

Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFl

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8×8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc504t-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### Pin Diagrams (Continued)



#### Pin Diagrams (Continued)





#### FIGURE 4-3: PROGRAM MEMORY MAP FOR dsPIC33EP128GP50X, dsPIC33EP128MC20X/50X AND PIC24EP128GP/MC20X DEVICES

#### 4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in wordaddressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-6).

Program memory addresses are always word-aligned on the lower word and addresses are incremented, or decremented by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

### 4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices reserve the addresses between 0x000000 and 0x000200 for hardcoded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 7.1** "Interrupt Vector Table".



#### FIGURE 4-6: PROGRAM MEMORY ORGANIZATION

TABLE 4	4-31:	PER	IPHERA	L PIN S	ELECT	INPUT F	REGISTI	ER MAP	FOR ds	sPIC33E	PXXXG	P50X D	EVICES	3 ONLY	

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—				INT1R<6:0>					—	—	—	—	_			0000
RPINR1	06A2		_			_	_		—		- INT2R<6:0>					0000		
RPINR3	06A6		_			_	_		—		- T2CKR<6:0>					0000		
RPINR7	06AE					IC2R<6:0>					IC1R<6:0>					0000		
RPINR8	06B0	_				IC4R<6:0>				_	- IC3R<6:0>					0000		
RPINR11	06B6	_	_	_	_	_	-	_	_	_			(	DCFAR<6:0	>			0000
RPINR18	06C4	_	_	_	_	_	-	_	_	_			l	J1RXR<6:0	>			0000
RPINR19	06C6	_	_	_	_	_	-	_	_	_			l	J2RXR<6:0	>			0000
RPINR22	06CC	_			S	CK2INR<6:0	)>			_	SDI2R<6:0> 0					0000		
RPINR23	06CE	_	_	_	_	_	-	_	_	_	SS2R<6:0> 00					0000		
RPINR26	06D4	_	_	-		_	—		_		C1RXR<6:0>					0000		

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### **TABLE 4-32:** PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—				INT1R<6:0>	>			_	—	—	—			_	_	0000
RPINR1	06A2	_	_	_	_	_	_	_	_	_	INT2R<6:0>				0000			
RPINR3	06A6	_	_	_	_	_	_	_	_	_			-	T2CKR<6:0>	>			0000
RPINR7	06AE	_				IC2R<6:0>				_	IC1R<6:0>					0000		
RPINR8	06B0	_				IC4R<6:0>				_	IC3R<6:0>					0000		
RPINR11	06B6	_	_	_	_	_	_	_	_	_			(	DCFAR<6:0	>			0000
RPINR12	06B8	_				FLT2R<6:0>	>			_				FLT1R<6:0>	•			0000
RPINR14	06BC	_			(	QEB1R<6:0	>			_			(	QEA1R<6:0	>			0000
RPINR15	06BE	_			Н	OME1R<6:(	)>			_			I	NDX1R<6:0	>			0000
RPINR18	06C4	_	_	_	_	_	_	_	_	_			ι	J1RXR<6:0	>			0000
RPINR19	06C6	_	_	_	_	_	_	_	_	_			ι	J2RXR<6:0	>			0000
RPINR22	06CC	_			S	CK2INR<6:	0>			_				SDI2R<6:0>				0000
RPINR23	06CE	_	_	_	_	_	-	_	_	_				SS2R<6:0>				0000
RPINR26	06D4	_	_	_	_	_	_	_	_	_			(	C1RXR<6:0	>			0000
RPINR37	06EA	_			S	YNCI1R<6:	0>			_						0000		
RPINR38	06EC	—			D	CMP1R<6	:0>			—						0000		
RPINR39	06EE	_			D	CMP3R<6	:0>			_	DTCMP2R<6:0> C					0000		

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

#### TABLE 4-39: PMD REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD	AD1MD	0000
PMD2	0762	_	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	_	_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	CRCMD	_	_	_	_	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	_	_	_	_	_	_	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
PMD7	076C		_			_		_		_	_		DMA0MD DMA1MD DMA2MD DMA3MD	PTGMD	_	_	_	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### TABLE 4-40: PMD REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD	AD1MD	0000
PMD2	0762	_	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	—	_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	CRCMD	_	—	_	—	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	_	_	_	_	_	—	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	_	_	PWM3MD	PWM2MD	PWM1MD	_	_	—	_	—	_	_	_	0000
													DMA0MD					
	0760												DMA1MD	DTOMD				
PIVID7	0760	_	_	_	_	_	_	_	_	_	_	_	DMA2MD	PIGMD	_	_	_	0000
													DMA3MD	]				

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

DS70000657H-page 95

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ILR3	ILR2	ILR1	ILR0
bit 15	·					•	bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VECNUM7	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-12	Unimplemen	ted: Read as '	0'				
bit 11-8	ILR<3:0>: Ne	w CPU Interru	pt Priority Lev	el bits			
	1111 = CPU	Interrupt Priori	y Level is 15				
	•						
	•						
	0001 = CPU 0000 = CPU	Interrupt Priorif Interrupt Priorif	y Level is 1 y Level is 0				
bit 7-0	VECNUM<7:0	D>: Vector Nun	- nber of Pendin	g Interrupt bits			
	11111111 = 2	255, Reserved	; do not use	0			
	•						
	•						
	•						
	00001001 =	9, IC1 – Input (	Capture 1				
	00001000 =	8, INT0 – Exte	rnal Interrupt (	)			
	00000111 = 00000110 = 00000110 = 00000110 = 00000110 = 00000100000000	7, Reserved; d	o not use				
	00000101 = 00000101 = 000000101 = 00000000	5. DMAC error	trap				
	00000100 =	4, Math error tr	ap				
	00000011 =	3, Stack error t	rap				
	00000010 = 2	2, Generic har	d trap				
	00000001 =	1, Address erro	or trap				
	0000000000	o, Oscillator la	nuap				

#### REGISTER 7-7: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

#### REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

- bit 3 SPI1MD: SPI1 Module Disable bit 1 = SPI1 module is disabled
  - 0 = SPI1 module is enabled
- bit 2 Unimplemented: Read as '0'
- bit 1 C1MD: ECAN1 Module Disable bit<sup>(2)</sup> 1 = ECAN1 module is disabled 0 = ECAN1 module is enabled
- bit 0 AD1MD: ADC1 Module Disable bit 1 = ADC1 module is disabled 0 = ADC1 module is enabled
- Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
  - 2: This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

NOTES:



#### FIGURE 18-1: SPIX MODULE BLOCK DIAGRAM

#### REGISTER 18-1: SPIx STAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 1 SPITBF: SPIx Transmit Buffer Full Status bit
  - 1 = Transmit not yet started, SPIxTXB is full
  - 0 = Transmit started, SPIxTXB is empty

#### Standard Buffer mode:

Automatically set in hardware when core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.

#### Enhanced Buffer mode:

Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

#### bit 0 SPIRBF: SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full

0 = Receive is incomplete, SPIxRXB is empty

#### Standard Buffer mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

#### Enhanced Buffer mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

### 21.2 Modes of Operation

The ECAN module can operate in one of several operation modes selected by the user. These modes include:

- · Initialization mode
- Disable mode
- Normal Operation mode
- · Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

#### 21.3 ECAN Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

#### 21.3.1 KEY RESOURCES

- "Enhanced Controller Area Network (ECAN™)" (DS70353) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- · Development Tools

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

#### REGISTER 21-19: CxFMSKSEL2: ECANx FILTER 15-8 MASK SELECTION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15M	ISK<1:0>	F14MS	K<1:0>	F13MS	SK<1:0>	F12MS	K<1:0>
bit 15							bit 8
	<b>D</b> 444 0	Date	<b>D M</b> ( <b>0</b>	<b>D</b> 444 0	<b>D</b> 444 0	<b>D</b> 444 0	<b>D</b> 444 0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11M	SK<1:0>	F10MS	K<1:0>	F9MS	K<1:0>	F8MS	K<1:0>
bit 7							bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-14	F15MSK<1: 11 = Reserv 10 = Accept 01 = Accept 00 = Accept	<b>0&gt;:</b> Mask Sourc ed ance Mask 2 reg ance Mask 1 reg ance Mask 0 reg	e for Filter 15 gisters contair gisters contair gisters contair	bits n mask n mask n mask			
bit 13-12	F14MSK<1:	0>: Mask Source	e for Filter 14	bits (same valu	ues as bits<15:	14>)	
bit 11-10	F13MSK<1:	0>: Mask Sourc	e for Filter 13	bits (same valu	ues as bits<15:	14>)	
bit 9-8	F12MSK<1:	0>: Mask Sourc	e for Filter 12	bits (same valu	ues as bits<15:	14>)	
bit 7-6	F11MSK<1:	0>: Mask Sourc	e for Filter 11	bits (same valu	ies as bits<15:	14>)	
bit 5-4	F10MSK<1:	0>: Mask Sourc	e for Filter 10	bits (same valu	ues as bits<15:	14>)	
bit 3-2	F9MSK<1:0	>: Mask Source	for Filter 9 bit	ts (same values	s as bits<15:14	>)	
bit 1-0	F8MSK<1:0	>: Mask Source	for Filter 8 bit	ts (same values	s as bits<15:14	>)	

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

#### REGISTER 26-3: CRCXORH: CRC XOR POLYNOMIAL HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			X<3	31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			X<2	3:16>			
bit 7							bit 0
Legend:							
R = Readable b	bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 X<31:16>: XOR of Polynomial Term X<sup>n</sup> Enable bits

#### REGISTER 26-4: CRCXORL: CRC XOR POLYNOMIAL LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		Х<	15:8>			
						bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
		X<7:1>				—
						bit 0
t	W = Writable	bit	U = Unimplen	nented bit, rea	nd as '0'	
R	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
· · · · · · · · · · · · · · · · · · ·	R/W-0	R/W-0     R/W-0       t     W = Writable       0R     '1' = Bit is set	R/W-0     R/W-0     R/W-0       X<7:1>       W = Writable bit       0R     '1' = Bit is set	R/W-0 R/W-0 R/W-0 R/W-0   X<15:8>   X<7:1>   U U   U U   U U   U U   U U   U U   U U   U U   U U   U U   U U   U U   U U   U U   U U   U U   U U	R/W-0 R/W-0 R/W-0 R/W-0   X<15:8>   X<7:1>   U	R/W-0 R/W-0 R/W-0 R/W-0 R/W-0   X<15:8>   R/W-0 R/W-0 R/W-0   X<7:1>     t W = Writable bit U = Unimplemented bit, read as '0'   VR '1' = Bit is set '0' = Bit is cleared x = Bit is unkr

bit 15-1X<15:1>: XOR of Polynomial Term X<sup>n</sup> Enable bitsbit 0Unimplemented: Read as '0'



#### FIGURE 30-24: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS

# TABLE 30-43:SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1)TIMING REQUIREMENTS

AC CHA	RACTERIST	ICS	Standard (unless o Operating	<b>Operatin</b> otherwise temperation	<b>g Conditi stated)</b> ture -40° -40°	ons: 3.0\ °C ≤ Ta ≤ °C ≤ Ta ≤	<b>/ to 3.6V</b> +85°C for Industrial +125°C for Extended
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	_		10	MHz	(Note 3)
SP20	TscF	SCK1 Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK1 Output Rise Time	_	—	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—		ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30			ns	

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.
- **4:** Assumes 50 pF load on all SPI1 pins.

#### 33.1 Package Marking Information (Continued)

48-Lead UQFN (6x6x0.5 mm)



Example 33EP64GP 504-I/MV (3) 1310017

64-Lead QFN (9x9x0.9 mm)



Example dsPIC33EP 64GP506 -I/MR® 1310017

64-Lead TQFP (10x10x1 mm)



Example



© 2011-2013 Microchip Technology Inc.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



## RECOMMENDED LAND PATTERN

	Units	nits MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	Е	1.27 BSC		
Contact Pad Spacing	С		9.40	
Contact Pad Width (X28)	Х			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



#### **RECOMMENDED LAND PATTERN**

	Units	its MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	nits MILLIMETERS			
Dimension Limits		MIN	NOM	MAX	
Contact Pitch	E		0.50 BSC		
Contact Pad Spacing	C1		11.40		
Contact Pad Spacing	C2		11.40		
Contact Pad Width (X64)	X1			0.30	
Contact Pad Length (X64)	Y1			1.50	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

#### Note the following details of the code protection feature on Microchip devices:

- · Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

## QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV == ISO/TS 16949 ==

#### Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC<sup>32</sup> logo, rfPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rfLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2011-2013, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN: 9781620773949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEEL0Q® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and mulfacture of development systems is ISO 9001:2000 certified.