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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Ξ·ΧΕΙ

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	·
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128mc506-e-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

Pin Diagrams



Pin Diagrams (Continued)



File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Reset
IFS0	0800		DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	_	_	_	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804		_	—	_	_	_	_	_	_	IC4IF	IC3IF	DMA3IF	_	_	SPI2IF	SPI2EIF	0000
IFS3	0806	_	_	—	_	_	QEI1IF	PSEMIF	_	_	_	_	_	_	MI2C2IF	SI2C2IF	—	0000
IFS4	0808		_	CTMUIF	_	—	_	—	_	_	_	_	_	CRCIF	U2EIF	U1EIF		0000
IFS5	080A	PWM2IF	PWM1IF	—	_	—	_	_	_	_	_	_	_	_	_	—		0000
IFS6	080C	_	_	_	_	—	—	—	_	_	_	_	_	_	_	_	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	_	_	—	—	—	_	_	_	_	_	_	_	_		0000
IFS9	0812		_	_	_	—	_	_	_	_	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF		0000
IEC0	0820		DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	_	_	_	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824		_	—	_	_	_	_	_	_	IC4IE	IC3IE	DMA3IE	_	_	SPI2IE	SPI2EIE	0000
IEC3	0826		_	_	_	_	QEI1IE	PSEMIE	_	_	_	_	_	_	MI2C2IE	SI2C2IE	—	0000
IEC4	0828		_	CTMUIE	_	_	_	_	_	_	_	_	_	CRCIE	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	—	_	_	_	_	_	_	_	_	_	_	_	_	—	0000
IEC6	082C		_	—	_	_	_	_	_	_	_	_	_	_	_	_	PWM3IE	0000
IEC8	0830	JTAGIE	ICDIE	—	_	_	_	_	_	_	_	_	_	_	_	_	—	0000
IEC9	0832		_	—	_	_	_	_	_	_	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	—	0000
IPC0	0840			T1IP<2:0>	`	_		OC1IP<2:0)>	_		IC1IP<2:0>		_		INT0IP<2:0>		4444
IPC1	0842			T2IP<2:0>	•	_		OC2IP<2:0)>	_		IC2IP<2:0>		_	[OMA0IP<2:0>		4444
IPC2	0844			U1RXIP<2:	0>	_		SPI1IP<2:0)>	_		SPI1EIP<2:0	>	_		T3IP<2:0>		4444
IPC3	0846	_	_	_	_	_	C	DMA1IP<2:	0>	_		AD1IP<2:0>	,	_		J1TXIP<2:0>		0444
IPC4	0848	_		CNIP<2:0	>	_		CMIP<2:0	>	_		MI2C1IP<2:0	>	_	9	SI2C1IP<2:0>		4444
IPC5	084A	_	_	_	_	_	_	_	_	_	_	_	_	_		INT1IP<2:0>		0004
IPC6	084C	_		T4IP<2:0>	, ,	_		OC4IP<2:0)>	_		OC3IP<2:0>	>	_	[DMA2IP<2:0>		4444
IPC7	084E	_		U2TXIP<2:0)>	_	ι	J2RXIP<2:	0>	_		INT2IP<2:0	>	_		T5IP<2:0>		4444
IPC8	0850		_	_	_	_	(C1RXIP<2:	0>	_		SPI2IP<2:0	>	_	5	SPI2EIP<2:0>		0444
IPC9	0852		_	_	_	_		IC4IP<2:0	>	_		IC3IP<2:0>		_	[DMA3IP<2:0>		0444
IPC12	0858		_	_	_	_	N	/II2C2IP<2:	:0>	_		SI2C2IP<2:0	>	_	_	_	_	0440
IPC14	085C		_	_	_	_		QEI1IP<2:)>	_		PSEMIP<2:0	>	_	_	_	_	0440
IPC16	0860	_		CRCIP<2:0)>	_		U2EIP<2:0)>	_		U1EIP<2:0>	>	_	_	_	_	4440
IPC19	0866	_	_	—	_	_	_		_	_		CTMUIP<2:0	>	_	_	_		0040
IPC23	086E	_		PWM2IP<2:	0>	_	F	WM1IP<2	:0>	_	_	_	_	_	_	_	_	4400
IPC24	0870	_	_	_	_	_	<u> </u>	_	_	_	_	_	_	_	F	WM3IP<2:0>		0004

TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY

TABLE 4-24: CRC REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON1	0640	CRCEN	—	CSIDL		VWORD<4:0>			CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	-	—	0000	
CRCCON2	0642	_	DWIDTH<4:0> PLEN<4:0> (0000						
CRCXORL	0644		X<15:1> 001									0000						
CRCXORH	0646		X<31:16> 00									0000						
CRCDATL	0648								CRC Data	Input Low V	Vord							0000
CRCDATH	064A		CRC Data Input High Word 000									0000						
CRCWDATL	064C		CRC Result Low Word 000								0000							
CRCWDATH	064E		CRC Result High Word 0000								0000							

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

TABLE 4-25: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC202/502 AND PIC24EPXXXGP/MC202 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	_	—		RP35R<5:0>					—	—			RP20F	R<5:0>			0000
RPOR1	0682	_	_		RP37R<5:0>					—	_	RP36R<5:0> 0						0000
RPOR2	0684	_	_		RP39R<5:0>					—	_	RP38R<5:0>					0000	
RPOR3	0686	_	_		RP41R<5:0>					—	_	RP40R<5:0>					0000	
RPOR4	0688	_	—	RP43R<5:0>				_	_	RP42R<5:0>				0000				

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC203/503 AND PIC24EPXXXGP/MC203 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	_		RP35R<5:0> — — RP					RP20	R<5:0>			0000				
RPOR1	0682	_	_			RP37	२<5:0>			_	_			RP36	२<5:0>			0000
RPOR2	0684	_	_			RP39	२<5:0>			_	_			RP38	२<5:0>			0000
RPOR3	0686	_	_			RP41	२<5:0>			_	_			RP40	२<5:0>			0000
RPOR4	0688	_	_			RP43	२<5:0>			_	_	RP42R<5:0>				0000		
RPOR5	068A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
RPOR6	068C			-	—	_		—			_			RP56	R<5:0>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



EXAMPLE 4-2: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION

The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS only. The Data Space and EDS can be read from, and written to, using DSRPAG and DSWPAG, respectively.



TABLE 4-64: BIT-REVERSED ADDRESSING SEQUENCE (16-ENTRY)

		Norma	al Addre	SS	Bit-Reversed Address							
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal			
0	0	0	0	0	0	0	0	0	0			
0	0	0	1	1	1	0	0	0	8			
0	0	1	0	2	0	1	0	0	4			
0	0	1	1	3	1	1	0	0	12			
0	1	0	0	4	0	0	1	0	2			
0	1	0	1	5	1	0	1	0	10			
0	1	1	0	6	0	1	1	0	6			
0	1	1	1	7	1	1	1	0	14			
1	0	0	0	8	0	0	0	1	1			
1	0	0	1	9	1	0	0	1	9			
1	0	1	0	10	0	1	0	1	5			
1	0	1	1	11	1	1	0	1	13			
1	1	0	0	12	0	0	1	1	3			
1	1	0	1	13	1	0	1	1	11			
1	1	1	0	14	0	1	1	1	7			
1	1	1	1	15	1	1	1	1	15			

7.0 INTERRUPT CONTROLLER

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP/MC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Interrupts" (DS70600) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 246 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit-wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See the **"Pin Diagrams"** section for the available 5V tolerant pins and Table 30-11 for the maximum VIH specification for each pin.

11.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP, as shown in Example 11-1.

11.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the Change Notification (CN) functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pulldowns act as a current source or sink source connected to the pin and eliminate the need for external resistors when push button, or keypad devices are connected. The pull-ups and pull-downs are enabled separately, using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note:	Pull-ups and pull-downs on Change Noti-
	fication pins should always be disabled
	when the port pin is configured as a digital
	output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

MOV	0xFF00, W0	; Configure PORTB<15:8>
		; as inputs
MOV	W0, TRISB	; and PORTB<7:0>
		; as outputs
NOP		; Delay 1 cycle
BTSS	PORTB, #13	; Next Instruction

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U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				U1RXR<6:0	>		
bit 7							bit 0
-							

REGISTER 11-10: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 Unimplemented: Read as '0' bit 6-0 U1RXR<6:0>: Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121

REGISTER 11-11: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_		_	—	_	—	_
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				U2RXR<6:0>	>		
bit 7							bit 0
Legend:							

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 Unimplemented: Read as '0'

^{0000000 =} Input tied to Vss

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	TRGDI	V<3:0>		—	—	—	—
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			TRGSTF	RT<5:0>(1)		
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own
bit 15-12	TRGDIV<3:0)>: Trigger # Ou	tput Divider b	vits			
	1111 = Trigg	er output for ev	ery 16th trigg	er event			
	1110 = Trigg	er output for ev	ery 15th trigg	er event			
	1101 = Trigg	er output for ev	ery 14th trigg	er event			
	1100 = Trigg	er output for ev	ery 13th trigg	er event			
	1011 = Irigg	er output for ev	ery 12th trigg	er event			
	1010 = Trigg	per output for ev	ery 11th trigge	er event			
	1001 - Trigg	er output for ev	ery 9th triage	r event			
	0111 = Trigg	er output for ev	erv 8th triage	r event			
	0110 = Trigg	er output for ev	erv 7th triage	r event			
	0101 = Trigg	er output for ev	ery 6th trigge	r event			
	0100 = Trigg	, jer output for ev	ery 5th trigge	r event			
	0011 = Trigg	er output for ev	ery 4th trigge	r event			
	0010 = Trigg	er output for ev	ery 3rd trigge	r event			
	0001 = Trigg	er output for ev	ery 2nd trigge	erevent			
	0000 = Trigg	ger output for ev	ery trigger ev	ent			
bit 11-6	Unimplemer	nted: Read as '	0'				
bit 5-0	TRGSTRT<5	5:0>: Trigger Po	stscaler Start	Enable Select	bits ⁽¹⁾		
	111111 = W	aits 63 PWM cy	cles before g	enerating the fir	rst trigger event	after the modu	le is enabled
	•						
	•						
	•						
	000010 = W	aits 2 PWM cyc	les before ge	nerating the firs	t trigger event a	after the module	e is enabled
	000001 = W	aits 1 PWM cyc	le before gen	erating the first	trigger event a	fter the module	is enabled
	000000 = W	aits 0 PWM cyc	les before ge	nerating the firs	t trigger event a	after the module	e is enabled

REGISTER 16-12: TRGCONx: PWMx TRIGGER CONTROL REGISTER



dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 17-13: QEI1LECH: QEI1 LESS THAN OR EQUAL COMPARE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILE	C<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILE	C<23:16>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable bi	t	U = Unimplen	nented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown

bit 15-0 **QEILEC<31:16>:** High Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

REGISTER 17-14: QEI1LECL: QEI1 LESS THAN OR EQUAL COMPARE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILE	C<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILI	EC<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
~							

bit 15-0 QEILEC<15:0>: Low Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

18.1 SPI Helpful Tips

- 1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
 - a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on SSx.
 - b) If FRMPOL = 0, use a pull-up resistor on $\frac{1}{SSx}$.

Note:	This	insures	that	the	first	fra	ame
	transn	nission	after	initializ	ation	is	not
	shifted	d or corru	upted.				

- 2. In Non-Framed 3-Wire mode, (i.e., not using SSx from a master):
 - a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on SSx.
 - b) If CKP = 0, always place a pull-down resistor on SSx.
 - **Note:** This will insure that during power-up and initialization the master/slave will not lose Sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.
- FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the SSx pin, which indicates the start of a data frame.
 - Note: Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in Section 30.0 "Electrical Characteristics" for details.
- In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPIx data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

18.2.1 KEY RESOURCES

- "Serial Peripheral Interface (SPI)" (DS70569) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

21.2 Modes of Operation

The ECAN module can operate in one of several operation modes selected by the user. These modes include:

- · Initialization mode
- Disable mode
- Normal Operation mode
- · Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

21.3 ECAN Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

21.3.1 KEY RESOURCES

- "Enhanced Controller Area Network (ECAN™)" (DS70353) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- · Development Tools

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8
bit 15							bit 8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
bit 7							bit 0
Legend:							

REGISTER 21-11: CxFEN1: ECANx ACCEPTANCE FILTER ENABLE REGISTER 1

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0

FLTEN<15:0>: Enable Filter n to Accept Messages bits

1 = Enables Filter n

0 = Disables Filter n

REGISTER 21-12: CxBUFPNT1: ECANx FILTER 0-3 BUFFER POINTER REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	F3BF	P<3:0>			F2B	P<3:0>	
bit 15				·			bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F1BP<3:0>					F0B	P<3:0>	
bit 7							bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimpler	nented bit, rea	ıd as '0'	
-n = Value at	POR	'1' = Bit is set	t	'0' = Bit is cle	ared	x = Bit is unki	nown
bit 15-12	F3BP<3:0>:	RX Buffer Mas	k for Filter 3 I	oits			
	1111 = Filte	r hits received in	n RX FIFO bu	uffer			
	1110 = Filte	r hits received in	n RX Buffer 1	4			
	•						
	•						
		r hito roccivad i	DV Duffer 1				
		r hits received in		1			
hit 11 0	E3DD -2:0		k for Filtor 2 l	, hito (como voluc	a aa hita <1 E 1	22)	
	F2BF<3:0>			oits (same value		Z ²)	
bit 7-4	F1BP<3:0>:	RX Buffer Mas	k for Filter 1 I	bits (same value	es as bits<15:1	2>)	
bit 3-0	F0BP<3:0>:	RX Buffer Mas	k for Filter 0 I	bits (same value	es as bits<15:1	2>)	

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-19: CxFMSKSEL2: ECANx FILTER 15-8 MASK SELECTION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F15M	F15MSK<1:0> F14MSK<1:0> F13MSK		SK<1:0>	F12MS	K<1:0>			
bit 15							bit 8	
	D 444 0	Date	D M (0	D 444 0	D 444 0	D 444 0	D 444 0	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F11M	SK<1:0>	F10MS	K<1:0>	F9MS	K<1:0>	F8MS	K<1:0>	
bit 7							bit 0	
Legend:								
R = Readabl	e bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared x		x = Bit is unkr	x = Bit is unknown	
bit 15-14	F15MSK<1: 11 = Reserv 10 = Accept 01 = Accept 00 = Accept	0>: Mask Sourc ed ance Mask 2 reg ance Mask 1 reg ance Mask 0 reg	e for Filter 15 gisters contair gisters contair gisters contair	bits n mask n mask n mask				
bit 13-12	F14MSK<1:	0>: Mask Sourc	e for Filter 14	bits (same valu	ues as bits<15:	14>)		
bit 11-10	F13MSK<1:	0>: Mask Sourc	e for Filter 13	bits (same valu	ues as bits<15:	14>)		
bit 9-8	F12MSK<1:0>: Mask Source for Filter 12 bits (same values as bits<15:14>)							
bit 7-6	F11MSK<1:0>: Mask Source for Filter 11 bits (same values as bits<15:14>)							
bit 5-4	F10MSK<1:	F10MSK<1:0>: Mask Source for Filter 10 bits (same values as bits<15:14>)						
bit 3-2	F9MSK<1:0	>: Mask Source	for Filter 9 bit	ts (same values	s as bits<15:14	>)		
bit 1-0	F8MSK<1:0	>: Mask Source	for Filter 8 bit	ts (same values	s as bits<15:14	>)		

AC CHARACTERISTICS			Standard Oper (unless otherw Operating temp	ating Co vise stat perature	onditions: 3.0V ed) -40°C ≤ TA ≤ + -40°C ≤ TA ≤ +	to 3.6V -85°C foi -125°C fo	r Industrial pr Extended	
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Тур.	Max.	Units	Conditions
ТВ10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or (TcY + 20)/N		_	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N		_	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from Clock Edge Increment	External TxCK to Timer	0.75 Tcy + 40		1.75 Tcy + 40	ns	

TABLE 30-24:	TIMER2 AND TI	MER4 (TYPE B TIM	ER) EXTERNAL CLOC	K TIMING REQUIREMENTS
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Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Charac	teristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions	
TC10	TtxH	TxCK High Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15	
TC11	TtxL	TxCK Low Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15	
TC15	TtxP	TxCK Input Period	Synchronous, with prescaler	2 Tcy + 40	—	_	ns	N = prescale value (1, 8, 64, 256)	
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

AC CHARA	CTERISTICS		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	СКЕ	СКР	SMP		
15 MHz	Table 30-33		_	0,1	0,1	0,1		
9 MHz	—	Table 30-34	—	1	0,1	1		
9 MHz	—	Table 30-35	—	0	0,1	1		
15 MHz	—	—	Table 30-36	1	0	0		
11 MHz	—	—	Table 30-37	1	1	0		
15 MHz		_	Table 30-38	0	1	0		
11 MHz	_	_	Table 30-39	0	0	0		

TABLE 30-33: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY

FIGURE 30-14: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



АС СНА	RACTERI	STICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param. No.	Symbol	Characte	eristic ⁽³⁾	Min.	Max.	Units	Conditions	
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7		μS		
			400 kHz mode	1.3	_	μS		
			1 MHz mode ⁽¹⁾	0.5	—	μS		
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	-	μS	Device must operate at a minimum of 1.5 MHz	
			400 kHz mode	0.6	—	μS	Device must operate at a minimum of 10 MHz	
			1 MHz mode ⁽¹⁾	0.5		μS		
IS20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be from	
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode ⁽¹⁾	—	100	ns		
IS21	TR:SCL	SDAx and SCLx	100 kHz mode	—	1000	ns	CB is specified to be from	
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode ⁽¹⁾	—	300	ns		
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250		ns		
			400 kHz mode	100		ns		
			1 MHz mode ⁽¹⁾	100		ns		
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0		μS		
			400 kHz mode	0	0.9	μS		
			1 MHz mode ⁽¹⁾	0	0.3	μS		
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7		μS	Only relevant for Repeated	
			400 kHz mode	0.6		μS	Start condition	
			1 MHz mode ⁽¹⁾	0.25	—	μS		
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	μS	After this period, the first	
			400 kHz mode	0.6	—	μS	clock pulse is generated	
			1 MHz mode ⁽¹⁾	0.25	—	μS		
IS33	TSU:STO	Stop Condition	100 kHz mode	4.7	—	μS		
		Setup Time	400 kHz mode	0.6	—	μS		
			1 MHz mode ⁽¹⁾	0.6	—	μS		
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4	—	μS		
			400 kHz mode	0.6	—	μS		
			1 MHz mode ⁽¹⁾	0.25		μS		
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns		
			400 kHz mode	0	1000	ns		
			1 MHz mode ⁽¹⁾	0	350	ns		
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μS	Time the bus must be free	
			400 kHz mode	1.3	—	μS	perore a new transmission	
	<u> </u>		1 MHz mode ⁽¹⁾	0.5	—	μS	Call Stall	
IS50	Св	Bus Capacitive Lo	bading	—	400	pF		
IS51	TPGD	Pulse Gobbler De	65	390	ns	(Note 2)		

TABLE 30-50: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: Typical value for this parameter is 130 ns.

3: These parameters are characterized, but not tested in manufacturing.

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)}^{(1)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions		
		Clock	k Paramet	ters					
AD50	TAD	ADC Clock Period	117.6	_	_	ns			
AD51	tRC	ADC Internal RC Oscillator Period ⁽²⁾		250		ns			
	Conversion Rate								
AD55	tCONV	Conversion Time		14 Tad		ns			
AD56	FCNV	Throughput Rate	_		500	ksps			
AD57a	TSAMP	Sample Time when Sampling any ANx Input	3 Tad	_	—	_			
AD57b	TSAMP	Sample Time when Sampling the Op Amp Outputs (Configuration A and Configuration B) ^(4,5)	3 Tad	—	_				
		Timin	g Parame	ters					
AD60	tPCS	Conversion Start from Sample Trigger ^(2,3)	2 Tad		3 Tad	_	Auto-convert trigger is not selected		
AD61	tpss	Sample Start from Setting Sample (SAMP) bit ^(2,3)	2 Tad	—	3 Tad	_			
AD62	tcss	Conversion Completion to Sample Start (ASAM = 1) ^(2,3)		0.5 TAD	1	_			
AD63	tdpu	Time to Stabilize Analog Stage from ADC Off to ADC On ^(2,3)			20	μs	(Note 6)		

TABLE 30-60: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: Parameters are characterized but not tested in manufacturing.
- **3:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.
- 4: See Figure 25-6 for configuration information.
- 5: See Figure 25-7 for configuration information.
- **6:** The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1<15>) = 1). During this time, the ADC result is indeterminate.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Microchip Tradema Architecture — Flash Memory Fam Program Memory S Product Group — Pin Count — Tape and Reel Flag Temperature Range Package Pattern	rk ily ize (Kb (if app	dsPI	C 33 EP 64 MC5 04 T 1/PT - XXX	Examples: dsPIC33EP64MC504-I/PT: dsPIC33, Enhanced Performance, 64-Kbyte Program Memory, Motor Control, 44-Pin, Industrial Temperature, TQFP package.
Architecture:	33 24	= =	16-bit Digital Signal Controller 16-bit Microcontroller	
Flash Memory Family:	EP	=	Enhanced Performance	
Product Group:	GP MC	= =	General Purpose family Motor Control family	
Pin Count:	02 03 04 06	= = =	28-pin 36-pin 44-pin 64-pin	
Temperature Range:	l E	= =	-40°C to+85°C (Industrial) -40°C to+125°C (Extended)	
Package:	ML MR MV PT SO SP SS TL TL		Plastic Quad, No Lead Package - (44-pin) 8x8 mm body (QFN) Plastic Quad, No Lead Package - (28-pin) 6x6 mm body (QFN-S) Plastic Quad, No Lead Package - (64-pin) 9x9 mm body (QFN) Thin Quad, No Lead Package - (64-pin) 9x9 mm body (UQFN) Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) Plastic Small Outline, Wide - (28-pin) 7.50 mm body (SOIC) Skinny Plastic Dual In-Line - (28-pin) 300 mil body (SPDIP) Plastic Shrink Small Outline - (28-pin) 5.30 mm body (SOP) Very Thin Leadless Array - (36-pin) 5x5 mm body (VTLA) Very Thin Leadless Array - (44-pin) 6x6 mm body (VTLA)	