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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gp502-e-so

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2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS AND MICROCONTROLLERS

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Familv Reference Manual", which is available from the Microchip web site (www.microchip.com)
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and Vss pins (see Section 2.2 "Decoupling Capacitors")
- All AVDD and AVss pins (regardless if ADC module is not used)

(see Section 2.2 "Decoupling Capacitors")
• VCAP

(see Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)")

- MCLR pin (see Section 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins used for In-Circuit Serial Programming[™] (ICSP[™]) and debugging purposes (see **Section 2.5 "ICSP Pins**")
- OSC1 and OSC2 pins when external oscillator source is used

(see Section 2.6 "External Oscillator Pins")

Additionally, the following pins may be required:

• VREF+/VREF- pins are used when external voltage reference for the ADC module is implemented

Note: The AVDD and AVSS pins must be connected, independent of the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: Recommendation of 0.1 μ F (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- Handling high-frequency noise: If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μ F to 0.001 μ F. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μ F in parallel with 0.001 μ F.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

FIGURE 3-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X CPU BLOCK DIAGRAM







SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100								Timer1	Register								xxxx
PR1	0102	Period Register 1 FF										FFFF						
T1CON	0104	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKP	S<1:0>	_	TSYNC	TCS	—	0000
TMR2	0106		Timer2 Register									xxxx						
TMR3HLD	0108	Timer3 Holding Register (for 32-bit timer operations only)									xxxx							
TMR3	010A								Timer3	Register								xxxx
PR2	010C	Period Register 2									FFFF							
PR3	010E								Period F	Register 3								FFFF
T2CON	0110	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKP	S<1:0>	T32	_	TCS	—	0000
T3CON	0112	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKP	S<1:0>	_	_	TCS	—	0000
TMR4	0114								Timer4	Register								xxxx
TMR5HLD	0116						Т	imer5 Holdii	ng Register	(for 32-bit o	perations on	ly)						xxxx
TMR5	0118								Timer5	Register								xxxx
PR4	011A								Period F	Register 4								FFFF
PR5	011C								Period F	Register 5								FFFF
T4CON	011E	TON	_	TSIDL	_	—	—	_	_	_	TGATE	TCKP	S<1:0>	T32	—	TCS	—	0000
T5CON	0120	TON		TSIDL	—	—	—	_	_	_	TGATE	TCKP	S<1:0>	—	_	TCS	—	0000

TABLE 4-8: TIMER1 THROUGH TIMER5 REGISTER MAP

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TADLL 4-2		LUANT	IL GIGI				ICINE	1<02) -	· • • • • .	I I OK US			IC/GFJ					
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	_	—	CSIDL	ABAT	CANCKS	R	EQOP<2:0)>	OPN	NODE<2:0	>	_	CANCAP	_	_	WIN	0480
C1CTRL2	0402	_	—	_	—	—	—	_	_	_	—	_		D	NCNT<4:0	>		0000
C1VEC	0404	_	_	_		F	ILHIT<4:0>			_				ICODE<6:0	>			0040
C1FCTRL	0406	[DMABS<2:0	>	—	—		—	_	_	—	—			FSA<4:0>			0000
C1FIFO	0408	_	_			FBP<	5:0>			— — FNRB<5:0>					0000			
C1INTF	040A	_	_	ТХВО	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	_	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	_	_	_	—	—	_	_	_	IVRIE	WAKIE	ERRIE	_	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E				TERRCN	T<7:0>				RERRCNT<7:0>							0000	
C1CFG1	0410	_	_	_	—	—	_	_	_	SJW<	1:0>			BRP	<5:0>			0000
C1CFG2	0412	_	WAKFIL	_	—	—	SI	EG2PH<2:(0>	SEG2PHTS	SAM	S	EG1PH<2	::0>	P	RSEG<2:0	>	0000
C1FEN1	0414	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C1FMSKSEL1	0418	F7MS	K<1:0>	F6MS	K<1:0>	F5MS	K<1:0>	F4MS	K<1:0>	F3MSK	<1:0>	F2MS	K<1:0>	F1MSł	<<1:0>	F0MS	<<1:0>	0000
C1FMSKSEL2	041A	F15MS	SK<1:0>	F14MS	K<1:0>	F13MS	SK<1:0>	F12MS	SK<1:0>	F11MSK	<1:0>	F10MS	K<1:0>	F9MSł	<<1:0>	F8MS	< <1:0>	0000

TABLE 4-21: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 0 OR 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 0 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400- 041E	See definition when WIN = x																
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C1RXOVF2	042A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PF	RI<1:0>	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PF	RI<1:0>	0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PF	RI<1:0>	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PF	RI<1:0>	0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PF	RI<1:0>	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PF	RI<1:0>	0000
C1TR67CON	0436	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	7 TX7PRI<1:0>		TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PF	RI<1:0>	xxxx
C1RXD	0440	ECAN1 Receive Data Word xx									xxxx							
C1TXD	0442							E	CAN1 Trans	smit Data W	ord							xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.5.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions. which apply to dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and the DSP accumulator class of instructions, which apply to the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.5.4 MAC INSTRUCTIONS (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X DEVICES ONLY)

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY. N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The Two-Source Operand Prefetch registers must be members of the set: {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the ${\tt MAC}$ class of instructions:

- · Register Indirect
- Register Indirect Post-Modified by 2
- · Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.5.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See the **"Pin Diagrams"** section for the available 5V tolerant pins and Table 30-11 for the maximum VIH specification for each pin.

11.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP, as shown in Example 11-1.

11.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the Change Notification (CN) functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pulldowns act as a current source or sink source connected to the pin and eliminate the need for external resistors when push button, or keypad devices are connected. The pull-ups and pull-downs are enabled separately, using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note:	Pull-ups and pull-downs on Change Noti-
	fication pins should always be disabled
	when the port pin is configured as a digital
	output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

MOV	0xFF00, W0	; Configure PORTB<15:8>
		; as inputs
MOV	W0, TRISB	; and PORTB<7:0>
		; as outputs
NOP		; Delay 1 cycle
BTSS	PORTB, #13	; Next Instruction

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				IC2R<6:0>			
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				IC1R<6:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	Unimplemen	ted: Read as '	0'				
bit 14-8	IC2R<6:0>: A (see Table 11	Assign Input Ca -2 for input pin	pture 2 (IC2) selection nur	to the Correspondent	onding RPn P	in bits	
	1111001 = I r	nput tied to RPI	121				
	•						
	0000001 = lr	nput tied to CM	P1				
	nl = 0000000	nput tied to Vss	;				
bit 7	Unimplemen	ted: Read as '	0'				
bit 6-0	IC1R<6:0>: A (see Table 11	Assign Input Ca -2 for input pin	pture 1 (IC1) selection nur	to the Correspondence	onding RPn P	in bits	
	1111001 = I r	nput tied to RPI	121				
	•						
	•						
	0000001 = lr	nput tied to CM	P1				
	0000000 = Ir	nput tied to Vss	;				

REGISTER 11-4: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

14.1 Input Capture Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

14.1.1 KEY RESOURCES

- "Input Capture" (DS70352) in the "dsPIC33/ PIC24 Family Reference Manual"
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5	 ADDEN: Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect 0 = Address Detect mode is disabled
bit 4	RIDLE: Receiver Idle bit (read-only) 1 = Receiver is Idle 0 = Receiver is active
bit 3	PERR: Parity Error Status bit (read-only) 1 = Parity error has been detected for the current character (character at the top of the receive FIFO) 0 = Parity error has not been detected
bit 2	<pre>FERR: Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character (character at the top of the receive FIFO) 0 = Framing error has not been detected</pre>
bit 1	 OERR: Receive Buffer Overrun Error Status bit (clear/read-only) 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receiver buffer and the UxRSR to the empty state
bit 0	 URXDA: UARTx Receive Buffer Data Available bit (read-only) 1 = Receive buffer has data, at least one more character can be read 0 = Receive buffer is empty

Note 1: Refer to the **"UART"** (DS70582) section in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER (CONTINUED)

- bit 1 **RBIF:** RX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 **TBIF:** TX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred

23.4 ADC Control Registers

REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0
bit 15						-	bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC, HS	R/C-0, HC, HS
SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE ⁽³⁾
bit 7						-	bit 0
Legend:		HC = Hardwa	re Clearable bit	HS = Hardwa	re Settable bit	C = Clearable bi	t
R = Readab	le bit	W = Writable I	bit	U = Unimpler	nented bit, read	d as '0'	
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknow	vn
bit 15	ADON: ADO	C1 Operating N	lode bit				
	1 = ADC mo	odule is operati	ng				
	0 = ADC is	off					
bit 14	Unimpleme	ented: Read as	'0'				
bit 13	ADSIDL: AI	DC1 Stop in Idle	e Mode bit				
	1 = Disconti	inues module o	peration when	device enters	Idle mode		
	0 = Continu	es module ope	ration in Idle mo	ode			
bit 12	ADDMABM	: DMA Buffer E	Build Mode bit				
	1 = DMA b	uffers are writte	en in the order	of conversion	; the module p	provides an addre	ess to the DMA
	0 = DMA bi	uffers are writte	en in Scatter/Ga	ther mode: the	e module prov	ides a Scatter/Ga	ther address to
	the DM	A channel, bas	ed on the index	of the analog	input and the	size of the DMA	ouffer.
bit 11	Unimpleme	ented: Read as	'0'				
bit 10	AD12B: AD	C1 10-Bit or 12	2-Bit Operation	Mode bit			
	1 = 12-bit, 1	-channel ADC	operation				
	0 = 10-bit, 4	-channel ADC	operation				
bit 9-8	FORM<1:0	>: Data Output	Format bits				
	For 10-Bit C	Operation:					
	11 = Signed	d fractional (Do	UT = sddd ddd	ld dd00 000	0, where $s = $.	NOT.d<9>)	
	10 = Fractions	hai (DOUT = ac	100 0000 000 = cccc cccd		where $c = N($	(<0>b T(
	00 = Intege	r (Dout = 0000	00dd dddd	dddd)		51.u (0 ²)	
	For 12-Bit C	Deration:		,			
	11 = Signed	fractional (Do	UT = sddd ddd	ld dddd 000	0, where $s = .$	NOT.d<11>)	
	10 = Fractic	onal (Dout = do	ldd dddd ddd	ld 0000)			
	00 = Intege	r (DOUT = 0.000)	- ssss sada) dddd dddd	aaaa aaad, dddd)	where $s = .NC$	JI.U<112)	
		. (2001 - 0000		adduj			
Note 1: S	See Section 24	1.0 "Peripheral	l Trigger Gene	rator (PTG) M	odule" for info	ormation on this s	election.

- 2: This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 3: Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

Bit Field	Description
WDTPRE	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST<3:0>	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • • • • • • • • • • •
WDTWIN<1:0>	Watchdog Window Select bits 11 = WDT window is 25% of WDT period 10 = WDT window is 37.5% of WDT period 01 = WDT window is 50% of WDT period 00 = WDT window is 75% of WDT period
ALTI2C1	Alternate I2C1 pin 1 = I2C1 is mapped to the SDA1/SCL1 pins 0 = I2C1 is mapped to the ASDA1/ASCL1 pins
ALTI2C2	Alternate I2C2 pin 1 = I2C2 is mapped to the SDA2/SCL2 pins 0 = I2C2 is mapped to the ASDA2/ASCL2 pins
JTAGEN ⁽²⁾	JTAG Enable bit 1 = JTAG is enabled 0 = JTAG is disabled
ICS<1:0>	ICD Communication Channel Select bits 11 = Communicate on PGEC1 and PGED1 10 = Communicate on PGEC2 and PGED2 01 = Communicate on PGEC3 and PGED3 00 = Reserved, do not use

TABLE 27-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

DC CHARACT	ERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended						
Parameter No.	Тур.	Max.	Units		Conditions				
Operating Cur	rent (IDD) ⁽¹⁾								
DC20d	9	15	mA	-40°C					
DC20a	9	15	mA	+25°C	3 3\/				
DC20b	9	15	mA	+85°C	3.5 V	10 1011-5			
DC20c	9	15	mA	+125°C					
DC22d	16	25	mA	-40°C					
DC22a	16	25	mA	+25°C	2 2)/				
DC22b	16	25	mA	+85°C	3.3V	20 101175			
DC22c	16	25	mA	+125°C					
DC24d	27	40	mA	-40°C					
DC24a	27	40	mA	+25°C	2 2)/				
DC24b	27	40	mA	+85°C	3.3V	40 101175			
DC24c	27	40	mA	+125°C					
DC25d	36	55	mA	-40°C					
DC25a	36	55	mA	+25°C	2.21/				
DC25b	36	55	mA	+85°C	3.3V	60 MIPS			
DC25c	36	55	mA	+125°C					
DC26d	41	60	mA	-40°C					
DC26a	41	60	mA	+25°C	3.3V 70 MIPS				
DC26b	41	60	mA	+85°C					

TABLE 30-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

• Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration Word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing while(1) {NOP(); } statement
- · JTAG is disabled

DC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic	Min.	Min. Typ. Max. Units Conditions				
	VIL	Input Low Voltage						
DI10		Any I/O Pin and MCLR	Vss	—	0.2 VDD	V		
DI18		I/O Pins with SDAx, SCLx	Vss	_	0.3 VDD	V	SMBus disabled	
DI19		I/O Pins with SDAx, SCLx	Vss	—	0.8	V	SMBus enabled	
	Vih	Input High Voltage						
DI20		I/O Pins Not 5V Tolerant	0.8 VDD	—	Vdd	V	(Note 3)	
		I/O Pins 5V Tolerant and MCLR	0.8 VDD	—	5.5	V	(Note 3)	
		I/O Pins with SDAx, SCLx	0.8 VDD	—	5.5	V	SMBus disabled	
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled	
	ICNPU	Change Notification Pull-up Current						
DI30			150	250	550	μA	VDD = 3.3V, VPIN = VSS	
	ICNPD	Change Notification Pull-Down Current ⁽⁴⁾						
DI31			20	50	100	μA	VDD = 3.3V, VPIN = VDD	

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (VSS 0.3). Characterized but not tested.

5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

TABLE 30-37:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	-	—	Lesser of FP or 15	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)
SP60	TssL2doV	SDO2 Data Output Valid after SS2 Edge	-	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions	
		ADC /	Accuracy	/ (12-Bit	Mode)			
AD20a	Nr	Resolution	12 Data Bits		bits			
AD21a	INL	Integral Nonlinearity	-2.5		2.5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)	
			-5.5		5.5	LSb	+85°C < TA \leq +125°C (Note 2)	
AD22a	DNL	Differential Nonlinearity	-1		1	LSb	-40°C \leq TA \leq +85°C (Note 2)	
			-1		1	LSb	+85°C < TA \leq +125°C (Note 2)	
AD23a	Gerr	Gain Error ⁽³⁾	-10		10	LSb	-40°C \leq TA \leq +85°C (Note 2)	
			-10		10	LSb	+85°C < TA \leq +125°C (Note 2)	
AD24a	EOFF	Offset Error	-5		5	LSb	$-40^{\circ}C \le TA \le +85^{\circ}C$ (Note 2)	
			-5		5	LSb	+85°C < TA \leq +125°C (Note 2)	
AD25a	—	Monotonicity	—			—	Guaranteed	
Dynamic Performance (12-Bit Mode)								
AD30a	THD	Total Harmonic Distortion ⁽³⁾	—	75		dB		
AD31a	SINAD	Signal to Noise and Distortion ⁽³⁾		68	-	dB		
AD32a	SFDR	Spurious Free Dynamic Range ⁽³⁾	_	80	_	dB		
AD33a	Fnyq	Input Signal Bandwidth ⁽³⁾	_	250		kHz		
AD34a	ENOB	Effective Number of Bits ⁽³⁾	11.09	11.3	_	bits		

TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.



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28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Contact Pitch	E	0.65 BSC			
Contact Pad Spacing	С		7.20		
Contact Pad Width (X28)				0.45	
Contact Pad Length (X28)	Y1			1.75	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A