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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gp502-e-ss">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gp502-e-ss</a>

## 2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V<sub>IH</sub>) and Voltage Input Low (V<sub>IL</sub>) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICKit™ 3, MPLAB ICD 3, or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

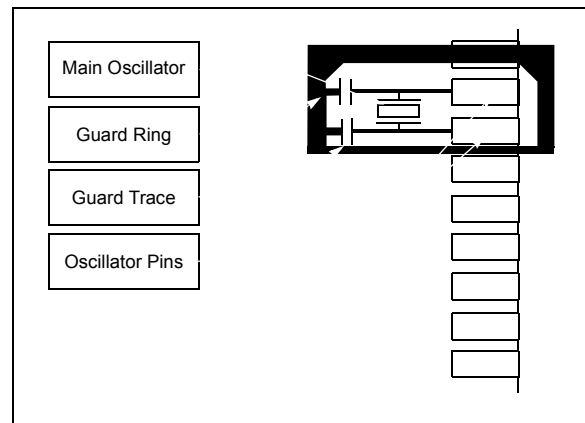
- "Using MPLAB® ICD 3" (poster) DS51765
- "MPLAB® ICD 3 Design Advisory" DS51764
- "MPLAB® REAL ICE™ In-Circuit Emulator User's Guide" DS51616
- "Using MPLAB® REAL ICE™ In-Circuit Emulator" (poster) DS51749

## 2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator. For details, see **Section 9.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

**FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT**



**FIGURE 3-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X CPU BLOCK DIAGRAM**

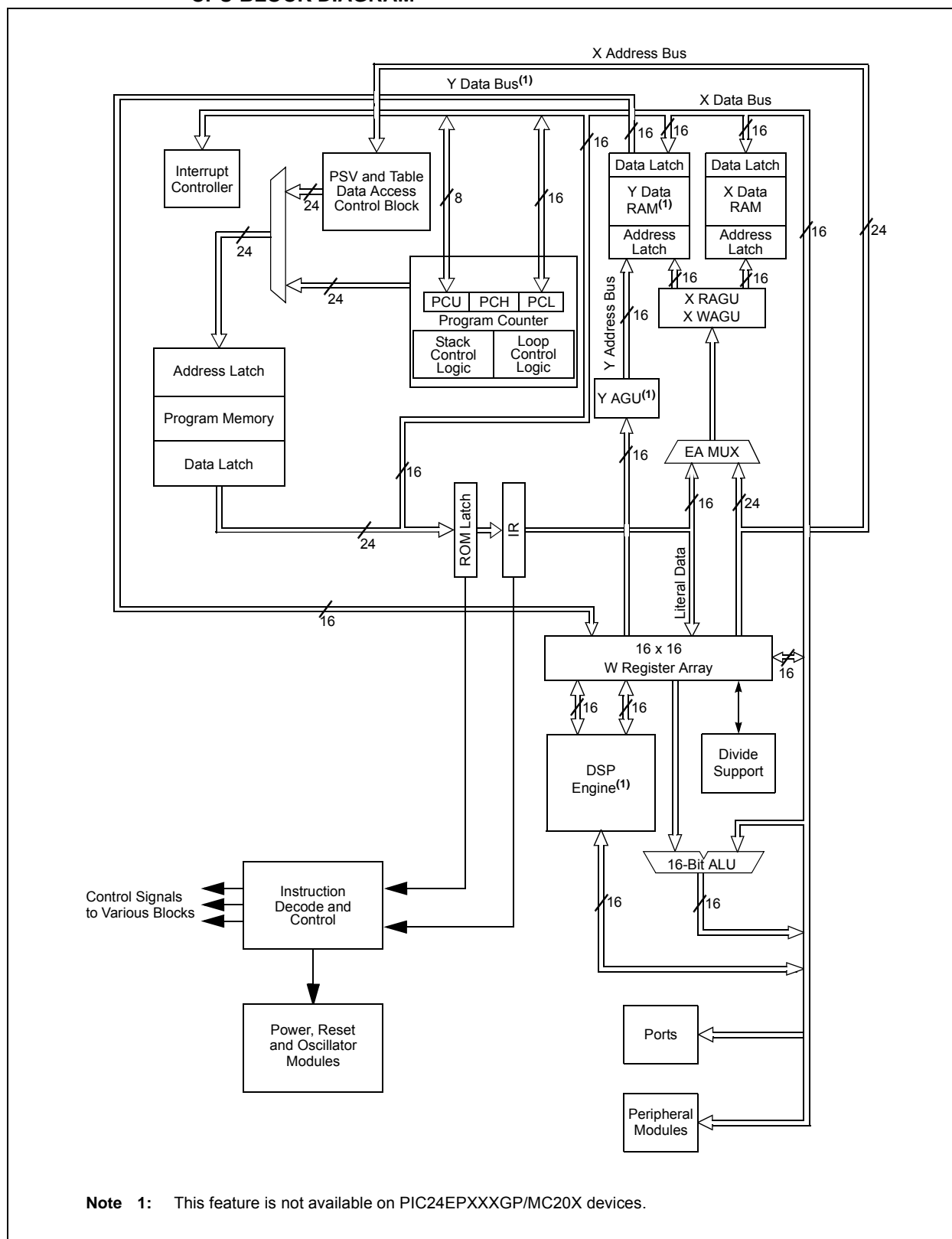
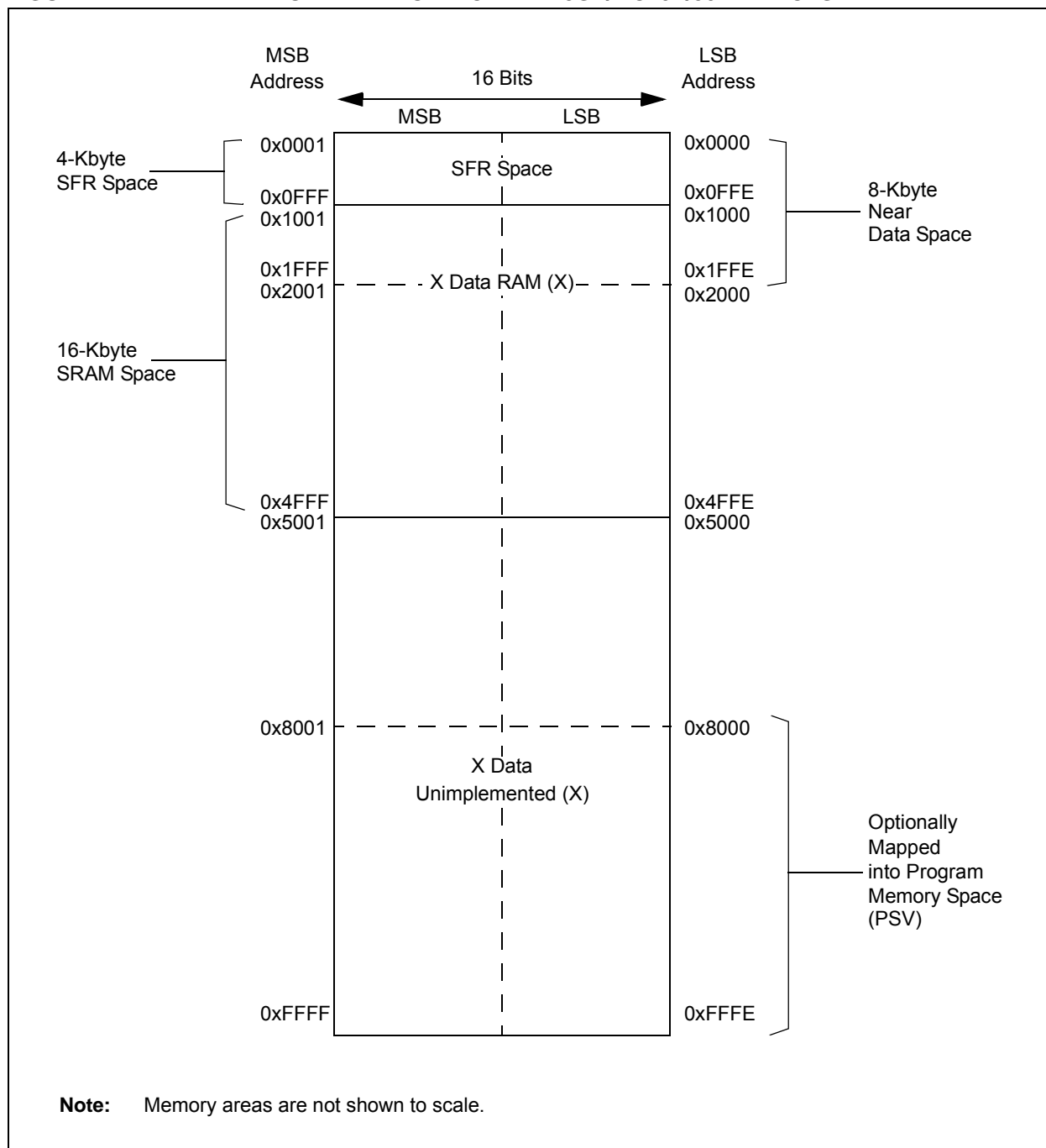


FIGURE 4-14: DATA MEMORY MAP FOR PIC24EP128GP/MC20X/50X DEVICES



## 11.0 I/O PORTS

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “I/O Ports” (DS70598) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

Many of the device pins are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

### 11.1 Parallel I/O (PIO) Ports

Generally, a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port

has ownership of the output data and control signals of the I/O pin. The logic also prevents “loop through,” in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

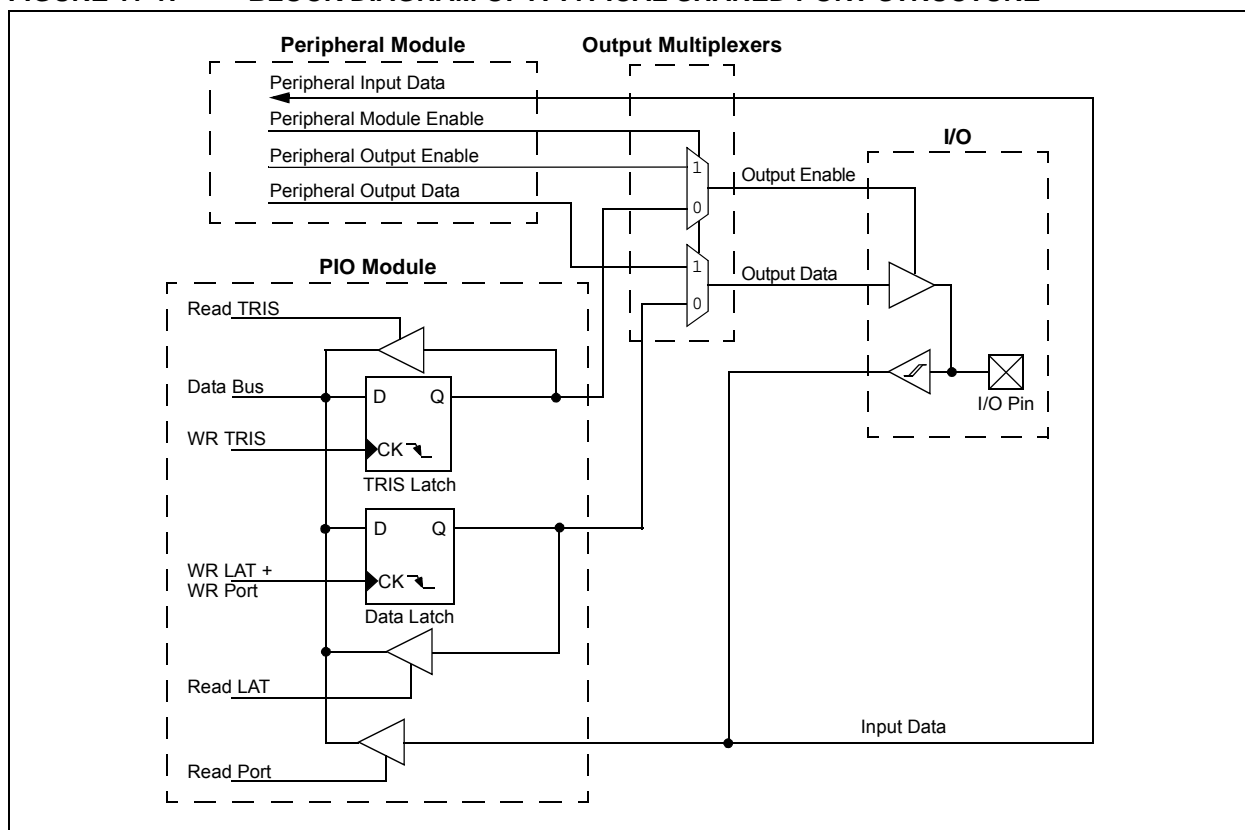
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have eight registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a ‘1’, then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Latch register (LATx) read the latch. Writes to the Latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device is disabled. This means the corresponding LATx and TRISx registers and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

**FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE**



## **11.4 Peripheral Pin Select (PPS)**

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient work-arounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

### **11.4.1 AVAILABLE PINS**

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, “RPn” or “RPI n”, in their full pin designation, where “n” is the remappable pin number. “RP” is used to designate pins that support both remappable input and output functions, while “RPI” indicates pins that support remappable input functions only.

### **11.4.2 AVAILABLE PERIPHERALS**

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I<sup>2</sup>C™ and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

### **11.4.3 CONTROLLING PERIPHERAL PIN SELECT**

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

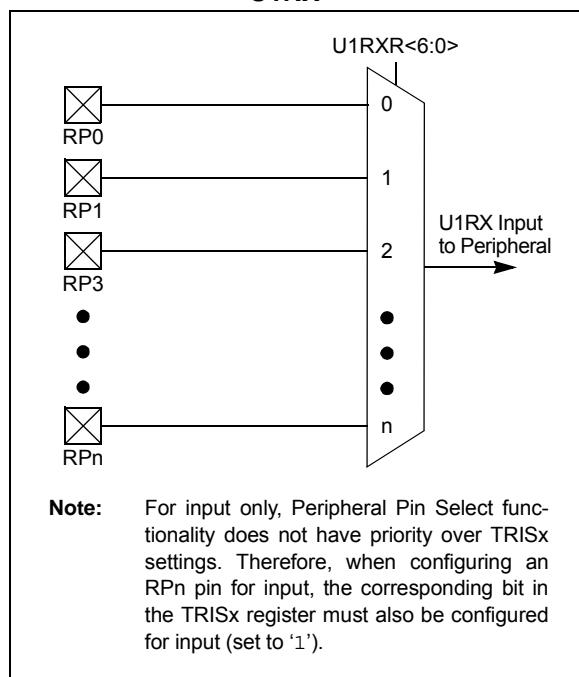
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

#### 11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

**FIGURE 11-2: REMAPPABLE INPUT FOR U1RX**



##### 11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 25-1 in **Section 25.0 “Op Amp/Comparator Module”**), and the PTG module (see **Section 24.0 “Peripheral Trigger Generator (PTG) Module”**).

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QE1 module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in **Section 17.0 “Quadrature Encoder Interface (QE1) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”**).

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of 'b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QE1 module allows peripherals to be connected to the QE1 digital filter input. To utilize this filter, the QE1 module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QE1 digital filter.

**EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QE1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE**

```
RPINR15 = 0x2500;    /* Connect the QE1 HOME1 input to RP37 (pin 43) */
RPINR7  = 0x009;    /* Connect the IC1 input to the digital filter on the FHOME1 input */

QE1IOC = 0x4000;    /* Enable the QE1 digital filter */
QE1CON = 0x8000;    /* Enable the QE1 module */
```

**REGISTER 11-9: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15  
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	HOME1R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INDX1R<6:0>						
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **HOME1R<6:0>:** Assign QE11 HOME1 (HOME1) to the Corresponding RPn Pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **INDX1R<6:0>:** Assign QE11 INDEX1 (INDX1) to the Corresponding RPn Pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

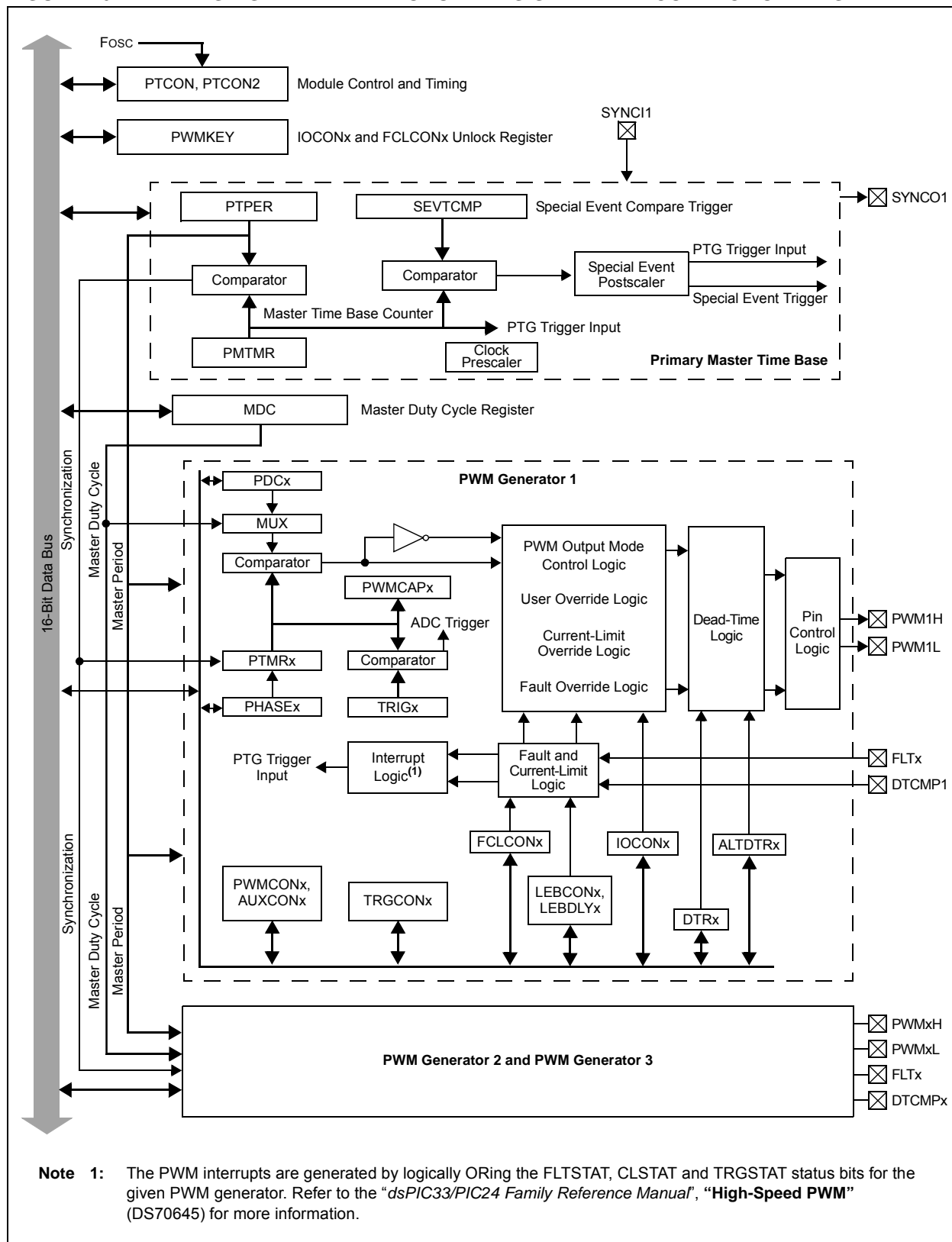
.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss



**FIGURE 16-2: HIGH-SPEED PWMx MODULE REGISTER INTERCONNECTION DIAGRAM**

**REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER<sup>(2)</sup> (CONTINUED)**

- bit 1      **SWAP:** SWAP PWMxH and PWMxL Pins bit  
            1 = PWMxH output signal is connected to PWMxL pins; PWMxL output signal is connected to PWMxH pins  
            0 = PWMxH and PWMxL pins are mapped to their respective pins
- bit 0      **OSYNC:** Output Override Synchronization bit  
            1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWMx period boundary  
            0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary

- Note 1:** These bits should not be changed after the PWMx module is enabled (PTEN = 1).
- 2:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

**REGISTER 21-8: CxEC: ECANx TRANSMIT/RECEIVE ERROR COUNT REGISTER**

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TERRCNT<7:0>							
bit 15							
bit 8							

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RERRCNT<7:0>							
bit 7							
bit 0							

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-8      **TERRCNT<7:0>**: Transmit Error Count bits

bit 7-0      **RERRCNT<7:0>**: Receive Error Count bits

**REGISTER 21-9: CxCFG1: ECANx BAUD RATE CONFIGURATION REGISTER 1**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							
bit 8							

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
bit 7							
bit 0							

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-8      **Unimplemented:** Read as '0'

bit 7-6      **SJW<1:0>**: Synchronization Jump Width bits

11 = Length is 4 x T<sub>Q</sub>

10 = Length is 3 x T<sub>Q</sub>

01 = Length is 2 x T<sub>Q</sub>

00 = Length is 1 x T<sub>Q</sub>

bit 5-0      **BRP<5:0>**: Baud Rate Prescaler bits

11 1111 = T<sub>Q</sub> = 2 x 64 x 1/FCAN

•

•

•

00 0010 = T<sub>Q</sub> = 2 x 3 x 1/FCAN

00 0001 = T<sub>Q</sub> = 2 x 2 x 1/FCAN

00 0000 = T<sub>Q</sub> = 2 x 1 x 1/FCAN

**REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGADJ<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGADJ<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **PTGADJ<15:0>**: PTG Adjust Register bits  
 This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGADD command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGL0<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGL0<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **PTGL0<15:0>**: PTG Literal 0 Register bits  
 This register holds the 16-bit value to be written to the AD1CHS0 register with the PTGCTRL Step command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

## 25.0 OP AMP/COMPARATOR MODULE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Op Amp/Comparator” (DS70357) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain up to four comparators, which can be configured in various ways. Comparators, CMP1, CMP2 and CMP3, also have the option to be configured as op amps, with the output being brought to an external pin for gain/filtering connections. As shown in Figure 25-1, individual comparator options are specified by the comparator module's Special Function Register (SFR) control bits.

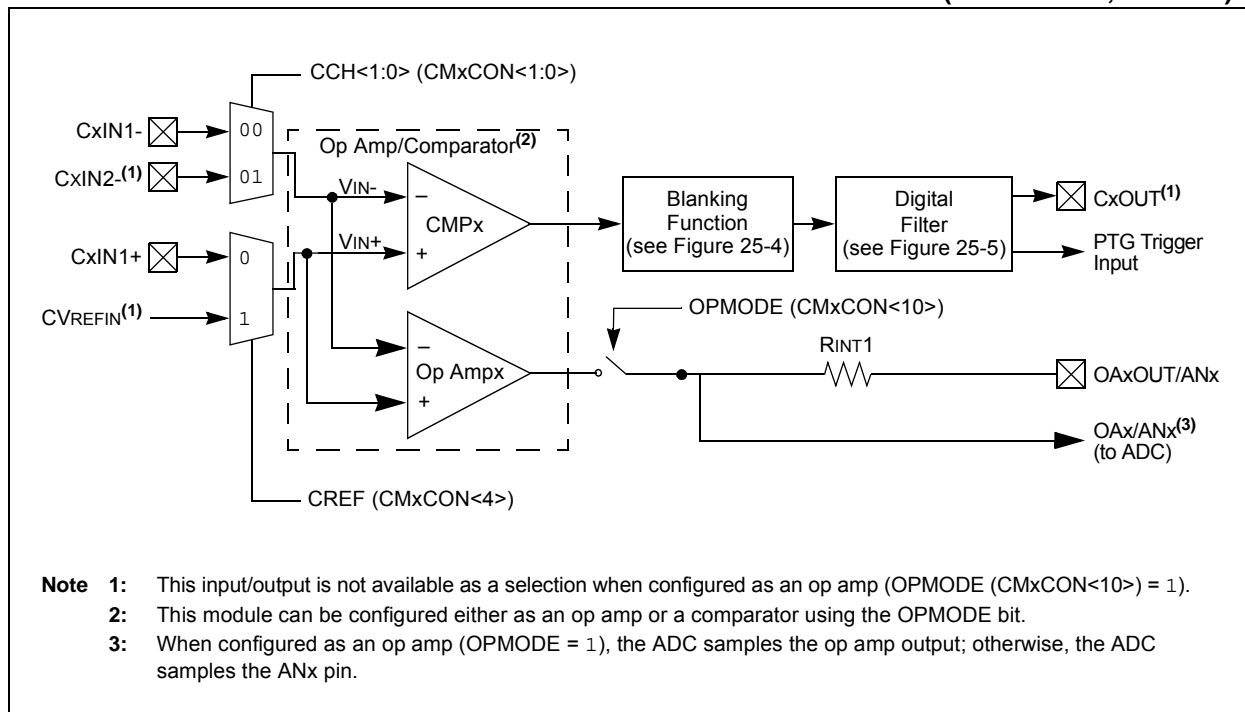
**Note:** Op Amp/Comparator 3 is not available on the dsPIC33EPXXXGP502/MC502/MC202 and PIC24EP256GP/MC202 (28-pin) devices.

These options allow users to:

- Select the edge for trigger and interrupt generation
- Configure the comparator voltage reference
- Configure output blanking and masking
- Configure as a comparator or op amp (CMP1, CMP2 and CMP3 only)

**Note:** Not all op amp/comparator input/output connections are available on all devices. See the “Pin Diagrams” section for available connections.

**FIGURE 25-1: OP AMP/COMPARATOR x MODULE BLOCK DIAGRAM (MODULES 1, 2 AND 3)**



**REGISTER 25-4: CMxMSKSRCA: COMPARATOR x MASK SOURCE SELECT  
CONTROL REGISTER (CONTINUED)**

bit 3-0      **SELSRCA<3:0>**: Mask A Input Select bits

1111 = FLT4  
1110 = FLT2  
1101 = PTGO19  
1100 = PTGO18  
1011 = Reserved  
1010 = Reserved  
1001 = Reserved  
1000 = Reserved  
0111 = Reserved  
0110 = Reserved  
0101 = PWM3H  
0100 = PWM3L  
0011 = PWM2H  
0010 = PWM2L  
0001 = PWM1H  
0000 = PWM1L

## **29.0 DEVELOPMENT SUPPORT**

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for  
Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICKit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,  
Evaluation Kits and Starter Kits
- Third-party development tools

## **29.1 MPLAB X Integrated Development Environment Software**

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

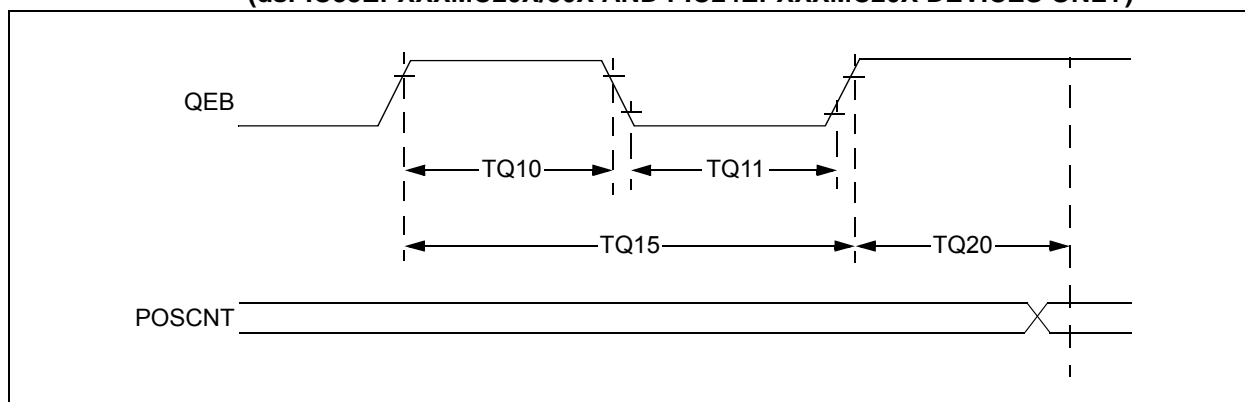
Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

**FIGURE 30-11: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS  
(dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)**



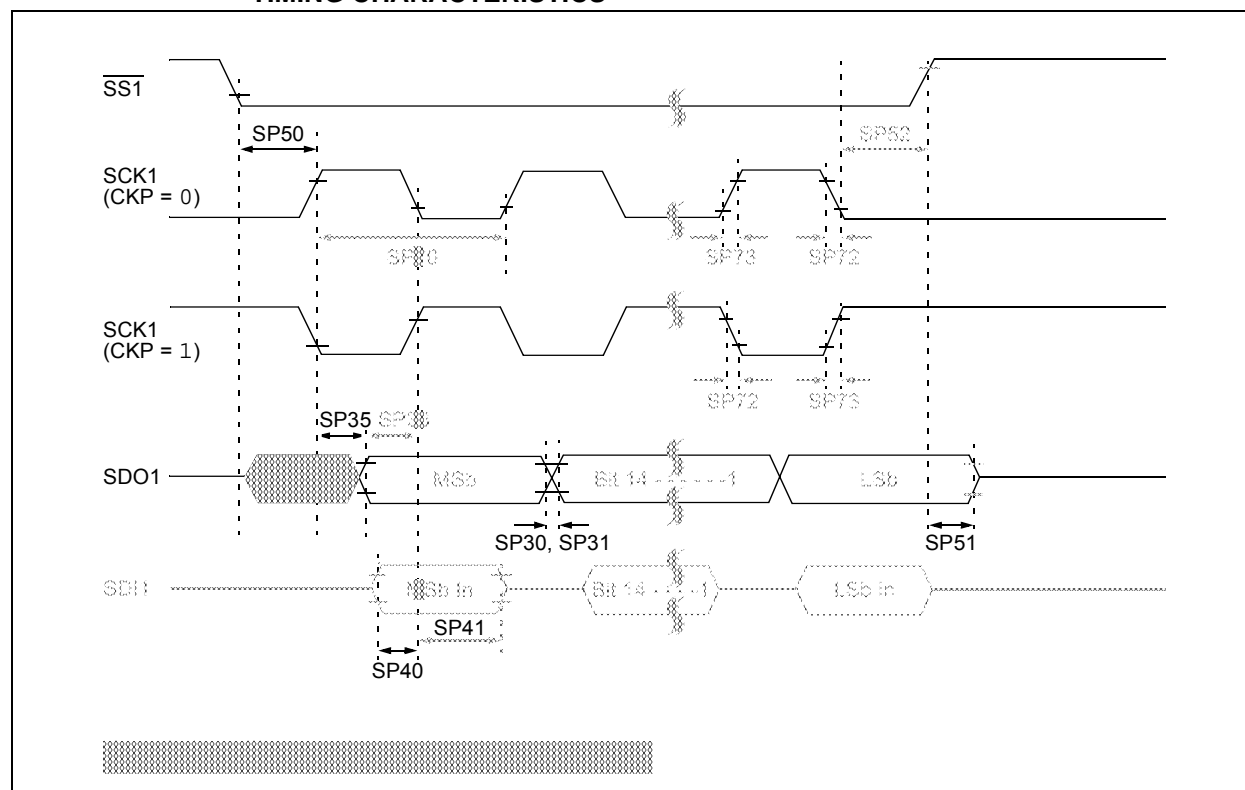
**TABLE 30-30: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS  
(dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)**

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>		Min.	Typ.	Max.	Units	Conditions
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	Greater of $12.5 + 25$ or $(0.5 T_{CY}/N) + 25$	—	—	ns	Must also meet Parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	Greater of $12.5 + 25$ or $(0.5 T_{CY}/N) + 25$	—	—	ns	Must also meet Parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	Greater of $25 + 50$ or $(1 T_{CY}/N) + 50$	—	—	ns	
TQ20	TCKEXTMRL	Delay from External TQCK Clock Edge to Timer Increment		—	1	$T_{CY}$	—	

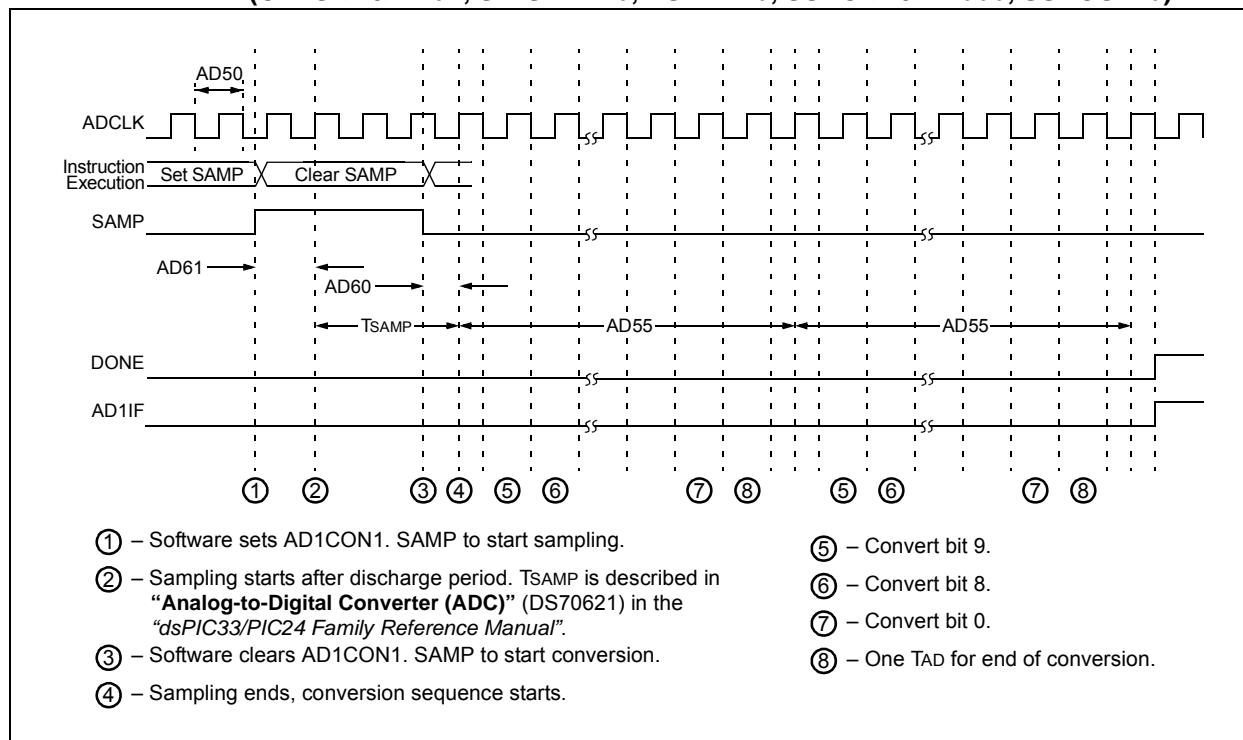
**Note 1:** These parameters are characterized but not tested in manufacturing.



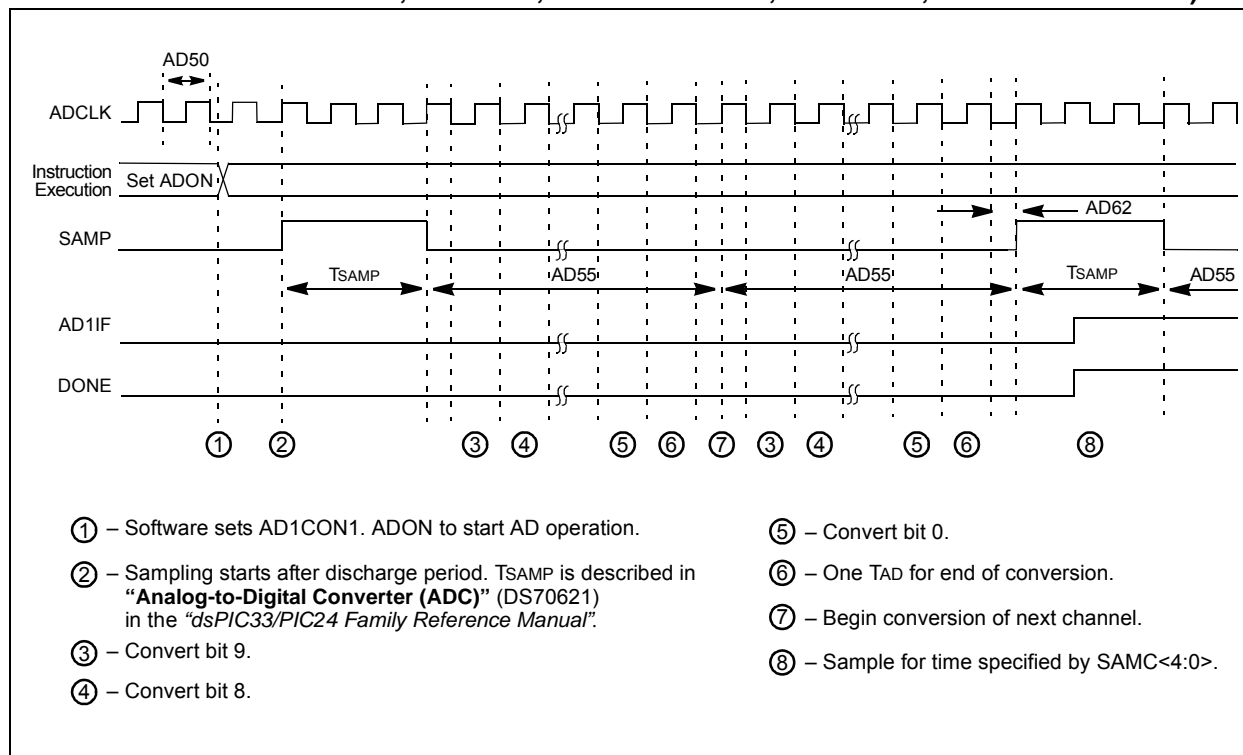
**FIGURE 30-28: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)**  
**TIMING CHARACTERISTICS**



**FIGURE 30-37: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS**  
(CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRG = 0)



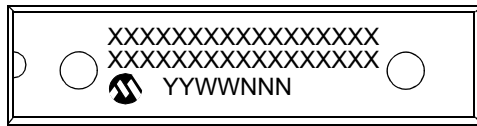
**FIGURE 30-38: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS** (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRG = 0, SAMC<4:0> = 00010)



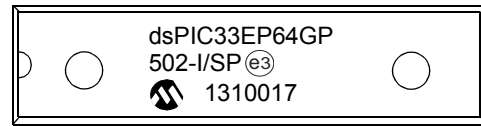
## 33.0 PACKAGING INFORMATION

### 33.1 Package Marking Information

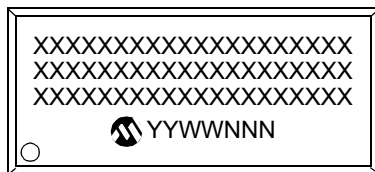
28-Lead SPDIP



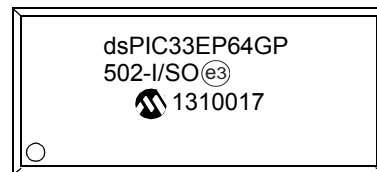
Example



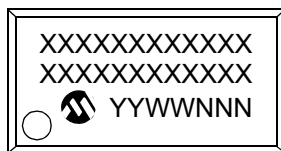
28-Lead SOIC (.300")



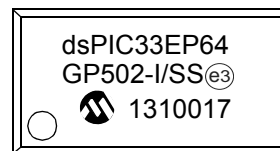
Example



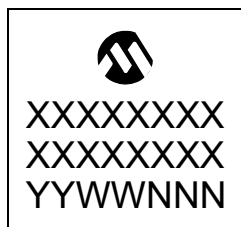
28-Lead SSOP



Example



28-Lead QFN-S (6x6x0.9 mm)



Example

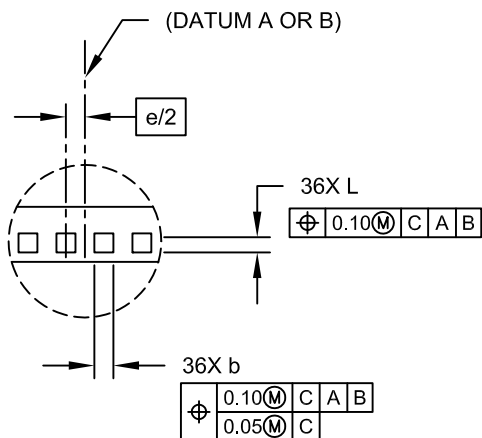
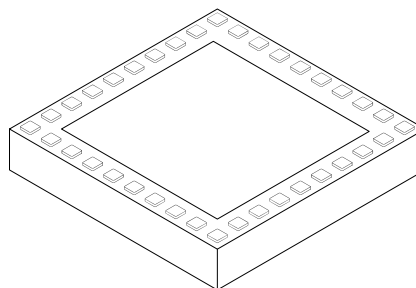


<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

**36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

**DETAIL A**

Dimension	Units	MILLIMETERS		
	Limits	MIN	NOM	MAX
Number of Pins	N	36		
Number of Pins per Side	ND	10		
Number of Pins per Side	NE	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	3.60	3.75	3.90
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	3.60	3.75	3.90
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

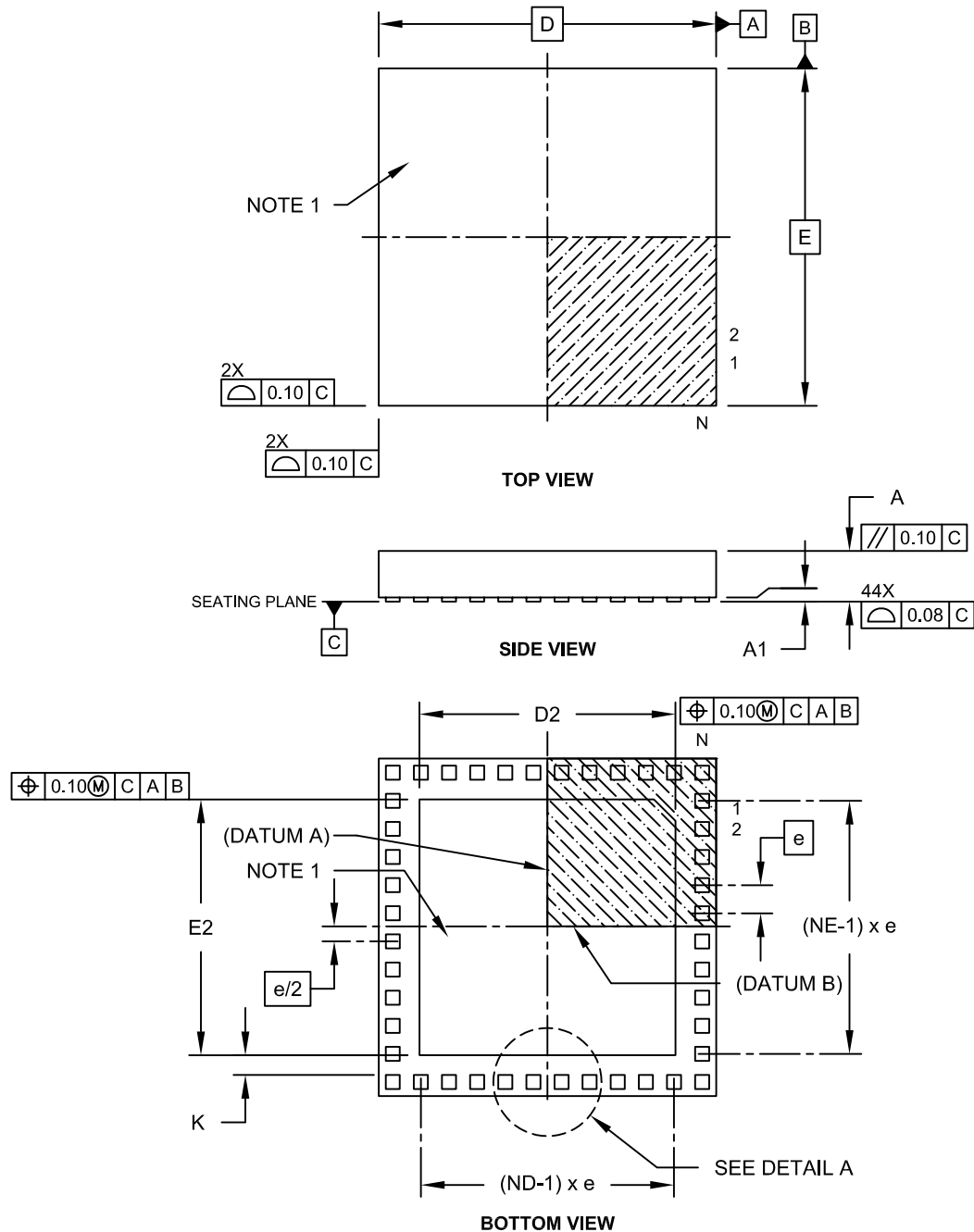
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2

#### 44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-157C Sheet 1 of 2