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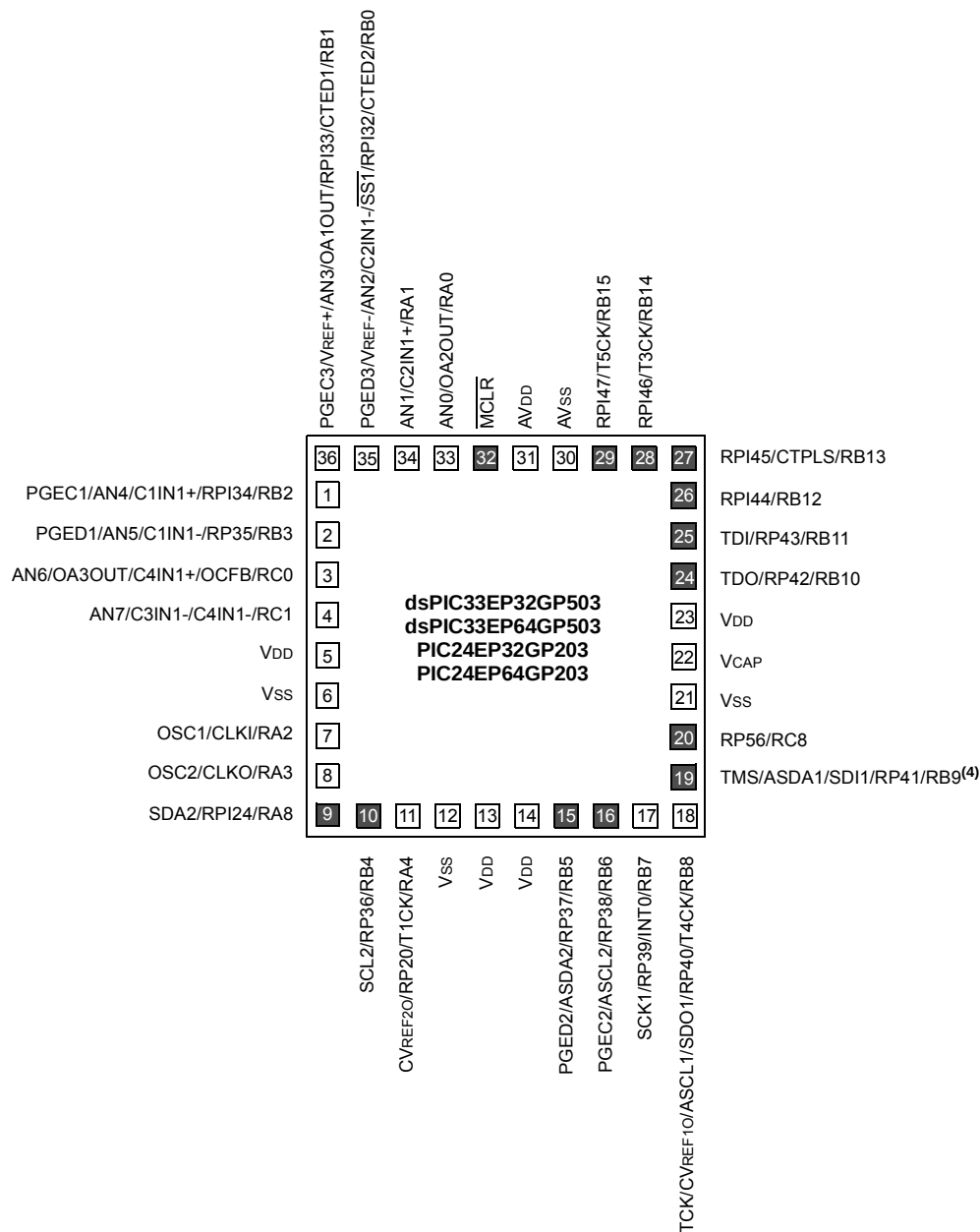
#### Details

|                            |                                                                                                                                                                                 |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                                          |
| Core Processor             | dsPIC                                                                                                                                                                           |
| Core Size                  | 16-Bit                                                                                                                                                                          |
| Speed                      | 70 MIPS                                                                                                                                                                         |
| Connectivity               | CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART                                                                                                                         |
| Peripherals                | Brown-out Detect/Reset, DMA, POR, PWM, WDT                                                                                                                                      |
| Number of I/O              | 21                                                                                                                                                                              |
| Program Memory Size        | 256KB (85.5K x 24)                                                                                                                                                              |
| Program Memory Type        | FLASH                                                                                                                                                                           |
| EEPROM Size                | -                                                                                                                                                                               |
| RAM Size                   | 16K x 16                                                                                                                                                                        |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V                                                                                                                                                                       |
| Data Converters            | A/D 6x10b/12b                                                                                                                                                                   |
| Oscillator Type            | Internal                                                                                                                                                                        |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                                               |
| Mounting Type              | Surface Mount                                                                                                                                                                   |
| Package / Case             | 28-SSOP (0.209", 5.30mm Width)                                                                                                                                                  |
| Supplier Device Package    | 28-SSOP                                                                                                                                                                         |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gp502-i-ss">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gp502-i-ss</a> |

## Pin Diagrams (Continued)

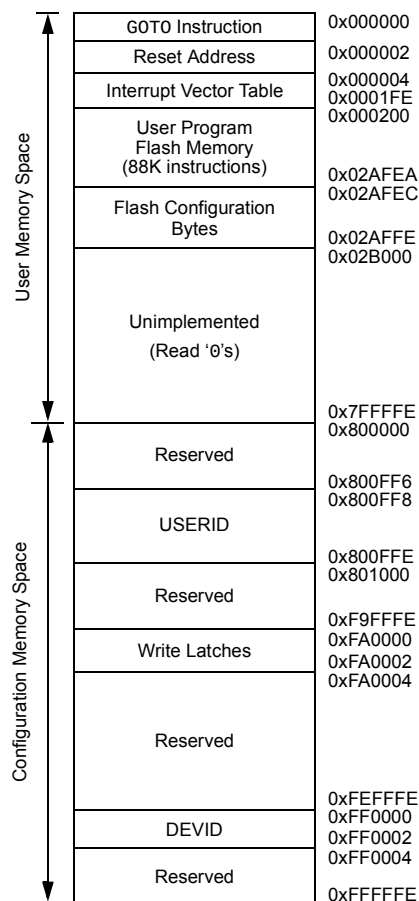
36-Pin VTLA<sup>(1,2,3)</sup>

■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
  - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
  - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
  - 4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X AND PIC24EP256GP/MC20X DEVICES



**Note:** Memory areas are not shown to scale.

**TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12  | Bit 11   | Bit 10 | Bit 9 | Bit 8 | Bit 7       | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2  | Bit 1   | Bit 0  | All Resets |
|-----------|-------|--------|--------|--------|---------|----------|--------|-------|-------|-------------|---------|---------|---------|---------|--------|---------|--------|------------|
| INTCON1   | 08C0  | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR  | OVATE  | OVBT  | COVTE | SFTACERR    | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | —      | 0000       |
| INTCON2   | 08C2  | GIE    | DISI   | SWTRAP | —       | —        | —      | —     | —     | —           | —       | —       | —       | —       | INT2EP | INT1EP  | INT0EP | 8000       |
| INTCON3   | 08C4  | —      | —      | —      | —       | —        | —      | —     | —     | —           | —       | DAE     | DOOVR   | —       | —      | —       | —      | 0000       |
| INTCON4   | 08C6  | —      | —      | —      | —       | —        | —      | —     | —     | —           | —       | —       | —       | —       | —      | —       | SGHT   | 0000       |
| INTTREG   | 08C8  | —      | —      | —      | —       | ILR<3:0> |        |       |       | VECNUM<7:0> |         |         |         |         |        |         |        | 0000       |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-27: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC204/504 AND PIC24EPXXXGP/MC204 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13     | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5      | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--------|--------|------------|--------|--------|--------|-------|-------|-------|-------|------------|-------|-------|-------|-------|-------|------------|
| RPOR0     | 0680  | —      | —      | RP35R<5:0> |        |        |        |       |       | —     | —     | RP20R<5:0> |       |       |       |       |       | 0000       |
| RPOR1     | 0682  | —      | —      | RP37R<5:0> |        |        |        |       |       | —     | —     | RP36R<5:0> |       |       |       |       |       | 0000       |
| RPOR2     | 0684  | —      | —      | RP39R<5:0> |        |        |        |       |       | —     | —     | RP38R<5:0> |       |       |       |       |       | 0000       |
| RPOR3     | 0686  | —      | —      | RP41R<5:0> |        |        |        |       |       | —     | —     | RP40R<5:0> |       |       |       |       |       | 0000       |
| RPOR4     | 0688  | —      | —      | RP43R<5:0> |        |        |        |       |       | —     | —     | RP42R<5:0> |       |       |       |       |       | 0000       |
| RPOR5     | 068A  | —      | —      | RP55R<5:0> |        |        |        |       |       | —     | —     | RP54R<5:0> |       |       |       |       |       | 0000       |
| RPOR6     | 068C  | —      | —      | RP57R<5:0> |        |        |        |       |       | —     | —     | RP56R<5:0> |       |       |       |       |       | 0000       |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-28: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC206/506 AND PIC24EPXXXGP/MC206 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13      | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5       | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--------|--------|-------------|--------|--------|--------|-------|-------|-------|-------|-------------|-------|-------|-------|-------|-------|------------|
| RPOR0     | 0680  | —      | —      | RP35R<5:0>  |        |        |        |       |       | —     | —     | RP20R<5:0>  |       |       |       |       |       | 0000       |
| RPOR1     | 0682  | —      | —      | RP37R<5:0>  |        |        |        |       |       | —     | —     | RP36R<5:0>  |       |       |       |       |       | 0000       |
| RPOR2     | 0684  | —      | —      | RP39R<5:0>  |        |        |        |       |       | —     | —     | RP38R<5:0>  |       |       |       |       |       | 0000       |
| RPOR3     | 0686  | —      | —      | RP41R<5:0>  |        |        |        |       |       | —     | —     | RP40R<5:0>  |       |       |       |       |       | 0000       |
| RPOR4     | 0688  | —      | —      | RP43R<5:0>  |        |        |        |       |       | —     | —     | RP42R<5:0>  |       |       |       |       |       | 0000       |
| RPOR5     | 068A  | —      | —      | RP55R<5:0>  |        |        |        |       |       | —     | —     | RP54R<5:0>  |       |       |       |       |       | 0000       |
| RPOR6     | 068C  | —      | —      | RP57R<5:0>  |        |        |        |       |       | —     | —     | RP56R<5:0>  |       |       |       |       |       | 0000       |
| RPOR7     | 068E  | —      | —      | RP97R<5:0>  |        |        |        |       |       | —     | —     | —           | —     | —     | —     | —     | —     | 0000       |
| RPOR8     | 0690  | —      | —      | RP118R<5:0> |        |        |        |       |       | —     | —     | —           | —     | —     | —     | —     | —     | 0000       |
| RPOR9     | 0692  | —      | —      | —           | —      | —      | —      | —     | —     | —     | —     | RP120R<5:0> |       |       |       |       |       | 0000       |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-29: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14       | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6      | Bit 5        | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |      |      |
|-----------|-------|--------|--------------|--------|--------|--------|--------|-------|-------|-------|------------|--------------|-------|-------|-------|-------|-------|------------|------|------|
| RPINR0    | 06A0  | —      | INT1R<6:0>   |        |        |        |        |       |       |       | —          | —            | —     | —     | —     | —     | —     | —          | 0000 |      |
| RPINR1    | 06A2  | —      | —            | —      | —      | —      | —      | —     | —     | —     | INT2R<6:0> |              |       |       |       |       |       |            | 0000 |      |
| RPINR3    | 06A6  | —      | —            | —      | —      | —      | —      | —     | —     | —     | T2CKR<6:0> |              |       |       |       |       |       |            | 0000 |      |
| RPINR7    | 06AE  | —      | IC2R<6:0>    |        |        |        |        |       |       |       | —          | IC1R<6:0>    |       |       |       |       |       |            |      | 0000 |
| RPINR8    | 06B0  | —      | IC4R<6:0>    |        |        |        |        |       |       |       | —          | IC3R<6:0>    |       |       |       |       |       |            |      | 0000 |
| RPINR11   | 06B6  | —      | —            | —      | —      | —      | —      | —     | —     | —     | OCFAR<6:0> |              |       |       |       |       |       |            | 0000 |      |
| RPINR12   | 06B8  | —      | FLT2R<6:0>   |        |        |        |        |       |       |       | —          | FLT1R<6:0>   |       |       |       |       |       |            |      | 0000 |
| RPINR14   | 06BC  | —      | QEB1R<6:0>   |        |        |        |        |       |       |       | —          | QEA1R<6:0>   |       |       |       |       |       |            |      | 0000 |
| RPINR15   | 06BE  | —      | HOME1R<6:0>  |        |        |        |        |       |       |       | —          | INDX1R<6:0>  |       |       |       |       |       |            |      | 0000 |
| RPINR18   | 06C4  | —      | —            | —      | —      | —      | —      | —     | —     | —     | U1RXR<6:0> |              |       |       |       |       |       |            | 0000 |      |
| RPINR19   | 06C6  | —      | —            | —      | —      | —      | —      | —     | —     | —     | U2RXR<6:0> |              |       |       |       |       |       |            | 0000 |      |
| RPINR22   | 06CC  | —      | SCK2INR<6:0> |        |        |        |        |       |       |       | —          | SDI2R<6:0>   |       |       |       |       |       |            |      | 0000 |
| RPINR23   | 06CE  | —      | —            | —      | —      | —      | —      | —     | —     | —     | SS2R<6:0>  |              |       |       |       |       |       |            | 0000 |      |
| RPINR26   | 06D4  | —      | —            | —      | —      | —      | —      | —     | —     | —     | —          | —            | —     | —     | —     | —     | —     | 0000       |      |      |
| RPINR37   | 06EA  | —      | SYNCI1R<6:0> |        |        |        |        |       |       |       | —          | —            | —     | —     | —     | —     | —     | —          | 0000 |      |
| RPINR38   | 06EC  | —      | DTCMP1R<6:0> |        |        |        |        |       |       |       | —          | —            | —     | —     | —     | —     | —     | —          | 0000 |      |
| RPINR39   | 06EE  | —      | DTCMP3R<6:0> |        |        |        |        |       |       |       | —          | DTCMP2R<6:0> |       |       |       |       |       |            |      | 0000 |

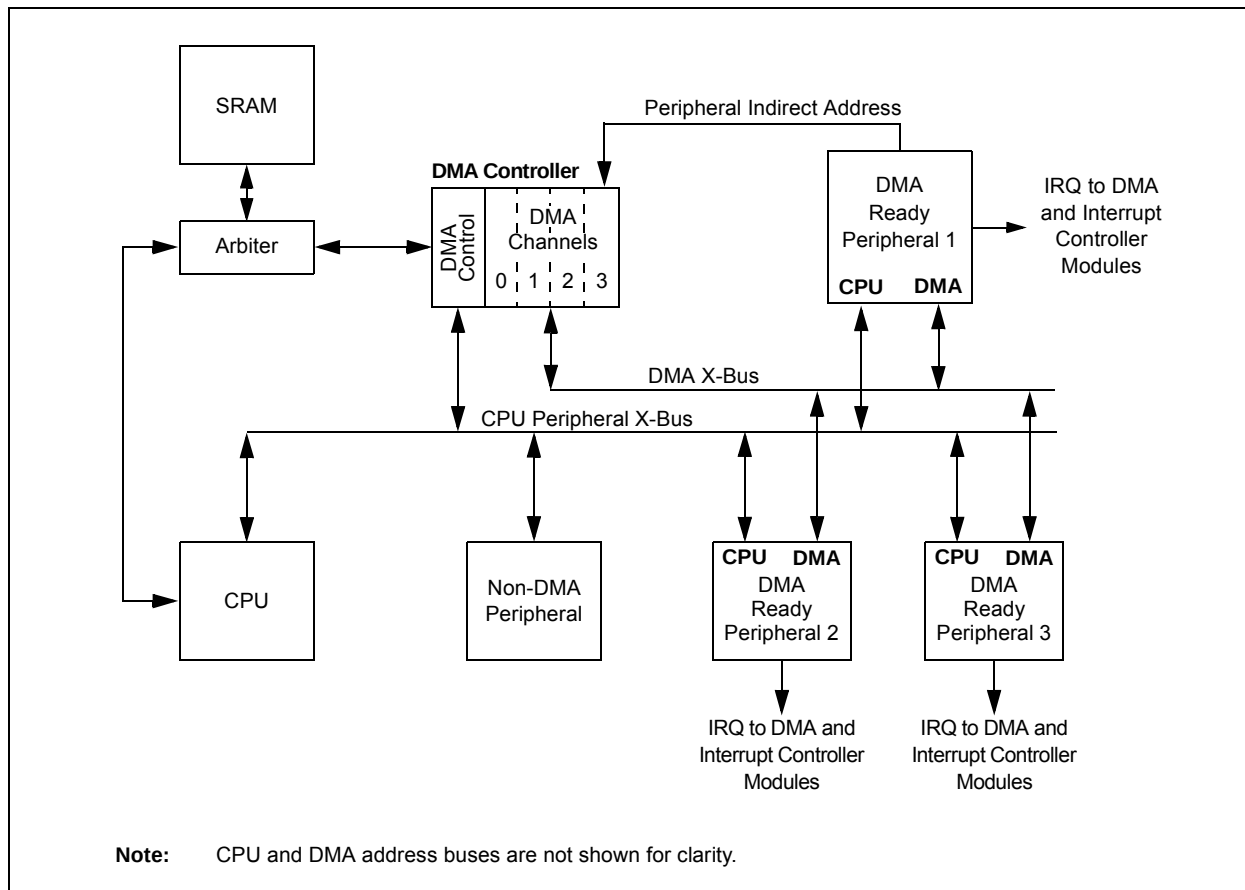
**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-30: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14       | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6      | Bit 5      | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |      |      |
|-----------|-------|--------|--------------|--------|--------|--------|--------|-------|-------|-------|------------|------------|-------|-------|-------|-------|-------|------------|------|------|
| RPINR0    | 06A0  | —      | INT1R<6:0>   |        |        |        |        |       |       |       | —          | —          | —     | —     | —     | —     | —     | —          | 0000 |      |
| RPINR1    | 06A2  | —      | —            | —      | —      | —      | —      | —     | —     | —     | INT2R<6:0> |            |       |       |       |       |       |            | 0000 |      |
| RPINR3    | 06A6  | —      | —            | —      | —      | —      | —      | —     | —     | —     | T2CKR<6:0> |            |       |       |       |       |       |            | 0000 |      |
| RPINR7    | 06AE  | —      | IC2R<6:0>    |        |        |        |        |       |       |       | —          | IC1R<6:0>  |       |       |       |       |       |            |      | 0000 |
| RPINR8    | 06B0  | —      | IC4R<6:0>    |        |        |        |        |       |       |       | —          | IC3R<6:0>  |       |       |       |       |       |            |      | 0000 |
| RPINR11   | 06B6  | —      | —            | —      | —      | —      | —      | —     | —     | —     | OCFAR<6:0> |            |       |       |       |       |       |            | 0000 |      |
| RPINR18   | 06C4  | —      | —            | —      | —      | —      | —      | —     | —     | —     | U1RXR<6:0> |            |       |       |       |       |       |            | 0000 |      |
| RPINR19   | 06C6  | —      | —            | —      | —      | —      | —      | —     | —     | —     | U2RXR<6:0> |            |       |       |       |       |       |            | 0000 |      |
| RPINR22   | 06CC  | —      | SCK2INR<6:0> |        |        |        |        |       |       |       | —          | SDI2R<6:0> |       |       |       |       |       |            |      | 0000 |
| RPINR23   | 06CE  | —      | —            | —      | —      | —      | —      | —     | —     | —     | SS2R<6:0>  |            |       |       |       |       |       |            | 0000 |      |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

FIGURE 8-2: DMA CONTROLLER BLOCK DIAGRAM



## 8.1 DMA Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 8.1.1 KEY RESOURCES

- **Section 22. "Direct Memory Access (DMA)"** (DS70348) in the "*dsPIC33/PIC24 Family Reference Manual*"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "*dsPIC33/PIC24 Family Reference Manual*" Sections
- Development Tools

## 8.2 DMAC Registers

Each DMAC Channel  $x$  (where  $x = 0$  through 3) contains the following registers:

- 16-Bit DMA Channel Control register (DMAxCON)
- 16-Bit DMA Channel IRQ Select register (DMAxREQ)
- 32-Bit DMA RAM Primary Start Address register (DMAxSTA)
- 32-Bit DMA RAM Secondary Start Address register (DMAxSTB)
- 16-Bit DMA Peripheral Address register (DMAxPAD)
- 14-Bit DMA Transfer Count register (DMAxCNT)

Additional status registers (DMAPWC, DMARQC, DMAPPS, DMALCA and DSADR) are common to all DMAC channels. These status registers provide information on write and request collisions, as well as on last address and channel access information.

The interrupt flags (DMAxIF) are located in an IFSx register in the interrupt controller. The corresponding interrupt enable control bits (DMAxIE) are located in an IECx register in the interrupt controller, and the corresponding interrupt priority control bits (DMAxIP) are located in an IPCx register in the interrupt controller.

**REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)**

|       |                                                                                                                     |
|-------|---------------------------------------------------------------------------------------------------------------------|
| bit 3 | <b>SPI1MD:</b> SPI1 Module Disable bit<br>1 = SPI1 module is disabled<br>0 = SPI1 module is enabled                 |
| bit 2 | <b>Unimplemented:</b> Read as '0'                                                                                   |
| bit 1 | <b>C1MD:</b> ECAN1 Module Disable bit <sup>(2)</sup><br>1 = ECAN1 module is disabled<br>0 = ECAN1 module is enabled |
| bit 0 | <b>AD1MD:</b> ADC1 Module Disable bit<br>1 = ADC1 module is disabled<br>0 = ADC1 module is enabled                  |

**Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

## 15.0 OUTPUT COMPARE

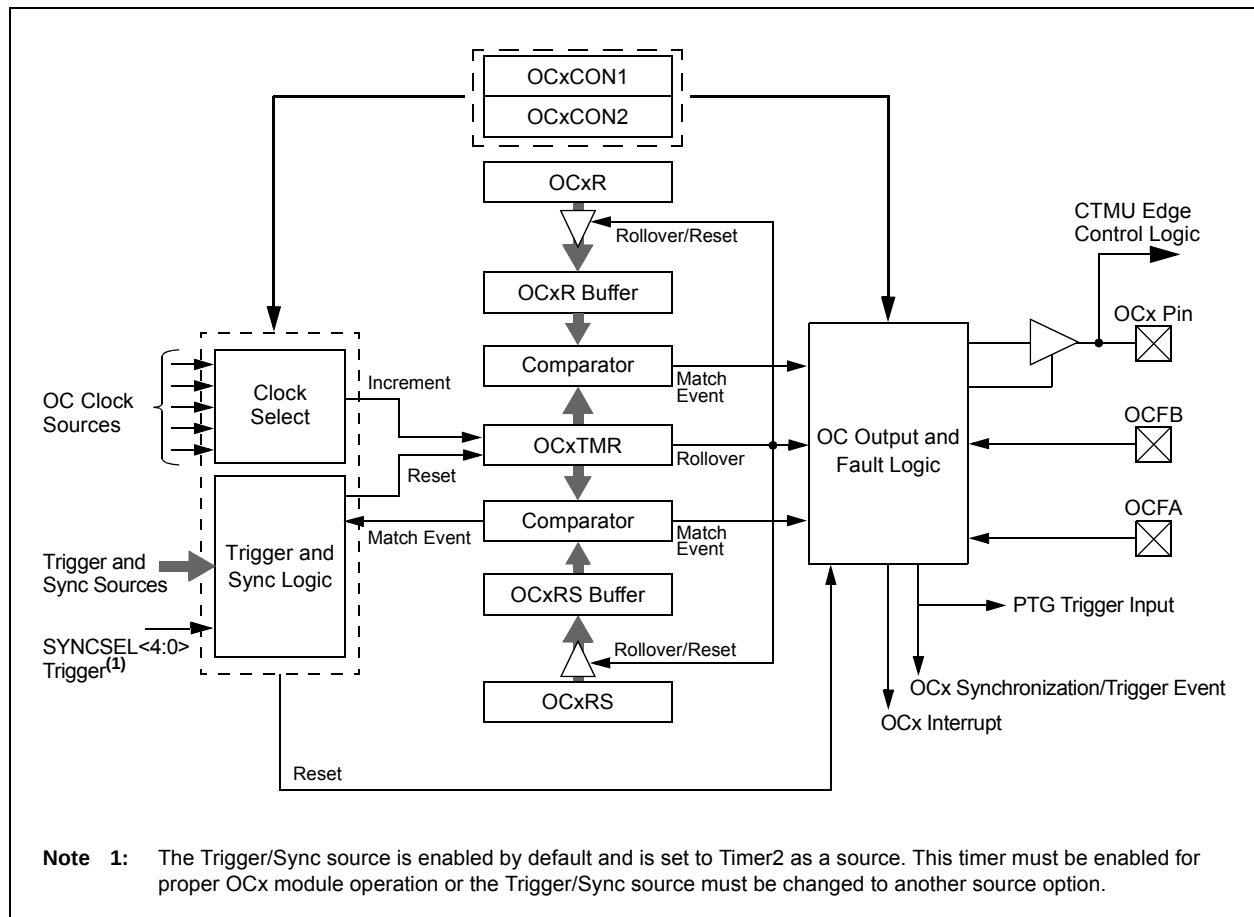
**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Output Compare**” (DS70358) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

**Note:** See “**Output Compare**” (DS70358) in the “dsPIC33/PIC24 Family Reference Manual” for OCxR and OCxRS register restrictions.

**FIGURE 15-1: OUTPUT COMPARE x MODULE BLOCK DIAGRAM**



## 18.0 SERIAL PERIPHERAL INTERFACE (SPI)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Serial Peripheral Interface (SPI)**” (DS70569) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with Motorola® SPI and SIOP interfaces.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X device family offers two SPI modules on a single device. These modules, which are designated as SPI1 and SPI2, are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

**Note:** In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of the SPI2 module, but results in a lower maximum speed for SPI2. See **Section 30.0 “Electrical Characteristics”** for more information.

The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- SSx/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, SSx is not used. In 2-pin mode, neither SDOx nor SSx is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

**REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER**

|          |          |     |     |     |           |          |          |
|----------|----------|-----|-----|-----|-----------|----------|----------|
| R-0, HSC | R-0, HSC | U-0 | U-0 | U-0 | R/C-0, HS | R-0, HSC | R-0, HSC |
| ACKSTAT  | TRSTAT   | —   | —   | —   | BCL       | GCSTAT   | ADD10    |
| bit 15   |          |     |     |     |           | bit 8    |          |

|           |           |          |            |            |          |          |          |
|-----------|-----------|----------|------------|------------|----------|----------|----------|
| R/C-0, HS | R/C-0, HS | R-0, HSC | R/C-0, HSC | R/C-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
| IWCOL     | I2COV     | D_A      | P          | S          | R_W      | RBF      | TBF      |
| bit 7     |           |          |            |            |          | bit 0    |          |

|                   |                   |                                    |                                       |
|-------------------|-------------------|------------------------------------|---------------------------------------|
| <b>Legend:</b>    | C = Clearable bit | HS = Hardware Settable bit         | HSC = Hardware Settable/Clearable bit |
| R = Readable bit  | W = Writable bit  | U = Unimplemented bit, read as '0' |                                       |
| -n = Value at POR | '1' = Bit is set  | '0' = Bit is cleared               | x = Bit is unknown                    |

- bit 15     **ACKSTAT:** Acknowledge Status bit (when operating as I<sup>2</sup>C™ master, applicable to master transmit operation)  
1 = NACK received from slave  
0 = ACK received from slave  
Hardware is set or clear at the end of slave Acknowledge.
- bit 14     **TRSTAT:** Transmit Status bit (when operating as I<sup>2</sup>C master, applicable to master transmit operation)  
1 = Master transmit is in progress (8 bits + ACK)  
0 = Master transmit is not in progress  
Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
- bit 13-11     **Unimplemented:** Read as '0'
- bit 10     **BCL:** Master Bus Collision Detect bit  
1 = A bus collision has been detected during a master operation  
0 = No bus collision detected  
Hardware is set at detection of a bus collision.
- bit 9     **GCSTAT:** General Call Status bit  
1 = General call address was received  
0 = General call address was not received  
Hardware is set when address matches general call address. Hardware is clear at Stop detection.
- bit 8     **ADD10:** 10-Bit Address Status bit  
1 = 10-bit address was matched  
0 = 10-bit address was not matched  
Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
- bit 7     **IWCOL:** I2Cx Write Collision Detect bit  
1 = An attempt to write to the I2CxTRN register failed because the I<sup>2</sup>C module is busy  
0 = No collision  
Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
- bit 6     **I2COV:** I2Cx Receive Overflow Flag bit  
1 = A byte was received while the I2CxRCV register was still holding the previous byte  
0 = No overflow  
Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
- bit 5     **D\_A:** Data/Address bit (when operating as I<sup>2</sup>C slave)  
1 = Indicates that the last byte received was data  
0 = Indicates that the last byte received was a device address  
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
- bit 4     **P:** Stop bit  
1 = Indicates that a Stop bit has been detected last  
0 = Stop bit was not detected last  
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

**REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER**

|        |     |     |     |     |     |       |       |
|--------|-----|-----|-----|-----|-----|-------|-------|
| U-0    | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| —      | —   | —   | —   | —   | —   | AMSK9 | AMSK8 |
| bit 15 |     |     |     |     |     | bit 8 |       |

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| AMSK7 | AMSK6 | AMSK5 | AMSK4 | AMSK3 | AMSK2 | AMSK1 | AMSK0 |
| bit 7 |       |       |       |       |       | bit 0 |       |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10

**Unimplemented:** Read as '0'

bit 9-0

**AMSK<9:0>:** Address Mask Select bits

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax + 1; bit match is required in this position

REGISTER 23-5: AD1CHS123: ADC1 INPUT CHANNEL 1, 2, 3 SELECT REGISTER (CONTINUED)

bit 0

**CH123SA:** Channel 1, 2, 3 Positive Input Select for Sample MUXA bit

In 12-bit mode (AD21B = 1), CH123SA is Unimplemented and is Read as '0':

| Value              | ADC Channel |         |         |
|--------------------|-------------|---------|---------|
|                    | CH1         | CH2     | CH3     |
| 1 <sup>(2)</sup>   | OA1/AN3     | OA2/AN0 | OA3/AN6 |
| 0 <sup>(1,2)</sup> | OA2/AN0     | AN1     | AN2     |

**Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

**2:** The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

## 27.0 SPECIAL FEATURES

**Note:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

## 27.1 Configuration Bits

In dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored in at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

**Note:** Configuration data is reloaded on all types of device Resets.

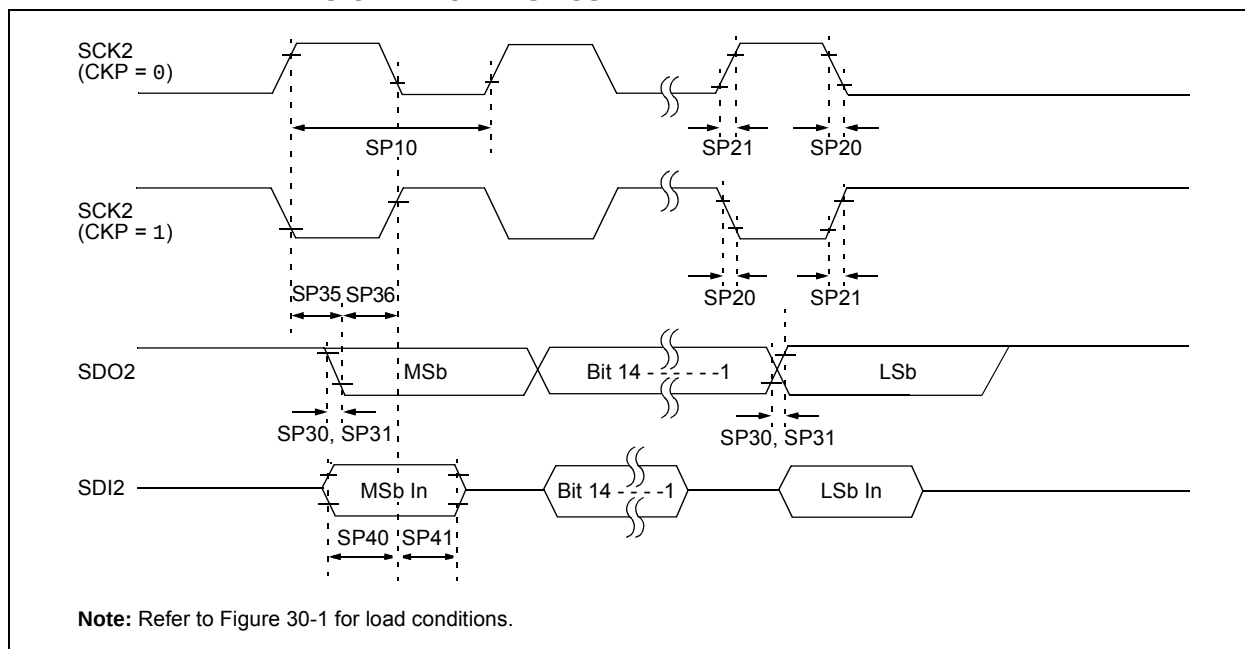
When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be ‘1111 1111 1111 1111’. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing ‘1’s to these locations has no effect on device operation.

**Note:** Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.

**FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)  
TIMING CHARACTERISTICS**



**TABLE 30-36: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)  
TIMING REQUIREMENTS**

| AC CHARACTERISTICS |                       |                                               | Standard Operating Conditions: 3.0V to 3.6V<br>(unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended |                     |      |       |                                |
|--------------------|-----------------------|-----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------|-------|--------------------------------|
| Param.             | Symbol                | Characteristic <sup>(1)</sup>                 | Min.                                                                                                                                                                    | Typ. <sup>(2)</sup> | Max. | Units | Conditions                     |
| SP10               | FscP                  | Maximum SCK2 Frequency                        | —                                                                                                                                                                       | —                   | 9    | MHz   | -40°C to +125°C<br>(Note 3)    |
| SP20               | TscF                  | SCK2 Output Fall Time                         | —                                                                                                                                                                       | —                   | —    | ns    | See Parameter DO32<br>(Note 4) |
| SP21               | TscR                  | SCK2 Output Rise Time                         | —                                                                                                                                                                       | —                   | —    | ns    | See Parameter DO31<br>(Note 4) |
| SP30               | TdoF                  | SDO2 Data Output Fall Time                    | —                                                                                                                                                                       | —                   | —    | ns    | See Parameter DO32<br>(Note 4) |
| SP31               | TdoR                  | SDO2 Data Output Rise Time                    | —                                                                                                                                                                       | —                   | —    | ns    | See Parameter DO31<br>(Note 4) |
| SP35               | Tsch2doV,<br>TscL2doV | SDO2 Data Output Valid after<br>SCK2 Edge     | —                                                                                                                                                                       | 6                   | 20   | ns    |                                |
| SP36               | TdoV2scH,<br>TdoV2scL | SDO2 Data Output Setup to<br>First SCK2 Edge  | 30                                                                                                                                                                      | —                   | —    | ns    |                                |
| SP40               | TdiV2scH,<br>TdiV2scL | Setup Time of SDI2 Data<br>Input to SCK2 Edge | 30                                                                                                                                                                      | —                   | —    | ns    |                                |
| SP41               | Tsch2diL,<br>TscL2diL | Hold Time of SDI2 Data Input<br>to SCK2 Edge  | 30                                                                                                                                                                      | —                   | —    | ns    |                                |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

FIGURE 32-5: TYPICAL  $I_{PD}$  CURRENT @  $V_{DD} = 3.3V$

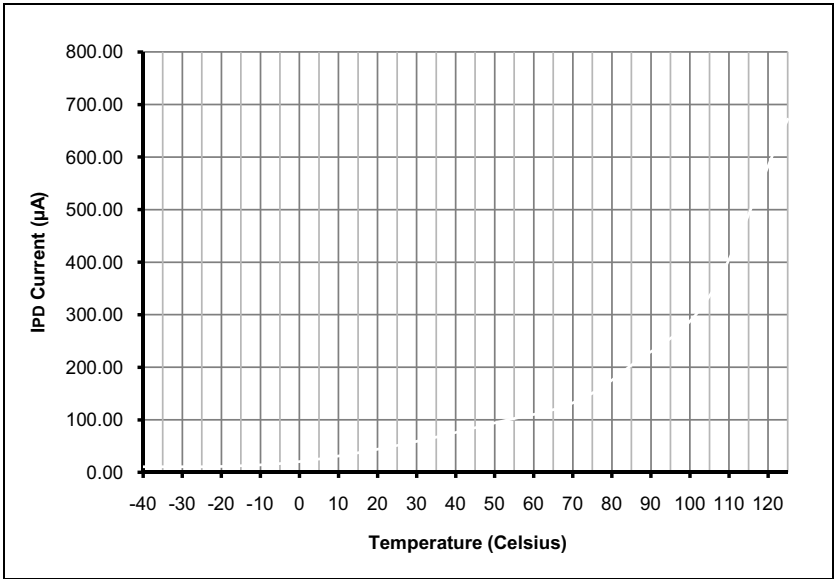


FIGURE 32-6: TYPICAL/MAXIMUM  $I_{DD}$  CURRENT @  $V_{DD} = 3.3V$

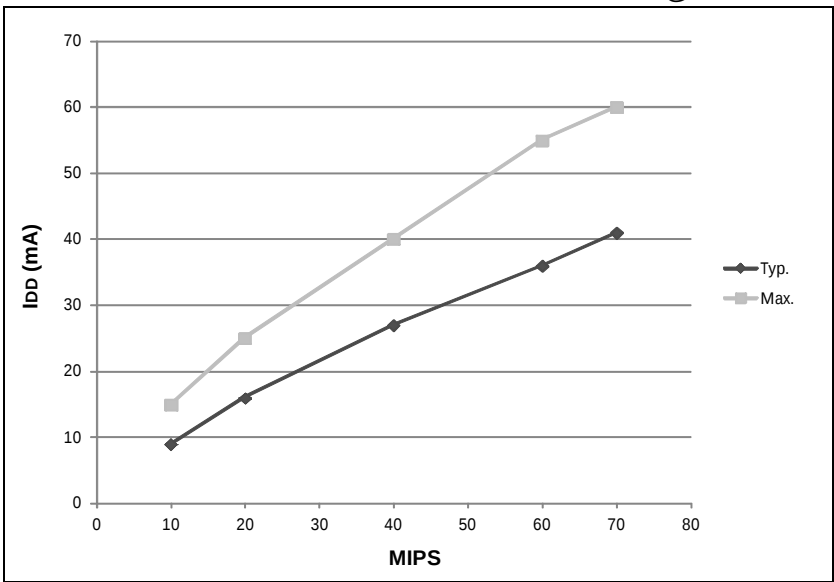


FIGURE 32-7: TYPICAL  $I_{DOZE}$  CURRENT @  $V_{DD} = 3.3V$

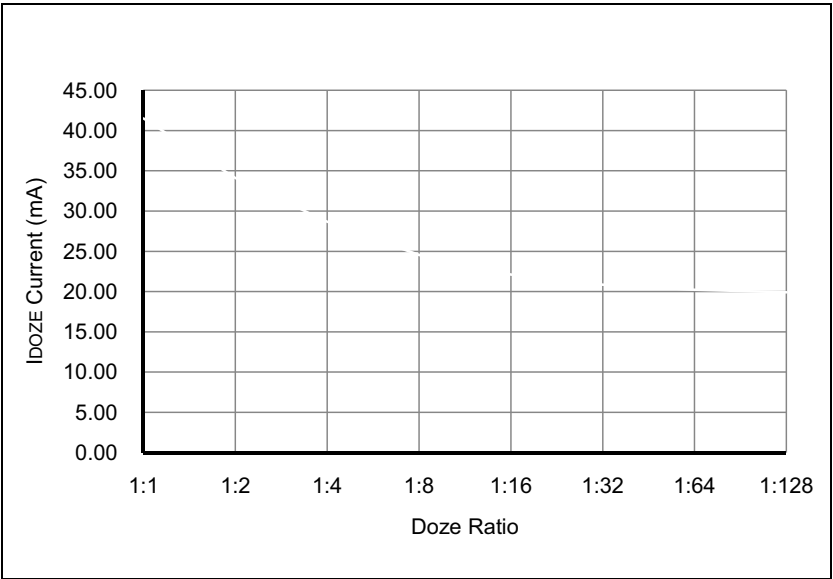
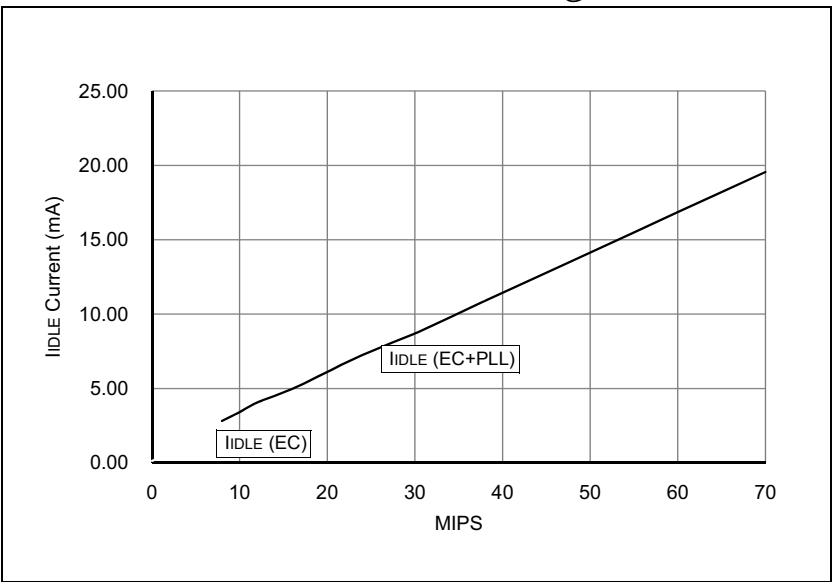
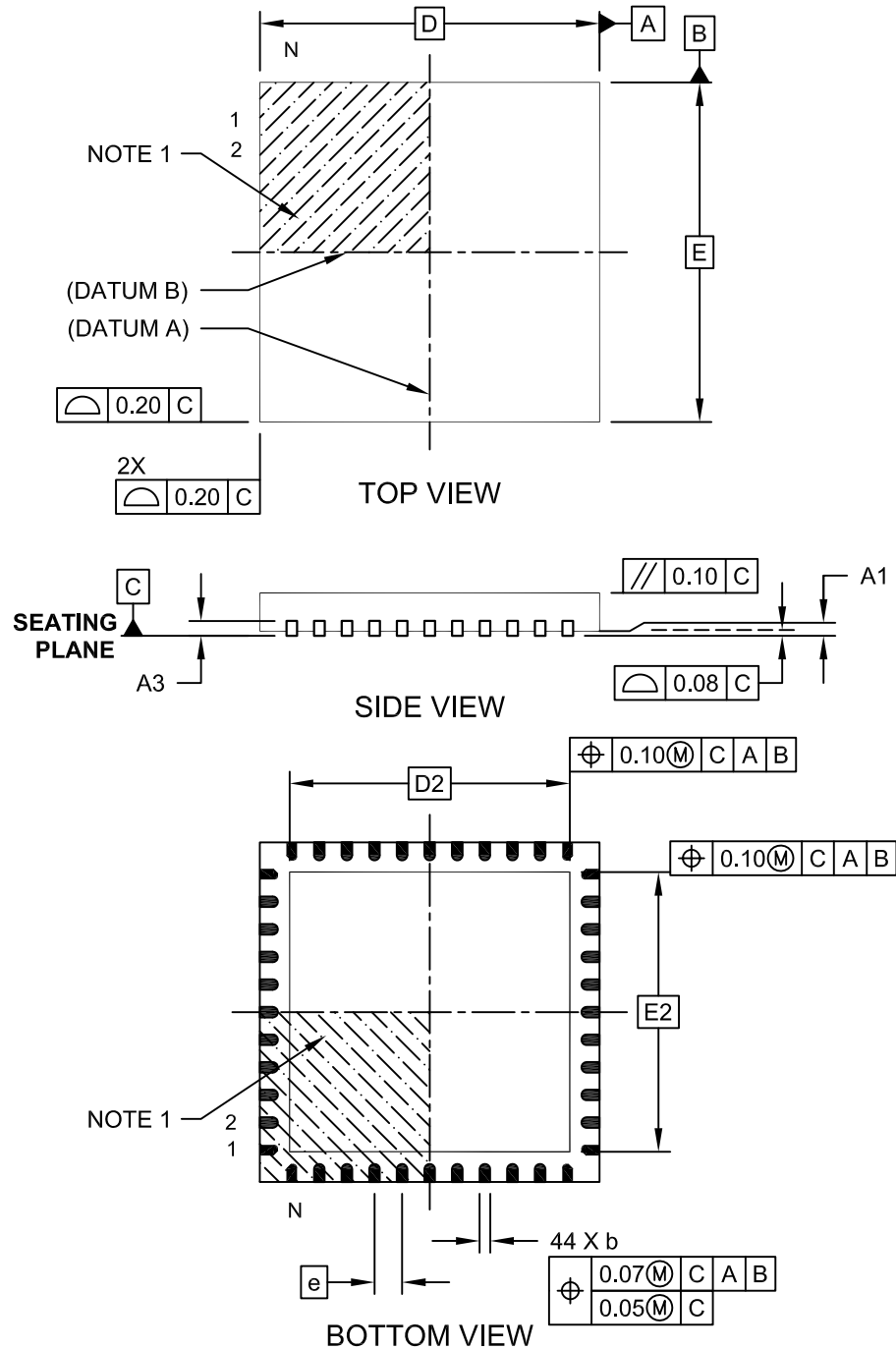


FIGURE 32-8: TYPICAL  $I_{IDLE}$  CURRENT @  $V_{DD} = 3.3V$



## 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-103C Sheet 1 of 2

**Revision D (December 2011)**

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

**TABLE A-3: MAJOR SECTION UPDATES**

| Section Name                                                                                                                                                | Update Description                                                                                                                                                                                                                                                                                                                                                                                  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>“16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High-Speed PWM, Op amps, and Advanced Analog”</b> | Removed the Analog Comparators column and updated the Op amps/Comparators column in Table 1 and Table 2.                                                                                                                                                                                                                                                                                            |
| <b>Section 21.0 “Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)”</b>                                                                       | Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).                                                                                                                                                                                                                                                                                                   |
| <b>Section 30.0 “Electrical Characteristics”</b>                                                                                                            | Updated the VBOR specifications and/or its related note in the following electrical characteristics tables: <ul style="list-style-type: none"><li>• Table 30-1</li><li>• Table 30-4</li><li>• Table 30-12</li><li>• Table 30-14</li><li>• Table 30-15</li><li>• Table 30-16</li><li>• Table 30-56</li><li>• Table 30-57</li><li>• Table 30-58</li><li>• Table 30-59</li><li>• Table 30-60</li></ul> |

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NOTES: