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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
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3.5 **Programmer's Model**

The programmer's model for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X is shown in Figure 3-2. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/

MC20X devices contain control registers for Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only), Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only) and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory mapped, as shown in Table 4-1.

Register(s) Name	Description
W0 through W15	Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
DSWPAG	Extended Data Space (EDS) Write Page Register
RCOUNT	REPEAT Loop Count Register
DCOUNT ⁽¹⁾	DO Loop Count Register
DOSTARTH ^(1,2) , DOSTARTL ^(1,2)	DO Loop Start Address Register (High and Low)
DOENDH ⁽¹⁾ , DOENDL ⁽¹⁾	DO Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Note 1: This register is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

2: The DOSTARTH and DOSTARTL registers are read-only.

TABLE 4-45: DMAC REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DMA0CON	0B00	CHEN	SIZE	DIR	HALF	NULLW		_	_	—	—	AMOD	E<1:0>	—	—	MODE	E<1:0>	0000
DMA0REQ	0B02	FORCE	_	-	_	-	_	-	_				IRQSEL	<7:0>				00FF
DMA0STAL	0B04								STA<1	5:0> 00							0000	
DMA0STAH	0B06	_	_	_		_	_	_	_	STA<23:16> 00							0000	
DMA0STBL	0B08								STB<1	5:0>								0000
DMA0STBH	0B0A	_	_	-		-	—	—	—	STB<23:16>						0000		
DMA0PAD	0B0C								PAD<1	5:0>								0000
DMA0CNT	0B0E	—	—							CNT<1	3:0>							0000
DMA1CON	0B10	CHEN	SIZE	DIR	HALF	NULLW	_	—	_	—	_	AMOD	E<1:0>	_	—	MODE	=<1:0>	0000
DMA1REQ	0B12	FORCE	_	_	_	_		_	_				IRQSEL	<7:0>				00FF
DMA1STAL	0B14								STA<1	5:0>								0000
DMA1STAH	0B16	_	—	_		_		—	_				STA<2	3:16>				0000
DMA1STBL	0B18								STB<1	5:0>								0000
DMA1STBH	0B1A	—	—	_		—		-	—				STB<2	3:16>				0000
DMA1PAD	0B1C								PAD<1	5:0>								0000
DMA1CNT	0B1E		_							CNT<1	3:0>							0000
DMA2CON	0B20	CHEN	SIZE	DIR	HALF	NULLW		-	—	—	_	AMOD	E<1:0>	—	—	MODE	=<1:0>	0000
DMA2REQ	0B22	FORCE	—	_		_		—	_				IRQSEL	_<7:0>				00FF
DMA2STAL	0B24								STA<1	5:0>								0000
DMA2STAH	0B26	—	—	—		—	_	—	—				STA<2	3:16>				0000
DMA2STBL	0B28								STB<1	5:0>								0000
DMA2STBH	0B2A	—	_	_		—		—	_				STB<2	3:16>				0000
DMA2PAD	0B2C								PAD<1	5:0>								0000
DMA2CNT	0B2E	—	_							CNT<1	3:0>							0000
DMA3CON	0B30	CHEN	SIZE	DIR	HALF	NULLW	_	—	—	—	—	AMOD	E<1:0>	—	—	MODE	E<1:0>	0000
DMA3REQ	0B32	FORCE	—	—		—	_	—	_				IRQSEL	_<7:0>				00FF
DMA3STAL	0B34								STA<1	5:0>								0000
DMA3STAH	0B36	—	—	—	—	—	—	—	—				STA<2	3:16>				0000
DMA3STBL	0B38								STB<1	5:0>								0000
DMA3STBH	0B3A	—	_	-		_		_	_				STB<2	3:16>				0000
DMA3PAD	0B3C								PAD<1	5:0>								0000
DMA3CNT	0B3E	—	—							CNT<1	3:0>							0000
DMAPWC	0BF0	—	_	-		_		_	_	-	_	—	_	PWCOL3	PWCOL2	PWCOL1	PWCOL0	0000
DMARQC	0BF2	—	_	—		—	_	—	—	—	—	—	—	RQCOL3	RQCOL2	RQCOL1	RQCOL0	0000
DMAPPS	0BF4	—	—	—		—	_	—	—	—	—	_	—	PPST3	PPST2	PPST1	PPST0	0000
DMALCA	0BF6	_	_	—		_	_	_		_		_			LSTCH	<3:0>		000F
DSADRL	0BF8								DSADR<	15:0>								0000
DSADRH	0BFA	_	_	_	_	_	_	_	_				DSADR<	:23:16>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-59: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00		—	—				—			—		TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	001F
PORTA	0E02		—	_		_		—			—		RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04		—	—				—			—		LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06		—	—				—			—		ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08		—	—				—			—		CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A		—	—				—			—		CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C		—	—				—			—		CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	-	—	—			-	—		_	_		ANSA4	_	—	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-60: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E			_	-	—	—	—	ANSB8		_	—		ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- · Register Indirect
- · Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal
- Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

4.6 Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.6.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified, and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Y space Modulo Addressing EA calcula-
	tions assume word-sized data (LSb of
	every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.6.2 W ADDRESS REGISTER SELECTION

The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '1111' and the XMODEN bit is set (MODCON<15>).

The Y Address Space Pointer W register (YWM), to which Modulo Addressing is to be applied, is stored in MODCON<7:4>. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '1111' and the YMODEN bit is set at MODCON<14>.



FIGURE 4-20: MODULO ADDRESSING OPERATION EXAMPLE

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
_	—	—	—	—	—	—	—	
bit 15							bit 8	
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	
—	_	—	—	PWCOL3	PWCOL2	PWCOL1	PWCOL0	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'		
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown		
bit 15-4	Unimplemen	ted: Read as '	0'					
bit 3	PWCOL3: DN	VA Channel 3 F	Peripheral Wri	te Collision Fla	ag bit			
	1 = Write col	lision is detecte	ed					
	0 = No write	collision is dete	ected					
bit 2	PWCOL2: DN	MA Channel 2 I	Peripheral Wri	te Collision Fla	ag bit			
	1 = Write col	lision is detecte	ed					
	0 = No write	collision is dete	ected					
bit 1	PWCOL1: DN	MA Channel 1 F	Peripheral Wri	te Collision Fla	ag bit			
	1 = Write col	lision is detecte	ed					
h:+ 0					h-14			
DIT U			Peripheral vvri	te Collision Fla	ag dit			
	$\perp = \text{VVrite COI}$	collision is detected	eted					

REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	—	_	_	_	—
bit 15		L	I	4			bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				INT2R<6:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown
-n = Value at F bit 15-7	POR Unimplemen	<pre>'1' = Bit is set ted: Read as '0</pre>	0'	ʻ0' = Bit is cle	ared	x = Bit is unkr	iown
-n = Value at F bit 15-7 bit 6-0	Unimplement INT2R<6:0>: (see Table 11-	'1' = Bit is set ted: Read as '0 Assign Externa -2 for input pin)' al Interrupt 2 (selection nun	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	POR Unimplement INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '0 Assign Externa -2 for input pin uput tied to RPI	o' al Interrupt 2 (selection nun 121	'0' = Bit is cle (INT2) to the C nbers)	ared	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	OR Unimplemen INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '(Assign Externa -2 for input pin put tied to RPI	o' al Interrupt 2 (selection nun 121	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	POR Unimplement INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '0 Assign Externa 2 for input pin uput tied to RPI	o' al Interrupt 2 (selection nun 121	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	POR Unimplement INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '0 Assign Externa 2 for input pin put tied to RPI	o' al Interrupt 2 (selection nun 121 P1	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	Unimplement INT2R<6:0>: (see Table 11- 1111001 = In 0000001 = In 0000000 = In	'1' = Bit is set ted: Read as '0 Assign Externa 2 for input pin put tied to RPI put tied to CMI put tied to Vss	o' al Interrupt 2 (selection nun 121 P1	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr	iown

REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_		_				_
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				T2CKR<6:0>			
bit 7							bit 0
Legend:							
R = Readabl	le bit	W = Writable I	bit	U = Unimplem	nented bit, read	as '0'	
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own
bit 15-7	Unimplemen	ted: Read as 'o)'				
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11	ted: Read as '(: Assign Timer2 -2 for input pin)' 2 External Clo selection nur	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as '(: Assign Timer2 -2 for input pin nput tied to RPI) [;] 2 External Clo selection nur 121	ock (T2CK) to th nbers)	ie Correspondii	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as '(: Assign Timer2 -2 for input pin nput tied to RPI) [;] 2 External Clo selection nur 121	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as ' : Assign Timer2 -2 for input pin nput tied to RPI)' 2 External Cle selection nur 121	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as 'c : Assign Timer2 -2 for input pin nput tied to RPI)' 2 External Clo selection nur 121 P1	ock (T2CK) to th nbers)	le Correspondi	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir 0000001 = Ir 0000000 = Ir	ted: Read as '(: Assign Timer2 -2 for input pin nput tied to RPI nput tied to CMI nput tied to Vss)' 2 External Clo selection nur 121 P1	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits	

NOTES:

16.3 PWMx Control Registers

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU ⁽¹⁾	SYNCPOL ⁽¹⁾	SYNCOEN ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN ⁽¹⁾	SYNCSRC2 ⁽¹⁾	SYNCSRC1 ⁽¹⁾	SYNCSRC0 ⁽¹⁾	SEVTPS3(1)	SEVTPS2 ⁽¹⁾	SEVTPS1 ⁽¹⁾	SEVTPS0 ⁽¹⁾
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	PTEN: PWMx Module Enable bit
	 1 = PWMx module is enabled 0 = PWMx module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	PTSIDL: PWMx Time Base Stop in Idle Mode bit
	 1 = PWMx time base halts in CPU Idle mode 0 = PWMx time base runs in CPU Idle mode
bit 12	SESTAT: Special Event Interrupt Status bit
	 1 = Special event interrupt is pending 0 = Special event interrupt is not pending
bit 11	SEIEN: Special Event Interrupt Enable bit
	1 = Special event interrupt is enabled
	0 = Special event interrupt is disabled
bit 10	EIPU: Enable Immediate Period Updates bit ⁽¹⁾
	 1 = Active Period register is updated immediately 0 = Active Period register updates occur on PWMx cycle boundaries
bit 9	SYNCPOL: Synchronize Input and Output Polarity bit ⁽¹⁾
	1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
	0 = SYNCI1/SYNCO1 is active-high
bit 8	SYNCOEN: Primary Time Base Sync Enable bit ⁽¹⁾
	1 = SYNCO1 output is enabled
L:1 7	0 = SYNCOT output is disabled
DIT /	SYNCEN: External Time Base Synchronization Enable bit
	1 = External synchronization of primary time base is enabled
Note 1:	These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user
	application must program the period register with a value that is slightly larger than the expected period of

the external synchronization input signal.

2: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Quadrature Encoder Interface (QEI)" (DS70601) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High register
- 32-Bit Position Compare Low register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXH	LD<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXH	HLD<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkı	nown

REGISTER 17-10: INDX1HLD: INDEX COUNTER 1 HOLD REGISTER

bit 15-0 INDXHLD<15:0>: Hold Register for Reading and Writing INDX1CNTH bits

REGISTER 17-11: QEI1ICH: QEI1 INITIALIZATION/CAPTURE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIIC	<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIIC	<23:16>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit			x = Bit is unkr	nown			
1							

bit 15-0 **QEIIC<31:16>:** High Word Used to Form 32-Bit Initialization/Capture Register (QEI1IC) bits

REGISTER 17-12: QEI1ICL: QEI1 INITIALIZATION/CAPTURE LOW WORD REGISTER

QEIIC<15:8> bit 15 bit 15 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 QEIIC<7:0> bit 7 bit 7 bit 7	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
bit 15 b R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 QEIIC<7:0> b b Legend: W = Writable bit U = Unimplemented bit read as '0'				QEII	C<15:8>			
R/W-0 R/W-0 <th< td=""><td>bit 15</td><td></td><td></td><td></td><td></td><td></td><td></td><td>bit 8</td></th<>	bit 15							bit 8
R/W-0 R/W-0 <th< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></th<>								
QEIIC<7:0> bit 7 Legend: R = Readable bit W = Writable bit	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
bit 7 b Legend: W = Writable bit B = Readable bit W = Writable bit				QEII	C<7:0>			
Legend: R = Readable bit W = Writable bit U = Unimplemented bit read as '0'	bit 7							bit 0
R = Readable bit W = Writable bit U = Unimplemented bit read as '0'								
R = Readable bit $W = Writable bit$ $U = Unimplemented bit read as '0'$	Legend:							
	R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown	-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown

bit 15-0 **QEIIC<15:0>:** Low Word Used to Form 32-Bit Initialization/Capture Register (QEI1IC) bits

19.1 I²C Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

19.1.1 KEY RESOURCES

- "Inter-Integrated Circuit (I²C)" (DS70330) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER (CONTINUED)

- bit 1 **RBIF:** RX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 **TBIF:** TX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred

26.3 Programmable CRC Registers

REGISTER 26-1: CRCCON1: CRC CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0			
CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0			
bit 15							bit 8			
R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0			
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	_	—			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown			
bit 15	CRCEN: CRC 1 = CRC mod 0 = CRC mod SFRs are	C Enable bit dule is enablec dule is disable not reset	l d; all state ma	ichines, pointe	rs and CRCWD	AT/CRCDAT a	re reset, other			
bit 14	Unimplemen	ted: Read as '	0'							
bit 13	CSIDL: CRC	Stop in Idle Mo	ode bit							
	1 = Discontin 0 = Continue	ues module op s module oper	peration when ation in Idle m	device enters lode	Idle mode					
bit 12-8	VWORD<4:0	>: Pointer Valu	e bits							
	Indicates the or 16 when Pl	number of value $LEN<4:0> \le 7.$	d words in the	FIFO. Has a n	naximum value	of 8 when PLE	N<4:0> > 7			
bit 7	CRCFUL: CR	C FIFO Full bi	t							
	1 = FIFO is fu	ll l								
		ot full								
DIT 6	1 = FIFO is e	C FIFO Empty	/ Bit							
	0 = FIFO is n	ot empty								
bit 5	CRCISEL: CF	RC Interrupt Se	election bit							
	 1 = Interrupt on FIFO is empty; final word of data is still shifting through CRC 0 = Interrupt on shift is complete and CRCWDAT results are ready 									
bit 4	CRCGO: Start CRC bit									
	 1 = Starts CRC serial shifter 0 = CRC serial shifter is turned off 									
bit 3	LENDIAN: Da	ata Word Little-	Endian Config	guration bit						
	1 = Data wor 0 = Data wor	d is shifted into d is shifted into	o the CRC star o the CRC star	rting with the L rting with the M	Sb (little endiar ISb (big endian	1))				
bit 2-0	Unimplemented: Read as '0'									

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
		—	DWIDTH4	DWIDTH3	DWIDTH2	DWIDTH1	DWIDTH0	
bit 15							bit 8	
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
		—	PLEN4	PLEN3	PLEN2	PLEN1	PLEN0	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown	
bit 15-13	Unimplemen	ted: Read as '	0'					
bit 12-8	DWIDTH<4:0	>: Data Width	Select bits					
	These bits set the width of the data word (DWIDTH<4:0> + 1).							
bit 7-5	bit 7-5 Unimplemented: Read as '0'							

REGISTER 26-2: CRCCON2: CRC CONTROL REGISTER 2

bit 4-0 **PLEN<4:0>:** Polynomial Length Select bits

These bits set the length of the polynomial (Polynomial Length = PLEN<4:0> + 1).

30.2 AC Characteristics and Timing Parameters

This section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X AC characteristics and timing parameters.

TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

	Standard Operating Conditions: 3.0V to 3.6V				
	(unless otherwise stated)				
	Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial				
AC CHARACTERISTICS	$-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
	Operating voltage VDD range as described in Section 30.1 "DC				
	Characteristics".				

FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
DO50	Cosco	OSC2 Pin	_	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	Сю	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	Св	SCLx, SDAx	_		400	pF	In I ² C™ mode

FIGURE 30-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS



TABLE 30-27: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min. Typ. Max. Units Conditions				Conditions	
OC10	TccF	OCx Output Fall Time	—			ns	See Parameter DO32	
OC11	TccR	OCx Output Rise Time	— — — ns See Parameter DO31					

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: OCx/PWMx MODULE TIMING CHARACTERISTICS



TABLE 30-28: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min. Typ. Max. Units Conditions					
OC15	TFD	Fault Input to PWMx I/O Change	—	_	Tcy + 20	ns		
OC20	TFLT	Fault Input Pulse Width	Tcy + 20		—	ns		

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 30-46:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)TIMING REQUIREMENTS

АС СНА	ARACTERIS	TICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	FscP	Maximum SCK1 Input Frequency	—	—	Lesserof FP or 11	MHz	(Note 3)	
SP72	TscF	SCK1 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK1 Input Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO1 Data Output Rise Time	—	-	—	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	-	—	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	-	—	ns		
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns		
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)	
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	—	ns	(Note 4)	
SP60	TssL2doV	SDO1 Data Output Valid after SS1 Edge	—	_	50	ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

TABLE 31-11: INTERNAL RC ACCURACY

AC CH	ARACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$							
Param No.	Characteristic	Min	Тур	Max	Units	Conditions			
	LPRC @ 32.768 kHz ^(1,2)								
HF21	LPRC	-30	_	+30	%	$-40^{\circ}C \le TA \le +150^{\circ}C VDD = 3.0-3.6V$			

Note 1: Change of LPRC frequency as VDD changes.

2: LPRC accuracy impacts the Watchdog Timer Time-out Period (TwDT). See Section 27.5 "Watchdog Timer (WDT)" for more information.