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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFI

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gp504t-e-pt

Email: info@E-XFL.COM

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# 2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS AND MICROCONTROLLERS

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Familv Reference Manual", which is available from the Microchip web site (www.microchip.com)
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

# 2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and Vss pins (see Section 2.2 "Decoupling Capacitors")
- All AVDD and AVss pins (regardless if ADC module is not used)

(see Section 2.2 "Decoupling Capacitors")
• VCAP

(see Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)")

- MCLR pin (see Section 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins used for In-Circuit Serial Programming<sup>™</sup> (ICSP<sup>™</sup>) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used

(see Section 2.6 "External Oscillator Pins")

Additionally, the following pins may be required:

• VREF+/VREF- pins are used when external voltage reference for the ADC module is implemented

Note: The AVDD and AVSS pins must be connected, independent of the ADC voltage reference source.

# 2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: Recommendation of 0.1  $\mu$ F (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- Handling high-frequency noise: If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of  $0.01 \ \mu\text{F}$  to  $0.001 \ \mu\text{F}$ . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example,  $0.1 \ \mu\text{F}$  in parallel with  $0.001 \ \mu\text{F}$ .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.





File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	<b>INT0IF</b>	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	_	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—		—		_	—	—	-	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	_		—		QEI1IF	PSEMIF	—		—		—		MI2C2IF	SI2C2IF		0000
IFS4	0808	_	_	CTMUIF	_		—	_	_		C1TXIF		_	CRCIF	U2EIF	U1EIF		0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	_	—	—	—	_	—	—	_	0000
IFS6	080C	—	—	—	—	—	—	—	—	_	—	—	—	_	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF		_		—	_	_		_		_		—	—		0000
IFS9	0812	_	_		_		—	_	_		PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF		0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	_	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	_	IC4IE	IC3IE	<b>DMA3IE</b>	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	QEI1IE	PSEMIE	—	_	—	—	—	_	MI2C2IE	SI2C2IE	_	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	_	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	_	0000
IEC5	082A	PWM2IE	PWM1IE	_	—	_	—	—	—	_	—	_	—	_	_	—	_	0000
IEC6	082C	—	—	_	—	_	—	—	—	_	—	_	—	_	_	—	PWM3IE	0000
IEC7	082E	—	—	_	—	_	—	—	—	_	—	_	—	_	—	—	_	0000
IEC8	0830	JTAGIE	ICDIE	_	—	_	—	—	—	_	—	_	—	_	—	—	_	0000
IEC9	0832	—	—	_	—	_	—		—	_	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	_	0000
IPC0	0840	—		T1IP<2:0>		_		OC1IP<2:0	)>	_		IC1IP<2:0>		_		INT0IP<2:0>		4444
IPC1	0842	—		T2IP<2:0>		_		OC2IP<2:0	)>	_		IC2IP<2:0>		_	1	DMA0IP<2:0>		4444
IPC2	0844	—		U1RXIP<2:0	)>	_		SPI1IP<2:0	)>	_		SPI1EIP<2:0	>	_		T3IP<2:0>		4444
IPC3	0846	—	—	_	—	_	0	)MA1IP<2:	0>	_		AD1IP<2:0>		_		U1TXIP<2:0>		0444
IPC4	0848			CNIP<2:0>		_		CMIP<2:0	>			MI2C1IP<2:0	>	_	:	SI2C1IP<2:0>		4444
IPC5	084A	—	—	_	—	_	—		—	_	—	_	—	_		INT1IP<2:0>		0004
IPC6	084C	—		T4IP<2:0>		_		OC4IP<2:0	)>	_		OC3IP<2:0>		_	1	DMA2IP<2:0>		4444
IPC7	084E	—		U2TXIP<2:0	>	_	ι	J2RXIP<2:(	0>	_		INT2IP<2:0>		_		T5IP<2:0>		4444
IPC8	0850	—		C1IP<2:0>	-	_	0	C1RXIP<2:(	0>	_		SPI2IP<2:0>		_		SPI2EIP<2:0>		4444
IPC9	0852	—	—	_	—	_		IC4IP<2:0	>	_		IC3IP<2:0>		_	1	DMA3IP<2:0>		0444
IPC12	0858	—	—	_	—	_	N	112C2IP<2:	0>	_		SI2C2IP<2:0	>	_	—	—	_	0440
IPC14	085C	—	_	—	—	—	(	QEI1IP<2:0	)>	_		PSEMIP<2:0	>	—	—	—	—	0440
IPC16	0860	_		CRCIP<2:0	>	_		U2EIP<2:0	>	_		U1EIP<2:0>		_	_	_	_	4440
IPC17	0862	_	—	_	—	_	(	C1TXIP<2:0	0>	_	—	—	—	_	_	_	_	0400
IPC19	0866	—	—	_	—	_	—	—	—	_		CTMUIP<2:0	>	_	—	—	—	0040

### TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

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# 4.6 Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

### 4.6.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified, and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Y space Modulo Addressing EA calcula-
	tions assume word-sized data (LSb of
	every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

#### 4.6.2 W ADDRESS REGISTER SELECTION

The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '1111' and the XMODEN bit is set (MODCON<15>).

The Y Address Space Pointer W register (YWM), to which Modulo Addressing is to be applied, is stored in MODCON<7:4>. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '1111' and the YMODEN bit is set at MODCON<14>.



### FIGURE 4-20: MODULO ADDRESSING OPERATION EXAMPLE

## 6.1 Reset Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

#### 6.1.1 KEY RESOURCES

- "Reset" (DS70602) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STB<	23:16>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown

#### REGISTER 8-5: DMAXSTBH: DMA CHANNEL X START ADDRESS REGISTER B (HIGH)

bit 15-8 Unimplemented: Read as '0'

bit 7-0 STB<23:16>: Secondary Start Address bits (source or destination)

#### REGISTER 8-6: DMAXSTBL: DMA CHANNEL X START ADDRESS REGISTER B (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STE	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			ST	3<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	mented bit, rea	id as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 **STB<15:0>:** Secondary Start Address bits (source or destination)

#### 10.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- · Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into Standby when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

#### 10.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- · The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see Section 10.4 "Peripheral Module Disable").
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- · Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction or the first instruction in the Interrupt Service Routine (ISR).

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the TSIDL bit in the Timer1 Control register (T1CON<13>).

#### 10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

### REGISTER 11-9: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				HOME1R<6:0	>		
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				INDX1R<6:0>	>		
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	Unimpleme	ented: Read as '	0'				
bit 15 bit 14-8	HOME1R<6	5:0>: Assign QEI	0 1 HOME1 (H selection nun	OME1) to the C	Corresponding	RPn Pin bits	
	1111001 =	Input tied to RPI	121	,			
		Input tied to CM	D1				
	0000000 =	Input tied to Vss	;				
bit 7	Unimpleme	ented: Read as '	0'				
bit 6-0	IND1XR<6: (see Table 2	<b>0&gt;:</b> Assign QEI1 I1-2 for input pin	INDEX1 (INE selection nun	0X1) to the Cor nbers)	responding R	Pn Pin bits	
	1111001 =	Input tied to RPI	121	,			
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss					

# 12.2 Timer1 Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON <sup>(1)</sup>	—	TSIDL	—	_	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	TCKPS1	TCKPS0	_	TSYNC <sup>(1)</sup>	TCS <sup>(1)</sup>	—
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own
		(1)					
bit 15	TON: Timer1	On bit <sup>(1)</sup>					
	1 = Starts 16-	bit Limer1 bit Timer1					
bit 1/	Unimplement	ted: Pead as '	ı'				
bit 13		1 Stop in Idle N	/ode hit				
DIC 15	1 = Discontinu	i stop in lae k	eration when a	device enters l	dle mode		
	0 = Continues	module opera	tion in Idle mo	ode			
bit 12-7	Unimplement	ted: Read as '	)'				
bit 6	TGATE: Time	r1 Gated Time	Accumulation	Enable bit			
	When TCS =	<u>1:</u> prod					
	When TCS =	0. 0.					
	1 = Gated tim	<u>e</u> accumulatior	n is enabled				
	0 = Gated tim	e accumulatior	n is disabled				
bit 5-4	TCKPS<1:0>	: Timer1 Input	Clock Prescal	e Select bits			
	11 = 1:256						
	10 = 1:64 01 = 1:8						
	01 = 1.0 00 = 1.1						
bit 3	Unimplement	ted: Read as '	)'				
bit 2	TSYNC: Time	er1 External Clo	ock Input Sync	chronization Se	elect bit <sup>(1)</sup>		
	When TCS =	1:					
	1 = Synchroni	izes external cl	ock input				
	0 = Does not	synchronize ex	ternal clock in	nput			
	This bit is jand	<u>ored</u> .					
bit 1	TCS: Timer1 (	Clock Source S	Select bit <sup>(1)</sup>				
	1 = External c	lock is from pir	n, T1CK (on th	ne rising edge)			
	0 = Internal cl	ock (FP)		5 5-7			
bit 0	Unimplement	ted: Read as '	)'				
Note 1: \	When Timer1 is en attempts by user so	abled in Exterr oftware to write	al Synchrono to the TMR1	us Counter mo register are ig	ode (TCS = 1, T nored.	SYNC = 1, TO	N = 1), any

## REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

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#### REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER (CONTINUED)

- bit 2 INDEX: Status of INDXx Input Pin After Polarity Control
  - 1 = Pin is at logic '1'
  - 0 = Pin is at logic '0'
- bit 1 QEB: Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1' 0 = Pin is at logic '0'
- bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1'
  - 0 = Pin is at logic '0'

# 21.2 Modes of Operation

The ECAN module can operate in one of several operation modes selected by the user. These modes include:

- · Initialization mode
- Disable mode
- Normal Operation mode
- · Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

#### 21.3 ECAN Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

#### 21.3.1 KEY RESOURCES

- "Enhanced Controller Area Network (ECAN™)" (DS70353) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- · Development Tools

# 23.4 ADC Control Registers

#### REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0
bit 15						-	bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC, HS	R/C-0, HC, HS
SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE <sup>(3)</sup>
bit 7						-	bit 0
Legend:		HC = Hardwa	re Clearable bit	HS = Hardwa	re Settable bit	C = Clearable bi	t
R = Readab	le bit	W = Writable I	bit	U = Unimpler	nented bit, read	d as '0'	
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknow	vn
bit 15	ADON: ADO	C1 Operating N	lode bit				
	1 = ADC mo	odule is operati	ng				
	0 = ADC is	off					
bit 14	Unimpleme	ented: Read as	'0'				
bit 13	ADSIDL: AI	DC1 Stop in Idle	e Mode bit				
	1 = Disconti	inues module o	peration when	device enters	Idle mode		
	0 = Continu	es module ope	ration in Idle mo	ode			
bit 12	ADDMABM	: DMA Buffer E	Build Mode bit				
	1 = DMA b	uffers are writte	en in the order	of conversion	; the module p	provides an addre	ess to the DMA
	0 = DMA bi	uffers are writte	en in Scatter/Ga	ther mode: the	e module prov	ides a Scatter/Ga	ther address to
	the DM	A channel, bas	ed on the index	of the analog	input and the	size of the DMA	ouffer.
bit 11	Unimpleme	ented: Read as	'0'				
bit 10	<b>AD12B:</b> AD	C1 10-Bit or 12	2-Bit Operation	Mode bit			
	1 = 12-bit, 1	-channel ADC	operation				
	0 = 10-bit, 4	-channel ADC	operation				
bit 9-8	FORM<1:0	>: Data Output	Format bits				
	For 10-Bit C	Operation:					
	11 = Signed	d fractional (Do	UT = sddd ddd	ld dd00 000	0, where $s = $ .	NOT.d<9>)	
	10 = Fractions	hai (DOUT = ac	100 0000 000 = cccc cccd		where $c = N($	(<0>b T(	
	00 = Intege	r (Dout = 0000	00dd dddd	dddd)		51.u (0 <sup>2</sup> )	
	For 12-Bit C	Deration:		,			
	11 = Signed	fractional (Do	UT = sddd ddd	ld dddd 000	0, where $s = .$	NOT.d<11>)	
	10 = Fractic	onal (Dout = do	ldd dddd ddd	ld 0000)			
	00 = Intege	r (DOUT = 0.000)	- ssss sada ) dddd dddd	aaaa aaad, dddd)	where $s = .NC$	JI.U<112)	
		. (2001 - 0000		adduj			
Note 1: S	See Section 24	1.0 "Peripheral	l Trigger Gene	rator (PTG) M	odule" for info	ormation on this s	election.

- 2: This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 3: Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

### REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1 (CONTINUED)

bit 7-5	SSRC<2:0>: Sample Trigger Source Select bits
	If SSRCG = 1: 111 = Reserved 110 = PTGO15 primary trigger compare ends sampling and starts conversion <sup>(1)</sup> 101 = PTGO14 primary trigger compare ends sampling and starts conversion <sup>(1)</sup> 100 = PTGO13 primary trigger compare ends sampling and starts conversion <sup>(1)</sup> 011 = PTGO12 primary trigger compare ends sampling and starts conversion <sup>(1)</sup> 010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion <sup>(2)</sup> 001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion <sup>(2)</sup> 000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion <sup>(2)</sup>
	If SSRCG = 0: 111 = Internal counter ends sampling and starts conversion (auto-convert) 110 = CTMU ends sampling and starts conversion 101 = Reserved
	<ul> <li>101 - Reserved</li> <li>100 = Timer5 compare ends sampling and starts conversion</li> <li>011 = PWM primary Special Event Trigger ends sampling and starts conversion</li> <li>010 = Timer3 compare ends sampling and starts conversion</li> <li>001 = Active transition on the INT0 pin ends sampling and starts conversion</li> <li>000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)</li> </ul>
bit 4	SSRCG: Sample Trigger Source Group bit
	See SSRC<2:0> for details.
bit 3	SIMSAM: Simultaneous Sample Select bit (only applicable when CHPS<1:0> = 01 or 1x) In 12-bit mode (AD21B = 1), SIMSAM is Unimplemented and is Read as '0': 1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS<1:0> = 1x); or samples CH0 and CH1 simultaneously (when CHPS<1:0> = 01) 0 = Samples multiple channels individually in sequence
bit 2	ASAM: ADC1 Sample Auto-Start bit
	<ul> <li>1 = Sampling begins immediately after the last conversion; SAMP bit is auto-set</li> <li>0 = Sampling begins when the SAMP bit is set</li> </ul>
bit 1	SAMP: ADC1 Sample Enable bit
	<ul> <li>1 = ADC Sample-and-Hold amplifiers are sampling</li> <li>0 = ADC Sample-and-Hold amplifiers are holding</li> <li>If ASAM = 0, software can write '1' to begin sampling. Automatically set by hardware if ASAM = 1. If SSRC&lt;2:0&gt; = 000, software can write '0' to end sampling and start conversion. If SSRC&lt;2:0&gt; ≠ 000, automatically cleared by hardware to end sampling and start conversion.</li> </ul>
bit 0	DONE: ADC1 Conversion Status bit <sup>(3)</sup>
	<ul> <li>1 = ADC conversion cycle has completed</li> <li>0 = ADC conversion has not started or is in progress</li> <li>Automatically set by hardware when the ADC conversion is complete. Software can write '0' to clear the DONE status bit (software is not allowed to write '1'). Clearing this bit does NOT affect any operation in progress. Automatically cleared by hardware at the start of a new conversion.</li> </ul>
Note 1:	See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

- 2: This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- **3:** Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, reac	l as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15-13 bit 12-8	PTGCLK<2:0 111 = Reserv 110 = Reserv 101 = PTG m 010 = PTG m 011 = PTG m 010 = PTG m 001 = PTG m 000 = PTG m PTGDIV<4:02	<ul> <li>Select PTG</li> <li>red</li> <li>odule clock so</li> </ul>	Source bits CLK CLK CLK D SSC S ler (divider) bi	ts			
	11111 = Divic 11110 = Divic • • • • • • • • • • • • • • • • • • •	de-by-32 de-by-31 de-by-2 de-by-1					
bit 7-4	PTGPWD<3:0	<b>0&gt;:</b> PTG Trigge	er Output Pulse	e-Width bits			
	<pre>1111 = All trigger outputs are 16 PTG clock cycles wide 1110 = All trigger outputs are 15 PTG clock cycles wide</pre>						
bit 3	Unimplemen	ted: Read as '	0'				
bit 2-0	PTGWDT<2:0	0>: Select PTG	Watchdog Tir	mer Time-out	Count Value bits	3	
	111 = Watcho 110 = Watcho 101 = Watcho 100 = Watcho 011 = Watcho 010 = Watcho 001 = Watcho 000 = Watcho	dog Timer will t dog Timer is dis	ime-out after 5 ime-out after 2 ime-out after 1 ime-out after 3 ime-out after 3 ime-out after 1 ime-out after 8 sabled	512 PTG clock 256 PTG clock 28 PTG clock 54 PTG clock 54 PTG clocks 52 PTG clocks 53 PTG clocks	S S S		

## REGISTER 24-2: PTGCON: PTG CONTROL REGISTER

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0
_	CVR2OE <sup>(1)</sup>	—	_	—	VREFSEL	—	—
bit 15							bit 8
R/W-0	D R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVRE	N CVR10E <sup>(1)</sup>	CVRR	CVRSS <sup>(2)</sup>	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0
Legend:							
R = Read	able bit	W = Writable bit U = Unimplemented H				as '0'	
-n = Value	e at POR	'1' = Bit is set	t	'0' = Bit is cle	eared	x = Bit is unkr	Iown
bit 15	Unimplemen	ted: Read as '	0'		(1)		
bit 14	CVR2OE: Co	mparator Volta	ige Reference	2 Output Ena	ble bit(")		
	1 = (AVDD - A 0 = (AVDD - A	AVSS)/2 is conr AVSS)/2 is disce	nected to the C	VREF20 pin the CVREF20	pin		
bit 13-11	Unimplemen	ted: Read as '	0'				
bit 10	VREFSEL: C	omparator Voli	age Reference	e Select bit			
	1 = CVREFIN :	= VREF+	-				
	0 = CVREFIN i	is generated by	y the resistor n	etwork			
bit 9-8	Unimplemen	ted: Read as '	0'				
bit 7	CVREN: Con	nparator Voltag	e Reference E	nable bit			
	1 = Compara	tor voltage refe	erence circuit is	s powered on	MD		
bit 6	CVR1OF: Co	CVP10F: Comparator Voltage Reference 1 Output Enable hit(1)					
bito	1 = Voltage le	evel is output o	n the CVRFF10				
	0 = Voltage le	evel is disconne	ected from the	n CVREF10 pi	n		
bit 5	CVRR: Comp	parator Voltage	Reference Ra	inge Selectior	n bit		
	1 = CVRSRC/2	24 step-size					
	0 = CVRSRC/3	32 step-size					
bit 4	CVRSS: Com	nparator Voltag	e Reference S	ource Selecti	on bit <sup>(2)</sup>		
	1 = Compara 0 = Compara	tor voltage refe tor voltage refe	erence source,	CVRSRC = (V CVRSRC = A)	REF+) – (AVSS) /dd – AVSS		
bit 3-0	<b>CVR&lt;3:0&gt;</b> Co	omparator Volt	age Reference	Value Select	ion $0 \leq CVR < 3$ :	$0> \le 15$ bits	
	When CVRR	= 1:					
	CVREFIN = (C	VR<3:0>/24) •	(CVRSRC)				
	When CVRR	= 0:					
	CVREFIN = (C	VRSRC/4) + (C	VR<3:0>/32) •	(CVRSRC)			
Note 1:	CVRxOE overrides	s the TRISx an	d the ANSELx	bit settings.			

#### REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

- 2: In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.

DC CHARACTERISTICS			$\begin{tabular}{ l l l l l l l l l l l l l l l l l l l$					
Param No.	Symbol	Characteristic	Min. Typ. Max. Units Conditions				Conditions	
Operati	Operating Voltage							
DC10	Vdd	Supply Voltage	3.0	_	3.6	V		
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	_	_	Vss	V		
DC17	Svdd	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.03	—	—	V/ms	0V-1V in 100 ms	

#### TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

### TABLE 30-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated):Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended							
Param No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Comments
	Cefc	External Filter Capacitor Value <sup>(1)</sup>	4.7	10	_	μF	Capacitor must have a low series resistance (< 1 Ohm)

**Note 1:** Typical VCAP voltage = 1.8 volts when VDD  $\geq$  VDDMIN.



#### FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X



#### FIGURE 30-34: ECAN<sub>x</sub> MODULE I/O TIMING CHARACTERISTICS

#### TABLE 30-51: ECANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			$ \begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \\ \end{array} $				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Тур. <sup>(2)</sup>	Max.	Units	Conditions
CA10	TIOF	Port Output Fall Time		_	_	ns	See Parameter DO32
CA11	TIOR	Port Output Rise Time	_	_	_	ns	See Parameter DO31
CA20	TCWF	Pulse Width to Trigger CAN Wake-up Filter	120			ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

#### **FIGURE 30-35: UARTX MODULE I/O TIMING CHARACTERISTICS**



#### TABLE 30-52: UARTX MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Тур. <sup>(2)</sup>	Max.	Units	Conditions
UA10	TUABAUD	UARTx Baud Time	66.67	_	_	ns	
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps	
UA20	TCWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	_	_	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

## 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Contact Pitch E		0.65 BSC			
Optional Center Pad Width	W2			6.60	
Optional Center Pad Length	T2			6.60	
Contact Pad Spacing	C1		8.00		
Contact Pad Spacing	C2		8.00		
Contact Pad Width (X44)	X1			0.35	
Contact Pad Length (X44)	Y1			0.85	
Distance Between Pads		0.25			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B

# APPENDIX A: REVISION HISTORY

# **Revision A (April 2011)**

This is the initial released version of the document.

## Revision B (July 2011)

This revision includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-1.

### TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers and Microcontrollers"	Changed all pin diagrams references of VLAP to TLA.
Section 4.0 "Memory Organization"	Updated the All Resets values for CLKDIV and PLLFBD in the System Control Register Map (see Table 4-35).
Section 5.0 "Flash Program Memory"	Updated "one word" to "two words" in the first paragraph of <b>Section 5.2 "RTSP Operation"</b> .
Section 9.0 "Oscillator Configuration"	Updated the PLL Block Diagram (see Figure 9-2). Updated the Oscillator Mode, Fast RC Oscillator (FRC) with divide-by-N and PLL (FRCPLL), by changing (FRCDIVN + PLL) to (FRCPLL).
	Changed (FRCDIVN + PLL) to (FRCPLL) for COSC<2:0> = 001 and NOSC<2:0> = 001 in the Oscillator Control Register (see Register 9-1).
	Changed the POR value from 0 to 1 for the DOZE<1:0> bits, from 1 to 0 for the FRCDIV<0> bit, and from 0 to 1 for the PLLPOST<0> bit; Updated the default definitions for the DOZE<2:0> and FRCDIV<2:0> bits and updated all bit definitions for the PLLPOST<1:0> bits in the Clock Divisor Register (see Register 9-2).
	Changed the POR value from 0 to 1 for the PLLDIV<5:4> bits and updated the default definitions for all PLLDIV<8:0> bits in the PLL Feedback Division Register (see Register 9-2).
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Updated the bit definitions for the IRNG<1:0> bits in the CTMU Current Control Register (see Register 22-3).
Section 25.0 "Op amp/ Comparator Module"	Updated the voltage reference block diagrams (see Figure 25-1 and Figure 25-2).