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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gp504t-i-mv

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FIGURE 2-7: INTERLEAVED PFC









4.5.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions. which apply to dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and the DSP accumulator class of instructions, which apply to the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.5.4 MAC INSTRUCTIONS (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X DEVICES ONLY)

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY. N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The Two-Source Operand Prefetch registers must be members of the set: {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the ${\tt MAC}$ class of instructions:

- · Register Indirect
- Register Indirect Post-Modified by 2
- · Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.5.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

7.0 INTERRUPT CONTROLLER

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP/MC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Interrupts" (DS70600) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 246 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit-wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/S-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
FORCE ⁽¹⁾	—	—	_	_	—	—	—		
bit 15		·			·		bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0		
bit 7		•			·		bit 0		
Legend:		S = Settable b	oit						
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'			
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	Iown		
bit 15	FORCE: Forc	e DMA Transfe	er bit ⁽¹⁾						
	1 = Forces a	single DMA tra	insfer (Manua	l mode)					
	0 = Automati	c DMA transfer	initiation by D	MA request					
bit 14-8	Unimplemen	ted: Read as '	י)						
bit 7-0	IRQSEL<7:0>	-: DMA Periphe	eral IRQ Numl	ber Select bits					
	01000110 =	ECAN1 – TX D	ata Request ⁽²	2)					
	00100110 =	IC4 – Input Caj	oture 4						
	00100101 =	IC3 – Input Ca	oture 3						
	00100010 =	ECAN1 – RX D	Data Ready(2)						
	00100001 = 3	SPIZ Transfer I	Jone NDT2 Transmi	ittor					
	00011111 =	UART2RX - U	ART2 Receive	ar					
	0001110 = 00011100 = 000011100 = 000011000 = 00000000	TMR5 – Timer	5						
	00011011 =	TMR4 – Timer4	1						
	00011010 =	OC4 – Output	Compare 4						
	00011001 =	OC3 – Output (Compare 3						
	00001101 =	ADC1 – ADC1	Convert done	•					
	00001100 =	UART1TX – U/	ART1 Transm	itter					
	00001011 =	UART1RX – U	ART1 Receive	er					
	00001010 =	SPI1 – Transfe	r Done						
	00001000 =	TMR3 – Timera	3						
	00000111 =	100RZ - 100RZ	<u>Compore 2</u>						
	00000110 = 0	IC2 – Duipui V	oture 2						
	00000101 = 0	OC1 = Outout 0	Compare 1						
	00000001 =	IC1 – Input Ca	oture 1						
	00000000 = INTO - External Interrupt O								

REGISTER 8-2: DMAXREQ: DMA CHANNEL x IRQ SELECT REGISTER

- **Note 1:** The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).
 - 2: This selection is available in dsPIC33EPXXXGP/MC50X devices only.

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON		ROSSLP	ROSEL	RODIV3 ⁽¹⁾	RODIV2 ⁽¹⁾	RODIV1 ⁽¹⁾	RODIV0 ⁽¹⁾
bit 15						•	bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
		<u> </u>				<u> </u>	
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	ROON: Refer	ence Oscillato	Output Enab	ole bit			
Sit 10	1 = Reference 0 = Reference	e oscillator outr e oscillator outr	but is enabled	on the REFCL	.K pin ⁽²⁾		
bit 14	Unimplemen	ted: Read as '	o'				
bit 13	ROSSLP: Re	ference Oscilla	tor Run in Sle	ep bit			
	1 = Reference	e oscillator outp	out continues	to run in Sleep			
	0 = Reference	e oscillator outp	out is disabled	l in Sleep			
bit 12	ROSEL: Refe	erence Oscillato	or Source Sel	ect bit			
	1 = Oscillator	crystal is used	as the refere	nce clock			
hit 11_8		Peference Os	cillator Divide	r hite(1)			
Dit 11-0	1111 = Refer	ence clock divi	ded by 32 76	R			
	1110 = Refer	ence clock divi	ded by 16,384	4			
	1101 = Refer	ence clock divi	ded by 8,192				
	1100 = Refer	ence clock divi	ded by 4,096				
	1011 = Refer	ence clock divi	ded by 2,048				
	1010 = Relef	ence clock divi	ded by 1,024 ded by 512				
	1000 = Refer	ence clock divi	ded by 256				
	0111 = Refer	ence clock divi	ded by 128				
	0110 = Refer	ence clock divi	ded by 64				
	0101 = Refer	ence clock divi	ded by 32				
	0100 = Refer	ence clock divi	ded by 16				
	0011 = Refer	ence clock divi	ded by 6 ded by 4				
	0001 = Refer	ence clock divi	ded by 2				
	0000 = Refer	ence clock	-				
bit 7-0	Unimplemen	ted: Read as '	כי				

REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

- **Note 1:** The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
 - 2: This pin is remappable. See Section 11.4 "Peripheral Pin Select (PPS)" for more information.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

r							
R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8
R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIC	G TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0
bit 7							bit 0
r							
Legend:		HS = Hardwa	ire Settable bit				
R = Reada	able bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value	at POR	'1' = Bit is set	['0' = Bit is clea	ared	x = Bit is unkn	own
bit 15	FLTMD: Fault	Mode Select	bit				
	1 = Fault mo	de is maintain	ed until the Fa	ault source is r	removed; the c	orresponding	OCFLTx bit is
	cleared in	n software and	a new PWM pe	eriod starts	loved and a po	N DWM poriod	etarte
hit 14							Starts
DIL 14	1 = PWM out	nut is driven h	iah on a Fault				
	0 = PWM out	put is driven lo	w on a Fault				
bit 13	FLTTRIEN: Fa	ault Output Sta	ate Select bit				
	1 = OCx pin i	s tri-stated on	a Fault conditio	on			
	0 = OCx pin I	/O state is def	ined by the FLT	OUT bit on a F	ault condition		
bit 12	OCINV: Outpu	ut Compare x I	nvert bit				
	1 = OCx outp	out is inverted	bo				
hit 11_9		ted: Read as '	0'				
bit 8	OC32. Casca	de Two OCx M	° Iodules Enable	hit (32-hit oper	ration)		
bit 0	1 = Cascade	module opera	tion is enabled		allony		
	0 = Cascade	module opera	tion is disabled				
bit 7	OCTRIG: Out	put Compare >	k Trigger/Sync S	Select bit			
	1 = Triggers (0 = Synchron	OCx from the s izes OCx with	source designat the source des	ted by the SYN	CSELx bits SYNCSELx bit	s	
bit 6	TRIGSTAT: Ti	mer Trigger St	atus bit	0 ,			
	1 = Timer sou	urce has been	triggered and is	s running			
	0 = Timer sou	urce has not be	een triggered a	nd is being held	d clear		
bit 5	OCTRIS: Out	put Compare x	Coutput Pin Dir	ection Select b	it		
	1 = OCx is tri	-stated					
		ompare x mod	ule drives the C	DCx pin			
Note 1:	Do not use the O	Cx module as i	its own Synchro	nization or Trig	ger source.		
2:	When the OCy module as a Trigg	odule is turned jer source, the	l OFF, it sends a OCy module m	a trigger out sig nust be unseled	gnal. If the OCx	module uses t source prior	he OCy to disabling it.
3:	Each Output Com	ipare x module	e (OCx) has one	e PTG Trigger/S	Synchronization	n source. See S	Section 24.0
	PTGO0 = OC1	Jei Generator			malion.		
	PTGO1 = OC2						
	PTGO2 = OC3						
	PTGO3 = OC4						

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

20.3 UARTx Control Registers

REGISTER 20-1: UXMODE: UARTX MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0		
UARTEN	יין <u>-</u>	USIDL	IREN ⁽²⁾	RTSMD	—	UEN1	UEN0		
bit 15							bit 8		
R/W-0, H	C R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL		
bit 7							bit 0		
Legend:		HC = Hardwa	re Clearable bi	t					
R = Reada	able bit	W = Writable	bit	U = Unimplem	ented bit, read	as '0'			
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown		
bit 15	UARTEN: UA 1 = UARTx is 0 = UARTx is minimal	NRTx Enable bit s enabled; all U s disabled; all U	(1) ARTx pins are IARTx pins are	controlled by U controlled by F	IARTx as define PORT latches; L	ed by UEN<1:0 JARTx power c	> onsumption is		
bit 14	Unimplemen	ted: Read as '	כ'						
bit 13	USIDL: UART	Tx Stop in Idle I	Mode bit						
	1 = Discontin 0 = Continue	ues module op s module opera	eration when c ation in Idle mo	device enters Id	le mode				
bit 12	IREN: IrDA [®] I	Encoder and D	ecoder Enable	bit ⁽²⁾					
	1 = IrDA ence	oder and decor	der are enabled	ł					
	0 = IrDA enco	oder and decod	der are disable	d					
bit 11	RTSMD: Mod	le Selection for	UxRTS Pin bit						
	1 = UXRISp 0 = UXRISp	in is in Simplex	mode						
bit 10		ted: Read as '	n'						
hit 9-8			ole hits						
	11 = UxTX. U	JxRX and BCL	(x pins are ena	bled and used:	UxCTS pin is c	ontrolled by PC)RT latches ⁽³⁾		
	10 = UxTX , U	IxRX, UxCTS a	nd UxRTS pin	s are enabled a	nd used ⁽⁴⁾	, ,			
	01 = UxTX, U	JxRX and UxRT	S pins are ena	bled and used;	UxCTS pin is c	ontrolled by PC	ORT latches ⁽⁴⁾		
	00 = UXIX ai PORT la	nd UXRX pins a	are enabled ar	id used; UXCTS	S and UXRIS/E	CLKx pins are	controlled by		
hit 7	WAKE: Wake	-un on Start hit	Detect During	Sleen Mode Fr	hable bit				
	1 = UARTx c	ontinues to sar	nple the UxRX	pin: interrupt is	generated on t	he falling edge	: bit is cleared		
	in hardwa	are on the follow	wing rising edg	e	g		,		
	0 = No wake	-up is enabled							
bit 6	LPBACK: UA	RTx Loopback	Mode Select b	bit					
	1 = Enables	Loopback mod	e						
	0 = Loopbacl	k mode is disab	Died						
Note 1:	Refer to the "UAF enabling the UAR	RT " (DS70582) Tx module for r	section in the " eceive or transi	dsPIC33/PIC24 mit operation.	Family Referen	<i>ce Manual"</i> for i	nformation on		
2:	This feature is on	ly available for	the 16x BRG r	mode (BRGH =	0).				
3:	This feature is on	is feature is only available on 44-pin and 64-pin devices.							

4: This feature is only available on 64-pin devices.





PTG Output Number	PTG Output Description
PTGO0	Trigger/Synchronization Source for OC1
PTGO1	Trigger/Synchronization Source for OC2
PTGO2	Trigger/Synchronization Source for OC3
PTGO3	Trigger/Synchronization Source for OC4
PTGO4	Clock Source for OC1
PTGO5	Clock Source for OC2
PTGO6	Clock Source for OC3
PTGO7	Clock Source for OC4
PTGO8	Trigger/Synchronization Source for IC1
PTGO9	Trigger/Synchronization Source for IC2
PTGO10	Trigger/Synchronization Source for IC3
PTGO11	Trigger/Synchronization Source for IC4
PTGO12	Sample Trigger for ADC
PTGO13	Sample Trigger for ADC
PTGO14	Sample Trigger for ADC
PTGO15	Sample Trigger for ADC
PTGO16	PWM Time Base Synchronous Source for PWM ⁽¹⁾
PTGO17	PWM Time Base Synchronous Source for PWM ⁽¹⁾
PTGO18	Mask Input Select for Op Amp/Comparator
PTGO19	Mask Input Select for Op Amp/Comparator
PTGO20	Reserved
PTGO21	Reserved
PTGO22	Reserved
PTGO23	Reserved
PTGO24	Reserved
PTGO25	Reserved
PTGO26	Reserved
PTGO27	Reserved
PTGO28	Reserved
PTGO29	Reserved
PTGO30	PTG Output to PPS Input Selection
PTGO31	PTG Output to PPS Input Selection

TABLE 24-2: PTG OUTPUT DESCRIPTIONS

Note 1: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER (CONTINUED)

- bit 3-0 SELSRCA<3:0>: Mask A Input Select bits
 - 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0101 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H 0000 = PWM1L

NOTES:

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
1	ADD	ADD	Acc ⁽¹⁾	Add Accumulators	1	1	OA,OB,SA,SB
		ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD	f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD	Wso,#Slit4,Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (4)	None
		BRA	GE, Expr	Branch if greater than or equal	1	1 (4)	None
		BRA	GEU, Expr	Branch if unsigned greater than or equal	1	1 (4)	None
		BRA	GT, Expr	Branch if greater than	1	1 (4)	None
		BRA	GTU, Expr	Branch if unsigned greater than	1	1 (4)	None
		BRA	LE, Expr	Branch if less than or equal	1	1 (4)	None
		BRA	LEU, Expr	Branch if unsigned less than or equal	1	1 (4)	None
		BRA	LT,Expr	Branch if less than	1	1 (4)	None
		BRA	LTU, Expr	Branch if unsigned less than	1	1 (4)	None
		BRA	N,Expr	Branch if Negative	1	1 (4)	None
		BRA	NC, Expr	Branch if Not Carry	1	1 (4)	None
		BRA	NN, Expr	Branch if Not Negative	1	1 (4)	None
		BRA	NOV, Expr	Branch if Not Overflow	1	1 (4)	None
		BRA	NZ,Expr	Branch if Not Zero	1	1 (4)	None
		BRA	OA, Expr(1)	Branch if Accumulator A overflow	1	1 (4)	None
		BRA	OB, Expr(1)	Branch if Accumulator B overflow	1	1 (4)	None
		BRA	OV, Expr(1)	Branch if Overflow	1	1 (4)	None
		BRA	SA, Expr(1)	Branch if Accumulator A saturated	1	1 (4)	None
		BRA	SB, Expr(1)	Branch if Accumulator B saturated	1	1 (4)	None
		BRA	Expr	Branch Unconditionally	1	4	None
		BRA	Z,Expr	Branch if Zero	1	1 (4)	None
L		BRA	Wn	Computed Branch	1	4	None
7	BSET	BSET	f,#bit4	Bit Set f	1	1	None
		BSET	Ws,#bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C	Ws,Wb	Write C bit to Ws <wb></wb>	1	1	None
		BSW.Z	Ws,Wb	Write Z bit to Ws <wb></wb>	1	1	None

TABLE 28-2: INSTRUCTION SET OVERVIEW

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

30.2 AC Characteristics and Timing Parameters

This section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X AC characteristics and timing parameters.

TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

	Standard Operating Conditions: 3.0V to 3.6V					
	(unless otherwise stated)					
	Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial					
AC CHARACTERISTICS	$-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
	Operating voltage VDD range as described in Section 30.1 "DC					
	Characteristics".					

FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
DO50	Cosco	OSC2 Pin	_	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	Сю	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	Св	SCLx, SDAx	_		400	pF	In I ² C™ mode

TABLE 30-37:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)TIMING REQUIREMENTS

АС СНА	AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions		
SP70	FscP	Maximum SCK2 Input Frequency	-	—	Lesser of FP or 15	MHz	(Note 3)		
SP72	TscF	SCK2 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)		
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)		
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)		
SP31	TdoR	SDO2 Data Output Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)		
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns			
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns			
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	—	ns			
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns			
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns			
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)		
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)		
SP60	TssL2doV	SDO2 Data Output Valid after SS2 Edge	-	—	50	ns			

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

TABLE 30-47:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)TIMING REQUIREMENTS

АС СНА	AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extende} \end{array}$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	FscP	Maximum SCK1 Input Frequency	—	—	15	MHz	(Note 3)	
SP72	TscF	SCK1 Input Fall Time	—	-	_	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK1 Input Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO1 Data Output Fall Time			_	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO1 Data Output Rise Time	—	-	_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	_	_	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	_	ns		
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120		—	ns		
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)	
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	_	ns	(Note 4)	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 30-48:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)TIMING REQUIREMENTS

АС СНА	AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions	
SP70	FscP	Maximum SCK1 Input Frequency		_	11	MHz	(Note 3)	
SP72	TscF	SCK1 Input Fall Time	_		—	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO1 Data Output Fall Time			_	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO1 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	_	_	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns		
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	Ι	—	ns		
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)	
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	_	ns	(Note 4)	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X



FIGURE 30-34: ECAN_x MODULE I/O TIMING CHARACTERISTICS

TABLE 30-51: ECANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions	
CA10	TIOF	Port Output Fall Time		_	_	ns	See Parameter DO32	
CA11	TIOR	Port Output Rise Time	_	_	_	ns	See Parameter DO31	
CA20	TCWF	Pulse Width to Trigger CAN Wake-up Filter	120			ns		

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 30-35: UARTX MODULE I/O TIMING CHARACTERISTICS



TABLE 30-52: UARTX MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions	
UA10	TUABAUD	UARTx Baud Time	66.67	_	_	ns		
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps		
UA20	TCWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	_	_	ns		

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]



Microchip Technology Drawing C04-154A Sheet 1 of 2

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Microchip Tradema Architecture — Flash Memory Fam Program Memory S Product Group — Pin Count — Tape and Reel Flag Temperature Range Package Pattern	rk ily ize (Kb (if app	dsPI	C 33 EP 64 MC5 04 T 1/PT - XXX	Examples: dsPIC33EP64MC504-I/PT: dsPIC33, Enhanced Performance, 64-Kbyte Program Memory, Motor Control, 44-Pin, Industrial Temperature, TQFP package.
Architecture:	33 24	= =	16-bit Digital Signal Controller 16-bit Microcontroller	
Flash Memory Family:	EP	=	Enhanced Performance	
Product Group:	GP MC	= =	General Purpose family Motor Control family	
Pin Count:	02 03 04 06	= = =	28-pin 36-pin 44-pin 64-pin	
Temperature Range:	l E	= =	-40°C to+85°C (Industrial) -40°C to+125°C (Extended)	
Package:	ML MR MV PT SO SP SS TL TL		Plastic Quad, No Lead Package - (44-pin) 8x8 mm body (QFN) Plastic Quad, No Lead Package - (28-pin) 6x6 mm body (QFN-S) Plastic Quad, No Lead Package - (64-pin) 9x9 mm body (QFN) Thin Quad, No Lead Package - (64-pin) 9x9 mm body (UQFN) Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) Plastic Small Outline, Wide - (28-pin) 7.50 mm body (SOIC) Skinny Plastic Dual In-Line - (28-pin) 300 mil body (SPDIP) Plastic Shrink Small Outline - (28-pin) 5.30 mm body (SOP) Very Thin Leadless Array - (36-pin) 5x5 mm body (VTLA) Very Thin Leadless Array - (44-pin) 6x6 mm body (VTLA)	