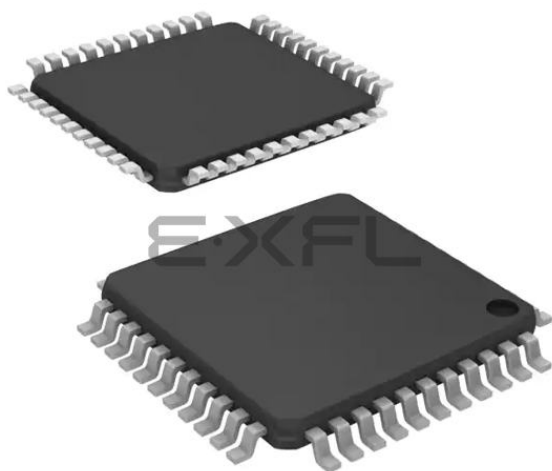




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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gp504t-i-pt

TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES

Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbytes)	Remappable Peripherals								I ² C™	CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages	
				16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM ⁽⁴⁾ (Channels)	Quadrature Encoder Interface	UART	SPI ⁽²⁾	ECAN™ Technology										External Interrupts ⁽³⁾
PIC24EP32MC202	512	32	4	5	4	4	6	1	2	2	—	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SPDIP, SOIC, SSOP ⁽⁵⁾ , QFN-S
PIC24EP64MC202	1024	64	8																		
PIC24EP128MC202	1024	128	16																		
PIC24EP256MC202	1024	256	32																		
PIC24EP512MC202	1024	512	48	5	4	4	6	1	2	2	—	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
PIC24EP32MC203	512	32	4																		
PIC24EP64MC203	1024	64	8																		
PIC24EP32MC204	512	32	4																		
PIC24EP64MC204	1024	64	8	5	4	4	6	1	2	2	—	3	2	1	9	3/4	Yes	Yes	35	44/ 48	VTLA ⁽⁵⁾ , TQFP, QFN, UQFN
PIC24EP128MC204	1024	128	16																		
PIC24EP256MC204	1024	256	32																		
PIC24EP512MC204	1024	512	48																		
PIC24EP64MC206	1024	64	8	5	4	4	6	1	2	2	—	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
PIC24EP128MC206	1024	128	16																		
PIC24EP256MC206	1024	256	32																		
PIC24EP512MC206	1024	512	48																		
dsPIC33EP32MC202	512	32	4	5	4	4	6	1	2	2	—	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SPDIP, SOIC, SSOP ⁽⁵⁾ , QFN-S
dsPIC33EP64MC202	1024	64	8																		
dsPIC33EP128MC202	1024	128	16																		
dsPIC33EP256MC202	1024	256	32																		
dsPIC33EP512MC202	1024	512	48	5	4	4	6	1	2	2	—	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
dsPIC33EP32MC203	512	32	4																		
dsPIC33EP64MC203	1024	64	8																		
dsPIC33EP32MC204	512	32	4																		
dsPIC33EP64MC204	1024	64	8	5	4	4	6	1	2	2	—	3	2	1	9	3/4	Yes	Yes	35	44/ 48	VTLA ⁽⁵⁾ , TQFP, QFN, UQFN
dsPIC33EP128MC204	1024	128	16																		
dsPIC33EP256MC204	1024	256	32																		
dsPIC33EP512MC204	1024	512	48																		
dsPIC33EP64MC206	1024	64	8	5	4	4	6	1	2	2	—	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP128MC206	1024	128	16																		
dsPIC33EP256MC206	1024	256	32																		
dsPIC33EP512MC206	1024	512	48																		
dsPIC33EP32MC502	512	32	4	5	4	4	6	1	2	2	1	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SPDIP, SOIC, SSOP ⁽⁵⁾ , QFN-S
dsPIC33EP64MC502	1024	64	8																		
dsPIC33EP128MC502	1024	128	16																		
dsPIC33EP256MC502	1024	256	32																		
dsPIC33EP512MC502	1024	512	48	5	4	4	6	1	2	2	1	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
dsPIC33EP32MC503	512	32	4																		
dsPIC33EP64MC503	1024	64	8																		

- Note 1:** On 28-pin devices, Comparator 4 does not have external connections. Refer to **Section 25.0 “Op Amp/Comparator Module”** for details.
2: Only SPI2 is remappable.
3: INT0 is not remappable.
4: Only the PWM Faults are remappable.
5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	—	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	QE11IF	PSEMIF	—	—	—	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	—	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	QE11IE	PSEMIE	—	—	—	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	—	—	—	—	CRCIE	U2EIE	U1EIE	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IE	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTIEIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	—	—	—	—	—	—	—	—	SPI2IP<2:0>			—	SPI2EIP<2:0>			0044
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC12	0858	—	—	—	—	—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC14	085C	—	—	—	—	—	QE11IP<2:0>			—	PSEMIP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040
IPC23	086E	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC24	0870	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IP<2:0>			4004

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-20: ADC1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
ADC1BUF0	0300	ADC1 Data Buffer 0																xxxx	
ADC1BUF1	0302	ADC1 Data Buffer 1																xxxx	
ADC1BUF2	0304	ADC1 Data Buffer 2																xxxx	
ADC1BUF3	0306	ADC1 Data Buffer 3																xxxx	
ADC1BUF4	0308	ADC1 Data Buffer 4																xxxx	
ADC1BUF5	030A	ADC1 Data Buffer 5																xxxx	
ADC1BUF6	030C	ADC1 Data Buffer 6																xxxx	
ADC1BUF7	030E	ADC1 Data Buffer 7																xxxx	
ADC1BUF8	0310	ADC1 Data Buffer 8																xxxx	
ADC1BUF9	0312	ADC1 Data Buffer 9																xxxx	
ADC1BUFA	0314	ADC1 Data Buffer 10																xxxx	
ADC1BUFB	0316	ADC1 Data Buffer 11																xxxx	
ADC1BUFC	0318	ADC1 Data Buffer 12																xxxx	
ADC1BUFD	031A	ADC1 Data Buffer 13																xxxx	
ADC1BUFE	031C	ADC1 Data Buffer 14																xxxx	
ADC1BUFF	031E	ADC1 Data Buffer 15																xxxx	
AD1CON1	0320	ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM<1:0>		SSRC<2:0>			SSRCG	SIMSAM	ASAM	SAMP	DONE	0000	
AD1CON2	0322	VCFG<2:0>			—	—	CSCNA	CHPS<1:0>		BUFS	SMPI<4:0>					BUFM	ALTS	0000	
AD1CON3	0324	ADRC	—	—	SAMC<4:0>				ADCS<7:0>										0000
AD1CHS123	0326	—	—	—	—	—	CH123NB<1:0>		CH123SB	—	—	—	—	—	CH123NA<1:0>		CH123SA	0000	
AD1CHS0	0328	CH0NB	—	—	CH0SB<4:0>					CH0NA	—	—	CH0SA<4:0>					0000	
AD1CSSH	032E	CSS31	CSS30	—	—	—	CSS26	CSS25	CSS24	—	—	—	—	—	—	—	—	0000	
AD1CSSL	0330	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000	
AD1CON4	0332	—	—	—	—	—	—	—	ADDMAEN	—	—	—	—	—	DMABL<2:0>			0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-49: PORTD REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E30	—	—	—	—	—	—	—	TRISD8	—	TRISD6	TRISD5	—	—	—	—	—	0160
PORTD	0E32	—	—	—	—	—	—	—	RD8	—	RD6	RD5	—	—	—	—	—	xxxx
LATD	0E34	—	—	—	—	—	—	—	LATD8	—	LATD6	LATD5	—	—	—	—	—	xxxx
ODCD	0E36	—	—	—	—	—	—	—	ODCD8	—	ODCD6	ODCD5	—	—	—	—	—	0000
CNEND	0E38	—	—	—	—	—	—	—	CNIED8	—	CNIED6	CNIED5	—	—	—	—	—	0000
CNPUD	0E3A	—	—	—	—	—	—	—	CNPUD8	—	CNPUD6	CNPUD5	—	—	—	—	—	0000
CNPDD	0E3C	—	—	—	—	—	—	—	CNPDD8	—	CNPDD6	CNPDD5	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-50: PORTE REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	0E40	TRISE15	TRISE14	TRISE13	TRISE12	—	—	—	—	—	—	—	—	—	—	—	—	F000
PORTE	0E42	RE15	RE14	RE13	RE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
LATE	0E44	LATE15	LATE14	LATE13	LATE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
ODCE	0E46	ODCE15	ODCE14	ODCE13	ODCE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNENE	0E48	CNIEE15	CNIEE14	CNIEE13	CNIEE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPUE	0E4A	CNPUE15	CNPUE14	CNPUE13	CNPUE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPDE	0E4C	CNPDE15	CNPDE14	CNPDE13	CNPDE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
ANSELE	0E4E	ANSE15	ANSE14	ANSE13	ANSE12	—	—	—	—	—	—	—	—	—	—	—	—	F000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-51: PORTF REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISF1	TRISF0	0003
PORTF	0E52	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RF1	RF0	xxxx
LATF	0E54	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATF1	LATF0	xxxx
ODCF	0E56	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCF1	ODCF0	0000
CNENF	0E58	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNIEF1	CNIEF0	0000
CNPUF	0E5A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUF1	CNPUF0	0000
CNPDF	0E5C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPDF1	CNPDF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDH and TBLWTH instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. TBLRDH and TBLWTH access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- TBLRDH (Table Read High):
 - In Word mode, this instruction maps the lower word of the Program Space location ($P<15:0>$) to a data address ($D<15:0>$)

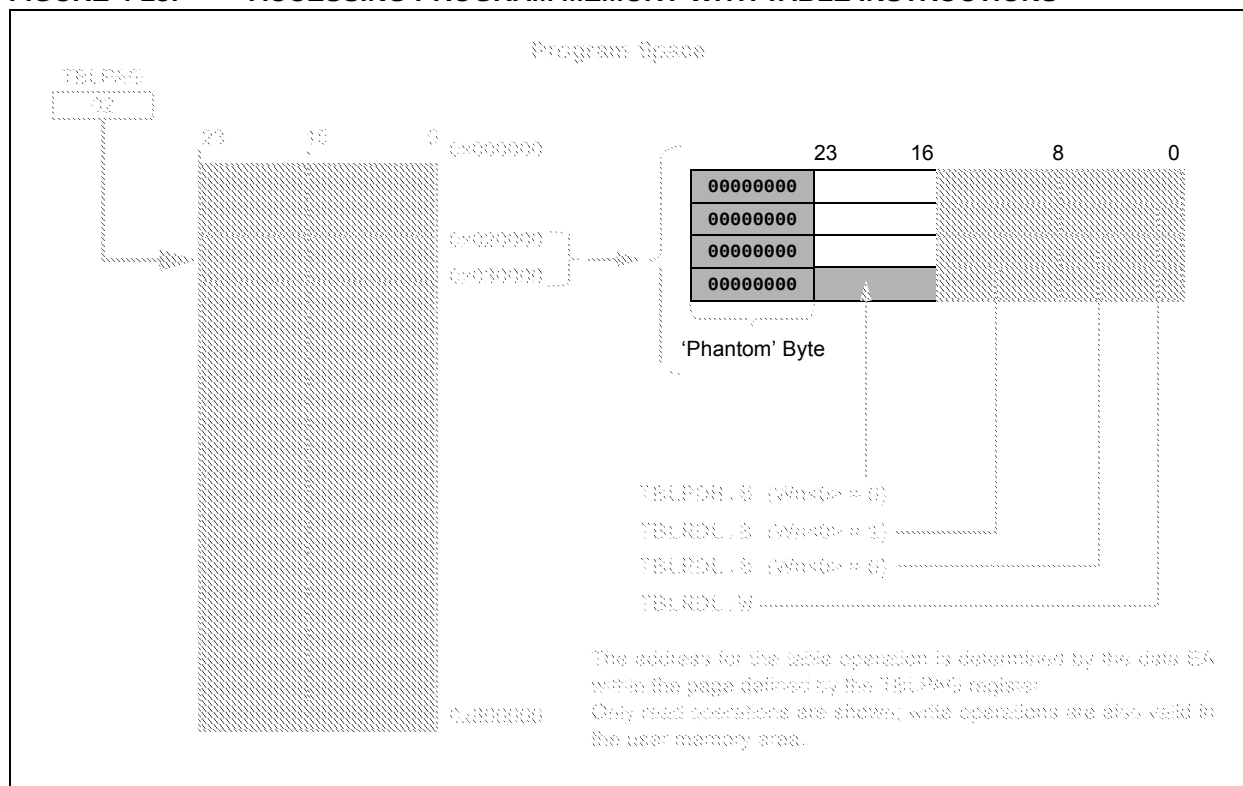
- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

- TBLRDH (Table Read High):
 - In Word mode, this instruction maps the entire upper word of a program address ($P<23:16>$) to a data address. The 'phantom' byte ($D<15:8>$) is always '0'.
 - In Byte mode, this instruction maps the upper or lower byte of the program word to $D<7:0>$ of the data address in the TBLRDH instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When $TBLPAG<7> = 0$, the table page is located in the user memory space. When $TBLPAG<7> = 1$, the page is located in configuration space.

FIGURE 4-23: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



6.1 Reset Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464
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6.1.1 KEY RESOURCES

- **“Reset”** (DS70602) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR ⁽¹⁾	OVBERR ⁽¹⁾	COVAERR ⁽¹⁾	COVBERR ⁽¹⁾	OVATE ⁽¹⁾	OVBTE ⁽¹⁾	COVTE ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR ⁽¹⁾	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFail	—
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **NSTDIS:** Interrupt Nesting Disable bit
 1 = Interrupt nesting is disabled
 0 = Interrupt nesting is enabled
- bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit⁽¹⁾
 1 = Trap was caused by overflow of Accumulator A
 0 = Trap was not caused by overflow of Accumulator A
- bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit⁽¹⁾
 1 = Trap was caused by overflow of Accumulator B
 0 = Trap was not caused by overflow of Accumulator B
- bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit⁽¹⁾
 1 = Trap was caused by catastrophic overflow of Accumulator A
 0 = Trap was not caused by catastrophic overflow of Accumulator A
- bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit⁽¹⁾
 1 = Trap was caused by catastrophic overflow of Accumulator B
 0 = Trap was not caused by catastrophic overflow of Accumulator B
- bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit⁽¹⁾
 1 = Trap overflow of Accumulator A
 0 = Trap is disabled
- bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit⁽¹⁾
 1 = Trap overflow of Accumulator B
 0 = Trap is disabled
- bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit⁽¹⁾
 1 = Trap on catastrophic overflow of Accumulator A or B is enabled
 0 = Trap is disabled
- bit 7 **SFTACERR:** Shift Accumulator Error Status bit⁽¹⁾
 1 = Math error trap was caused by an invalid accumulator shift
 0 = Math error trap was not caused by an invalid accumulator shift
- bit 6 **DIV0ERR:** Divide-by-Zero Error Status bit
 1 = Math error trap was caused by a divide-by-zero
 0 = Math error trap was not caused by a divide-by-zero
- bit 5 **DMACERR:** DMAC Trap Flag bit
 1 = DMAC trap has occurred
 0 = DMAC trap has not occurred

Note 1: These bits are available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

9.0 OSCILLATOR CONFIGURATION

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Oscillator**” (DS70580) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

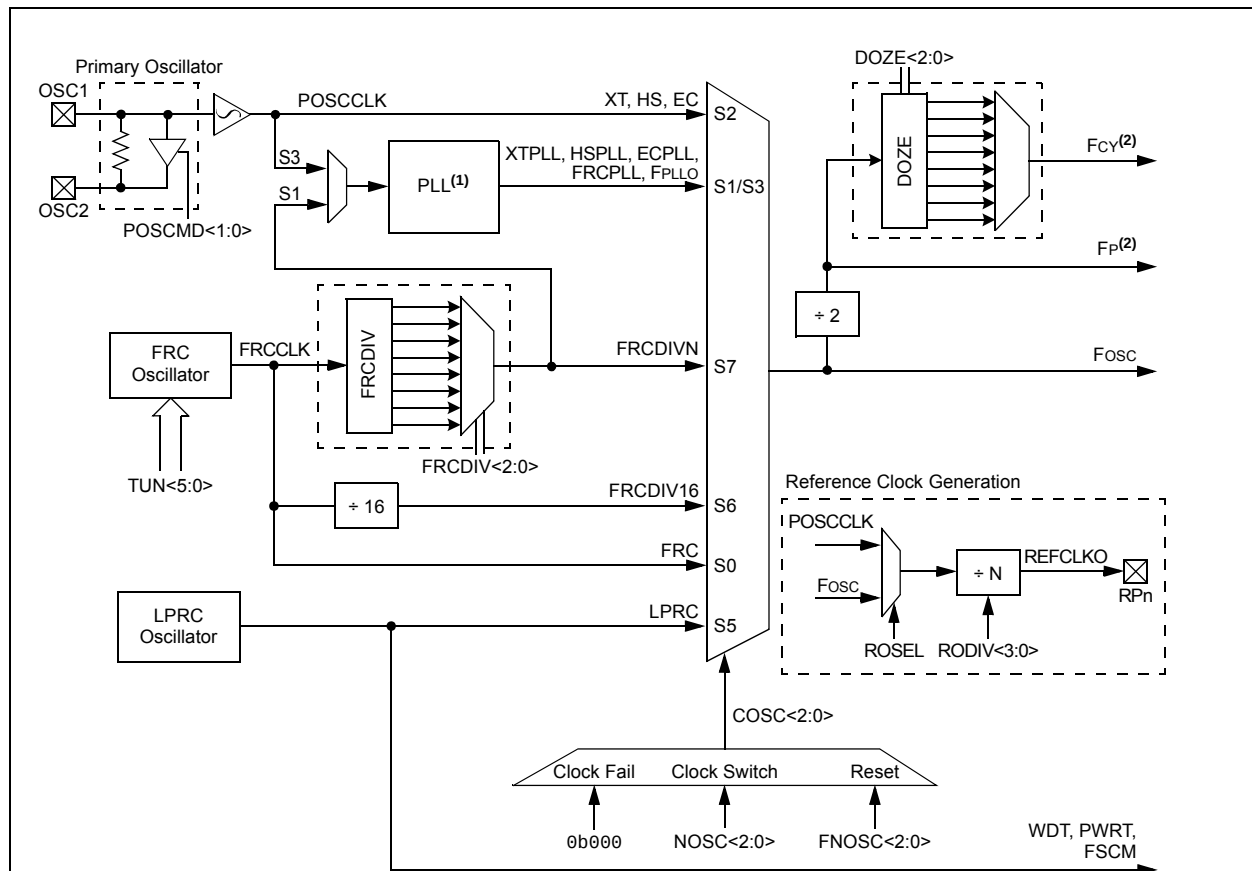
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X oscillator system provides:

- On-chip Phase-Locked Loop (PLL) to boost internal operating frequency on select internal and external oscillator sources
- On-the-fly clock switching between various clock sources
- Doze mode for system power savings
- Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Configuration bits for clock source selection

A simplified diagram of the oscillator system is shown in Figure 9-1.

FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM



Note 1: See Figure 9-2 for PLL details.

2: The term, Fp, refers to the clock source for all peripherals, while Fcy refers to the clock source for the CPU. Throughout this document, Fcy and Fp are used interchangeably, except in the case of Doze mode. Fp and Fcy will be different when Doze mode is used with a doze ratio of 1:2 or lower.

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
T5MD	T4MD	T3MD	T2MD	T1MD	QE11MD ⁽¹⁾	PWMMD ⁽¹⁾	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD ⁽²⁾	AD1MD
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **T5MD:** Timer5 Module Disable bit
1 = Timer5 module is disabled
0 = Timer5 module is enabled
- bit 14 **T4MD:** Timer4 Module Disable bit
1 = Timer4 module is disabled
0 = Timer4 module is enabled
- bit 13 **T3MD:** Timer3 Module Disable bit
1 = Timer3 module is disabled
0 = Timer3 module is enabled
- bit 12 **T2MD:** Timer2 Module Disable bit
1 = Timer2 module is disabled
0 = Timer2 module is enabled
- bit 11 **T1MD:** Timer1 Module Disable bit
1 = Timer1 module is disabled
0 = Timer1 module is enabled
- bit 10 **QE11MD:** QE11 Module Disable bit⁽¹⁾
1 = QE11 module is disabled
0 = QE11 module is enabled
- bit 9 **PWMMD:** PWM Module Disable bit⁽¹⁾
1 = PWM module is disabled
0 = PWM module is enabled
- bit 8 **Unimplemented:** Read as '0'
- bit 7 **I2C1MD:** I2C1 Module Disable bit
1 = I2C1 module is disabled
0 = I2C1 module is enabled
- bit 6 **U2MD:** UART2 Module Disable bit
1 = UART2 module is disabled
0 = UART2 module is enabled
- bit 5 **U1MD:** UART1 Module Disable bit
1 = UART1 module is disabled
0 = UART1 module is enabled
- bit 4 **SPI2MD:** SPI2 Module Disable bit
1 = SPI2 module is disabled
0 = SPI2 module is enabled

Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

REGISTER 11-20: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP39R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP38R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP39R<5:0>:** Peripheral Output Function is Assigned to RP39 Output Pin bits
(see Table 11-3 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP38R<5:0>:** Peripheral Output Function is Assigned to RP38 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 11-21: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP41R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP40R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP41R<5:0>:** Peripheral Output Function is Assigned to RP41 Output Pin bits
(see Table 11-3 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP40R<5:0>:** Peripheral Output Function is Assigned to RP40 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 17-19: INT1HLDH: INTERVAL 1 TIMER HOLD HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **INTHLD<31:16>**: Hold Register for Reading and Writing INT1TMRH bits

REGISTER 17-20: INT1HLDL: INTERVAL 1 TIMER HOLD LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **INTHLD<15:0>**: Hold Register for Reading and Writing INT1TMRL bits

REGISTER 21-15: CxBUFNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15BP<3:0>				F14BP<3:0>			
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F13BP<3:0>				F12BP<3:0>			
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **F15BP<3:0>**: RX Buffer Mask for Filter 15 bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•

•

•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 11-8 **F14BP<3:0>**: RX Buffer Mask for Filter 14 bits (same values as bits<15:12>)

bit 7-4 **F13BP<3:0>**: RX Buffer Mask for Filter 13 bits (same values as bits<15:12>)

bit 3-0 **F12BP<3:0>**: RX Buffer Mask for Filter 12 bits (same values as bits<15:12>)

22.2 CTMU Control Registers

REGISTER 22-1: CTMUCON1: CTMU CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN ⁽¹⁾	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

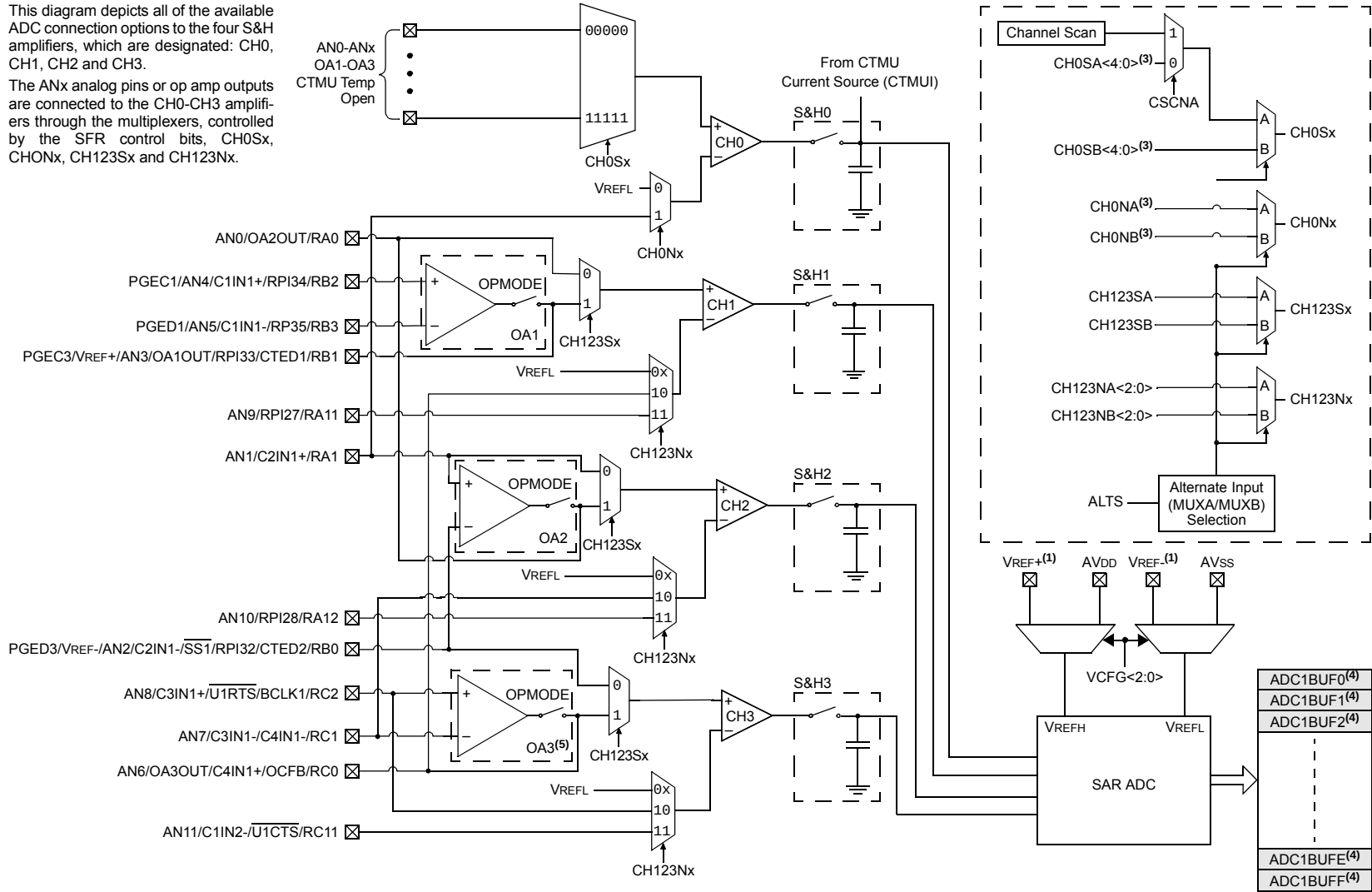
- bit 15 **CTMUEN:** CTMU Enable bit
 1 = Module is enabled
 0 = Module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **TGEN:** Time Generation Enable bit
 1 = Enables edge delay generation
 0 = Disables edge delay generation
- bit 11 **EDGEN:** Edge Enable bit
 1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)
 0 = Software is used to trigger edges (manual set of EDGxSTAT)
- bit 10 **EDGSEQEN:** Edge Sequence Enable bit
 1 = Edge 1 event must occur before Edge 2 event can occur
 0 = No edge sequence is needed
- bit 9 **IDISSEN:** Analog Current Source Control bit⁽¹⁾
 1 = Analog current source output is grounded
 0 = Analog current source output is not grounded
- bit 8 **CTTRIG:** ADC Trigger Control bit
 1 = CTMU triggers ADC start of conversion
 0 = CTMU does not trigger ADC start of conversion
- bit 7-0 **Unimplemented:** Read as '0'

Note 1: The ADC module Sample-and-Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

FIGURE 23-1: ADC MODULE BLOCK DIAGRAM WITH CONNECTION OPTIONS FOR ANx PINS AND OP AMPS

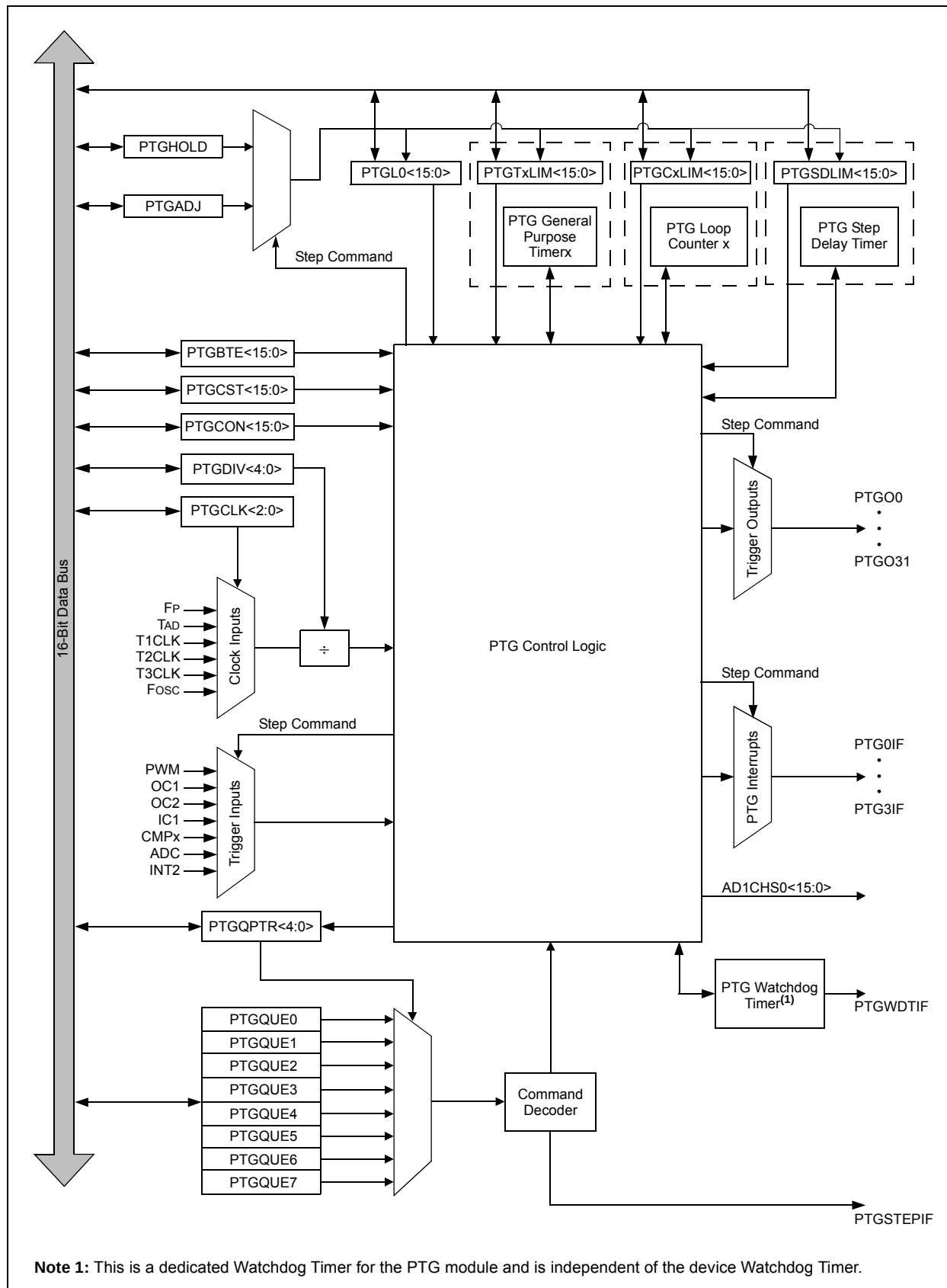
This diagram depicts all of the available ADC connection options to the four S&H amplifiers, which are designated: CH0, CH1, CH2 and CH3.

The ANx analog pins or op amp outputs are connected to the CH0-CH3 amplifiers through the multiplexers, controlled by the SFR control bits, CH0Sx, CHONx, CH123Sx and CH123Nx.



- Note**
- 1: VREF+, VREF- inputs can be multiplexed with other analog inputs.
 - 2: Channels 1, 2 and 3 are not applicable for the 12-bit mode of operation.
 - 3: These bits can be updated with Step commands from the PTG module. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.
 - 4: When ADDMAEN (AD1CON4<8>) = 1, enabling DMA, only ADC1BUF0 is used.
 - 5: OA3 is not available for 28-pin devices.

FIGURE 24-1: PTG BLOCK DIAGRAM



25.1 Op Amp Application Considerations

There are two configurations to take into consideration when designing with the op amp modules that are available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices. Configuration A (see Figure 25-6) takes advantage of the internal connection to the ADC module to route the output of the op amp directly to the ADC for measurement. Configuration B (see Figure 25-7) requires that the designer externally route the output of the op amp (OAxOUT) to a separate analog input pin (ANy) on the device. Table 30-55 in **Section 30.0 “Electrical Characteristics”** describes the performance characteristics for the op amps, distinguishing between the two configuration types where applicable.

25.1.1 OP AMP CONFIGURATION A

Figure 25-6 shows a typical inverting amplifier circuit taking advantage of the internal connections from the op amp output to the input of the ADC. The advantage of this configuration is that the user does not need to consume another analog input (ANy) on the device, and allows the user to simultaneously sample all three op amps with the ADC module, if needed. However, the presence of the internal resistance, RINT1, adds an error in the feedback path. Since RINT1 is an internal resistance, in relation to the op amp output (VOAxOUT) and ADC internal connection (VADC), RINT1 must be included in the numerator term of the transfer function. See Table 30-53 in **Section 30.0 “Electrical Characteristics”** for the typical value of RINT1. Table 30-60 and Table 30-61 in **Section 30.0 “Electrical Characteristics”** describe the minimum sample time (TSAMP) requirements for the ADC module in this configuration. Figure 25-6 also defines the equations that should be used when calculating the expected voltages at points, VADC and VOAxOUT.

FIGURE 25-6: OP AMP CONFIGURATION A

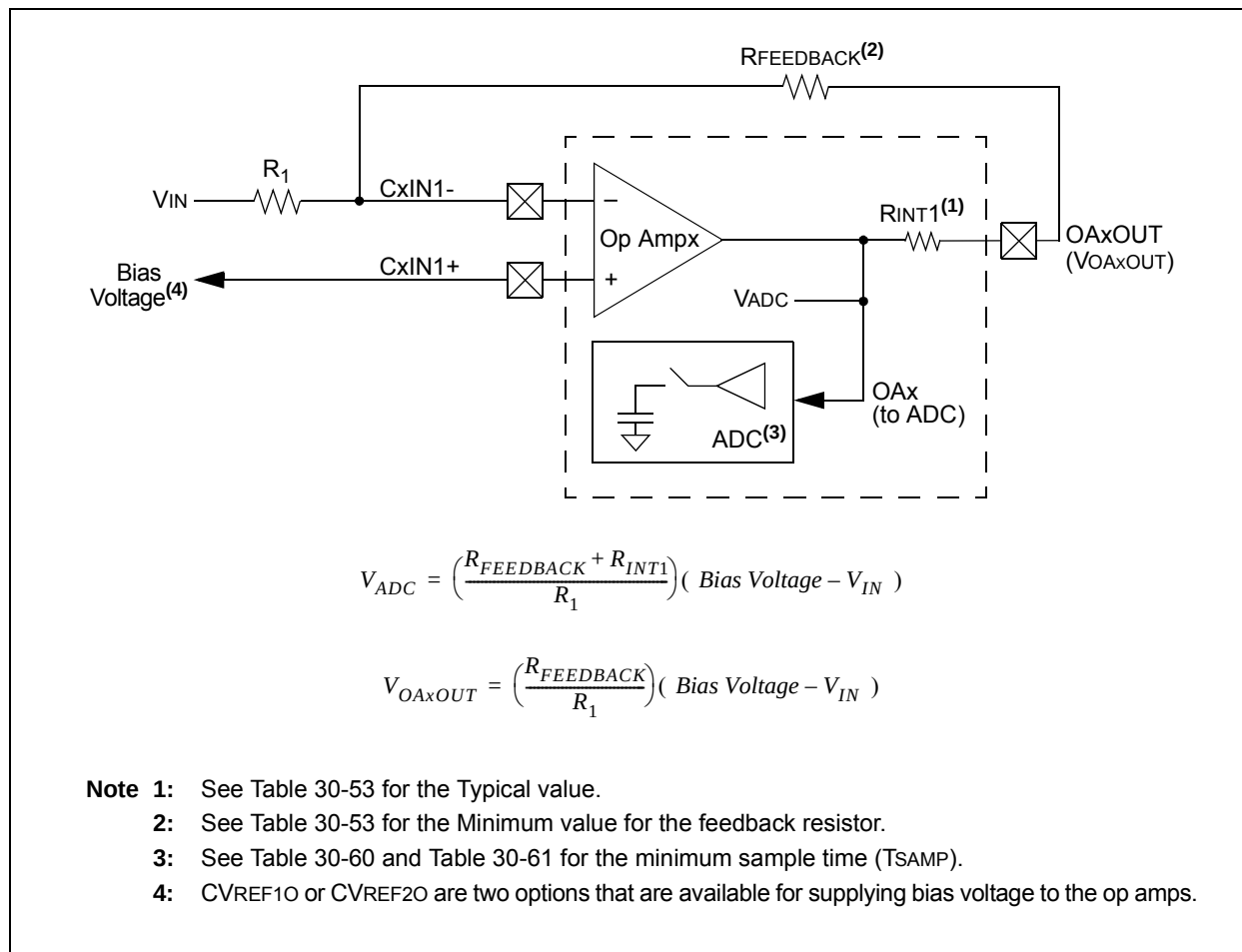


FIGURE 30-9: HIGH-SPEED PWMx MODULE FAULT TIMING CHARACTERISTICS
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

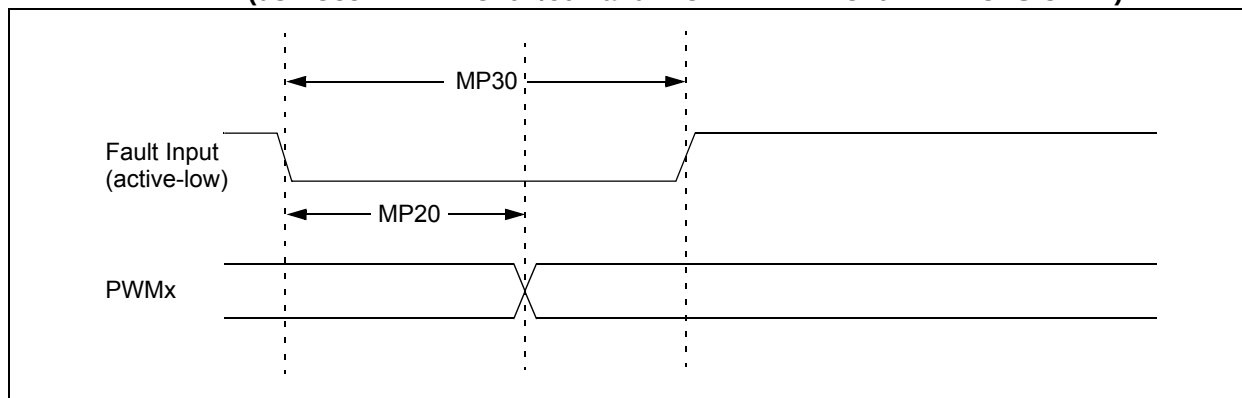


FIGURE 30-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

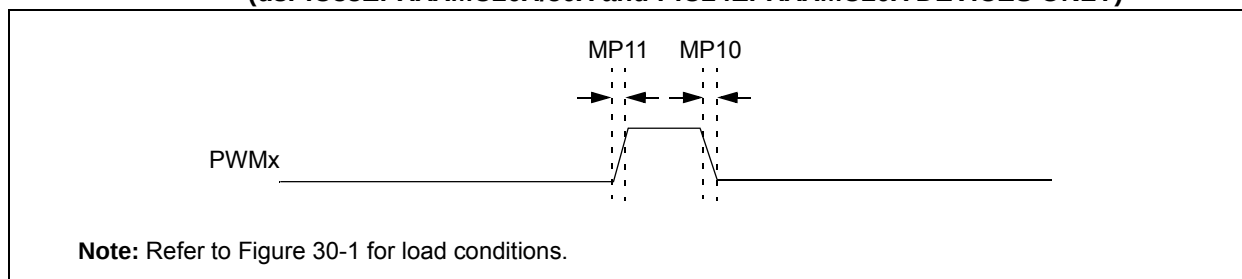


TABLE 30-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
MP10	TFPWM	PWMx Output Fall Time	—	—	—	ns	See Parameter DO32
MP11	TRPWM	PWMx Output Rise Time	—	—	—	ns	See Parameter DO31
MP20	T _{FD}	Fault Input ↓ to PWMx I/O Change	—	—	15	ns	
MP30	T _{FH}	Fault Input Pulse Width	15	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 31-12: ADC MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-Bit Mode) ⁽¹⁾							
HAD20a	Nr	Resolution ⁽³⁾	12 Data Bits			bits	
HAD21a	INL	Integral Nonlinearity	-5.5	—	5.5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD22a	DNL	Differential Nonlinearity	-1	—	1	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD23a	GERR	Gain Error	-10	—	10	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD24a	EOFF	Offset Error	-5	—	5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
Dynamic Performance (12-Bit Mode) ⁽²⁾							
HAD33a	FNYQ	Input Signal Bandwidth	—	—	200	kHz	

Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

TABLE 31-13: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (10-Bit Mode) ⁽¹⁾							
HAD20b	Nr	Resolution ⁽³⁾	10 Data Bits			bits	
HAD21b	INL	Integral Nonlinearity	-1.5	—	1.5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD22b	DNL	Differential Nonlinearity	-0.25	—	0.25	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD23b	GERR	Gain Error	-2.5	—	2.5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD24b	EOFF	Offset Error	-1.25	—	1.25	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
Dynamic Performance (10-Bit Mode) ⁽²⁾							
HAD33b	FNYQ	Input Signal Bandwidth	—	—	400	kHz	

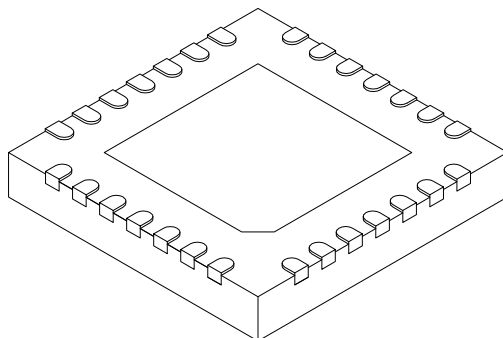
Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.70
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.70
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

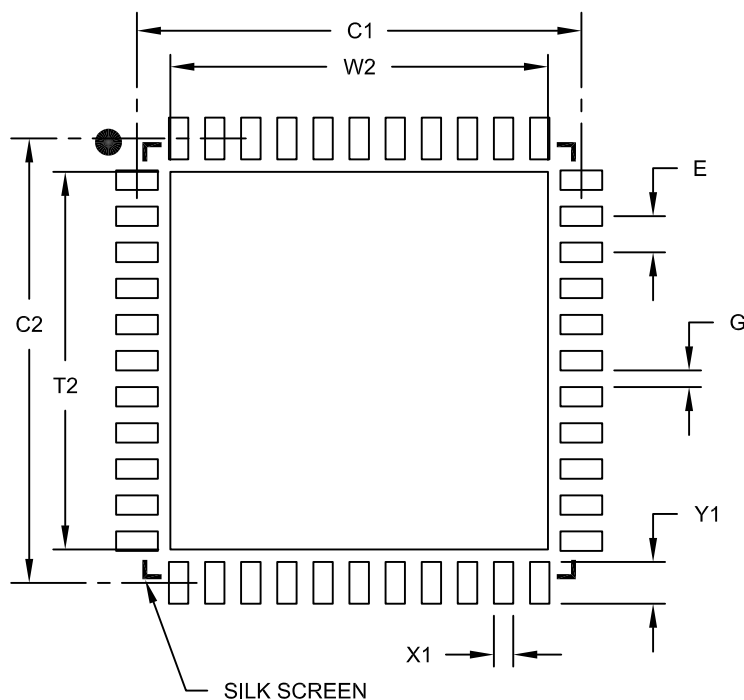
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124C Sheet 2 of 2

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B