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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

 $= K \in$

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K × 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gp506-e-mr

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FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X AND PIC24EP64GP/MC20X DEVICES



Note: Memory areas are not shown to scale.









File Name Addr. Bit 15 Bit 14 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 00 All Reset OC1CON1 0900 — — OCSIDL CCTSEL<2.0> — ENFLT8 ENFLT8 — OCFIT8 OCFIT8<	IADLL 4	+- I U.	001	FULC			CUGII	OUTFU			KE013		F						
OC1CON1 0900 — — ENFLTB ENFLTB ENFLTB OCFLTB OCFLTB OCFLTA TRIGMODE OCM<2:0> 0000 OC1CON2 9902 FLTMD FLTOUT FLTRIEN OCINV — — — OC32 OCTRIG TRIGSTAT OCFLTB OCFLTA TRIGMODE OCM<2:0> 0000 OC100N2 9902 FLTMD FLTRIEN OCINV — — — OC32 OCTRIG TRIGSTAT OCTRIS SYNCSEL 0000 OC100N2 9906 — — Output Compare 1 Beotondary Register \$xxxx OC2001 9906 — — OLTME 1 Register \$xxxx OC2001 9904 — — OC32 OCTRIG TRIGSTAT OCTRIS SYNCSEL \$0000 OC2001 9906 — TITMEVALUE 1 Register OCTRIS SYNCSEL \$0000 \$00000 OC22001 9900 — — OLTUT	File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON2 0902 FLTMD FLTNIEN OCINV — — OC22 OCTRIG TRIGSTAT OCTRIS SYNCSEL4:0> 0000 OC1RN 0906	OC1CON1	0900	_	—	OCSIDL	C	CTSEL<2:	0>	—	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>	•	0000
0C1RS 0904	OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS		SYN	NCSEL<4:0)>		000C
OC1R 096	OC1RS	0904							Outp	out Compare	e 1 Seconda	ary Register			xx				xxxx
0C1TMR 0908	OC1R	0906								Output Co	mpare 1 Re	egister							xxxx
OC2CON1 090A — OCSIDL C_TSEL<2:> — ENFLTB ENFLTB M OCFLTB OCFLTA TRIGMODE OCM 000000000000000000000000000000000000	OC1TMR	0908								Timer V	alue 1 Regi	ster							xxxx
OC2CON2 0900 FLTMU FLTMU FLTNIEN OCINV - - OC32 OCTRIG TRIGSTAT OCTRIS SYNCSEL4:0> OOD OC2R 0906 - - OC4 Corras SYNCSEL4:0> OOD OOD OC2R OOD Corras SYNCSEL4:0> OOD OO	OC2CON1	090A		—	OCSIDL	0	CTSEL<2:	0>	—	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000
OC2RS 0906 Image: Second Windows Condows	OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>				000C	
OC2R 0910 UNIC UNIC UNIC UNIC UNIC UNIC UNIC UNIC	OC2RS	090E							Outp	out Compare	e 2 Seconda	ary Register			x				xxxx
OC2TMR 0912 Image: Second	OC2R	0910	Output Compare 2 Register x						xxxx										
OC3CON1 0914 — — OCSIDL OCTSEL<2:> — ENFLTB ENFLTA — OCFLTB OCFLTA TRIGMODE OCM<2:>> 000000000000000000000000000000000000	OC2TMR	0912								Timer V	alue 2 Regi	ster							xxxx
OC3CON20916FLTMDFLTOUTFLTRIENOCINV———OC32OCTRIGTRIGSTATOCTRISSYNCSEL4:0>0000OC3RS09180918	OC3CON1	0914		—	OCSIDL	0	CTSEL<2:	0>	—	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000
OC3Rs 0918 Output Compare 3 Secondary Register xxxx OC3R 091A	OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS		SYN	NCSEL<4:0)>		000C
OC3R 091A	OC3RS	0918							Outp	out Compare	e 3 Seconda	ary Register							xxxx
OC3TMR 091C	OC3R	091A								Output Co	mpare 3 Re	egister							xxxx
OC4CON1 091E — OCSIDL OCTSEL<2:··· — ENFLTB ENFLTB OCFLTB OCFLTB OCFLTA TRIGMODE OCM<2:0> 000000000000000000000000000000000000	OC3TMR	091C								Timer V	alue 3 Regi	ster							xxxx
OC4CON2 0920 FLTMD FLTRIEN OCINV — — OC32 OCTRIG TRIGSTAT OCTRIS SYNCSEL<4:0> 000000000000000000000000000000000000	OC4CON1	091E	—	—	OCSIDL	0	CTSEL<2:	0>	_	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000
OC4Rs0922Output Compare 4 Secondary RegisterxxxxOC4R0924Output Compare 4 RegisterxxxxOC4TMR0926Timer Value 4 Registerxxxx	OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	_	_	_	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0> 00				000C	
OC4R 0924 Output Compare 4 Register xxxx OC4TMR 0926 Timer Value 4 Register xxxx	OC4RS	0922	Output Compare 4 Secondary Register xxxx						xxxx										
OC4TMR 0926 Timer Value 4 Register xxxx	OC4R	0924								Output Co	mpare 4 Re	egister							xxxx
	OC4TMR	0926		Timer Value 4 Register xxxx															

TABLE 4-10: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 4 REGISTER MAP

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

			FERIFIERAL FIN SELECT INFUT REGISTER WAF															
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	_				INT1R<6:0>	>			—	-	-	_	—	—	—	—	0000
RPINR1	06A2	_	_	_	_	_	—	_	—	_				INT2R<6:0>	•			0000
RPINR3	06A6	_	_	_	_		_		—	_	T2CKR<6:0>						0000	
RPINR7	06AE	_		IC2R<6:0>						_	IC1R<6:0>						0000	
RPINR8	06B0			IC4R<6:0>						_	IC3R<6:0>						0000	
RPINR11	06B6	_	_						_	OCFAR<6:0>						0000		
RPINR12	06B8	_		FLT2R<6:0>						_				FLT1R<6:0>	>			0000
RPINR14	06BC	_			(QEB1R<6:0	>						(QEA1R<6:0	>			0000
RPINR15	06BE				Н	OME1R<6:0	0>			_			I	NDX1R<6:0	>			0000
RPINR18	06C4		_	_	_	_	—	_	_	_	U1RXR<6:0>						0000	
RPINR19	06C6		_	_	_	_	—	_	_	_			ι	J2RXR<6:0	>			0000
RPINR22	06CC				S	CK2INR<6:	0>			_				SDI2R<6:0>	>			0000
RPINR23	06CE		_	_	_	_	—	_	_	_				SS2R<6:0>				0000
RPINR26	06D4		_	_	_	_	—	_	_	_	_	_	_	_	_	_	_	0000
RPINR37	06EA			SYNCI1R<6:0>						_	_	_	_	_	_	_	_	0000
RPINR38	06EC	_		DTCMP1R<6:0>						_						0000		
RPINR39	06EE	_		DTCMP3R<6:0>						_	DTCMP2R<6:0>					0000		

TABLE 4-29: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—		INT1R<6:0>						_	—	_	—	_	—	—		0000
RPINR1	06A2	—	_	_	—	_	_	—	—	_	— INT2R<6:0>					0000		
RPINR3	06A6	—	_	_	—	_	_	—	—	_	T2CKR<6:0>					0000		
RPINR7	06AE	—		IC2R<6:0>						_		IC1R<6:0>						0000
RPINR8	06B0	_				IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6	_	_	_	_	_	_	_	_	_			(DCFAR<6:0	>			0000
RPINR18	06C4	_	_	_	_	_	_	_	_	_			ι	J1RXR<6:0	>			0000
RPINR19	06C6	_	_	_	_	_	_	_	_	_			ι	J2RXR<6:0	>			0000
RPINR22	06CC	—			S	CK2INR<6:0)>			— SDI2R<6:0>					0000			
RPINR23	06CE	_	_	_	_	—	_	_	_	_	– SS2R<6:0>					0000		

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

6.0 RESETS

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Reset" (DS70602) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

- · POR: Power-on Reset
- · BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the SYSRST signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

Note: Refer to the specific peripheral section or Section 4.0 "Memory Organization" of this manual for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits, except for the POR and BOR bits (RCON<1:0>), that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

For all Resets, the default clock source is determined by the FNOSC<2:0> bits in the FOSCSEL Configuration register. The value of the FNOSC<2:0> bits is loaded into NOSC<2:0> (OSCCON<10:8>) on Reset, which in turn, initializes the system clock.



U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_		_	_		_	
bit 15			•				bit 8
U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
—	—		_		LSTCI	H<3:0>	
bit 7				-			bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value a	It POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-4	Unimplemen	ted: Read as '	0'				
bit 3-0	LSTCH<3:0>	: Last DMAC C	hannel Active	e Status bits			
	1111 = No DI 1110 = Reser	MA transfer ha rved	s occurred sir	nce system Re	set		
	•						
	•						
	•						
	0100 = Reser 0011 = Last c 0010 = Last c 0001 = Last c	rved Jata transfer wa Jata transfer wa Jata transfer wa	as handled by as handled by as handled by	/ Channel 3 / Channel 2 / Channel 1			

REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER

0000 = Last data transfer was handled by Channel 0 0000 = Last data transfer was handled by Channel 0

9.3 Oscillator Control Registers

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾

11-0	R-0	R-0	R-0	U-O	R/W-v	R/W-v	R/W-v						
	COSC2	COSC1	COSCO	_	NOSC2 ⁽²⁾	NOSC1 ⁽²⁾	NOSCO ⁽²⁾						
bit 15							bit 8						
R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0						
CLKLOC	CK IOLOCK	LOCK		CF ⁽³⁾		—	OSWEN						
bit 7							bit 0						
			(
Legend:	- h l - h :4	y = Value set	from Configur	ation bits on P	'OR	(0)							
		vv = vvritable	DIL	0 = 0	mented bit, read	as u							
-n = value	alpor	I = BILIS Set		0 = BIUS CIE	ared		IOWN						
bit 15	Unimplemen	ted: Read as '	0'										
bit 14-12	COSC<2:0>: Current Oscillator Selection bits (read-only)												
	111 = Fast R(111 = Fast RC Oscillator (FRC) with Divide-by-n											
	110 = Fast R	110 = Fast RC Oscillator (FRC) with Divide-by-16											
	101 = Low-Po	101 = Low-Power RC Oscillator (LPRC)											
	011 = Primary	100 = Reserved 011 = Primary Oscillator (XT, HS, EC) with PLL											
	010 = Primary	y Oscillator (X	r, HS, EC)										
	001 = Fast R 000 = Fast R	C Oscillator (F C Oscillator (F	RC) with Divid RC)	le-by-N and PL	L (FRCPLL)								
bit 11	Unimplemen	ted: Read as '	0'										
bit 10-8	NOSC<2:0>:	New Oscillator	Selection bits	_S (2)									
	111 = Fast R	C Oscillator (FRC) with Divide-by-n											
	110 = Fast R	C Oscillator (FRC) with Divide-by-16											
	101 - Low-PC 100 = Reserv	ed											
	011 = Primary	y Oscillator (X	r, HS, EC) wit	h PLL									
	010 = Primary	y Oscillator (X	r, HS, EC)										
	001 = Fast R0 000 = Fast R0	C Oscillator (FI	RC) with Divid RC)	Ie-by-N and PL	L (FRCPLL)								
bit 7	CLKLOCK: C	lock Lock Ena	ble bit										
	1 = If (FCKS	M0 = 1), then c	lock and PLL	configurations	are locked; if (F	CKSM0 = 0), t	hen clock and						
	0 = Clock and	d PLL selection	ns are not lock	ked, configurat	ions may be mo	dified							
bit 6	IOLOCK: I/O	Lock Enable b	it										
	1 = I/O lock is	active											
	0 = I/O lock is	not active	/ I I \										
bit 5	LOCK: PLL L	ock Status bit	(read-only)	ant un tincaria	a atiafia d								
	 1 = indicates 0 = Indicates 	that PLL is in	t of lock, start	-up timer is -up timer is in	progress or PLL	is disabled							
Note 1:	Writes to this regis	ter require an e erence Manual	unlock sequer " (available fro	nce. Refer to " om the Microch	Oscillator" (DS ip web site) for	70580) in the <i>"</i> o details.	dsPIC33/						
2:	Direct clock switch This applies to cloc	es between an ck switches in o	y primary osci either direction	llator mode wit	h PLL and FRC ances, the appli	PLL mode are r cation must sw	not permitted. itch to FRC						
	moue as a transitio	nai Clock Sour		IE IWO PLL IIIO	u c s.								

3: This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

REGISTER 11-9: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				HOME1R<6:0	>		
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				INDX1R<6:0>	>		
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	x = Bit is unkr	nown	
bit 15	Unimpleme	ented: Read as '	0'				
bit 15 bit 14-8	HOME1R<6	5:0>: Assign QEI	0 1 HOME1 (H selection nun	OME1) to the C	Corresponding	RPn Pin bits	
	1111001 =	Input tied to RPI	121	,			
		Input tied to CM	D1				
	0000000 =	Input tied to Vss	;				
bit 7	Unimpleme	ented: Read as '	0'				
bit 6-0	IND1XR<6: (see Table 2	0>: Assign QEI1 I1-2 for input pin	INDEX1 (INE selection nun	0X1) to the Cor nbers)	responding R	Pn Pin bits	
	1111001 =	Input tied to RPI	121	,			
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss					

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON ⁽¹⁾	—	TSIDL ⁽²⁾	—	_	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE ⁽¹⁾	TCKPS1 ⁽¹⁾	TCKPS0 ⁽¹⁾	_	—	TCS ^(1,3)	—
bit 7							bit 0

REGISTER 13-2: TyCON: (TIMER3 AND TIMER5) CONTROL REGISTER

Legend:				
R = Read	lable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value	e at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	TON: Tim	ery On bit ⁽¹⁾		
	1 = Starts	16-bit Timery		
	0 = Stops	16-bit Timery		
bit 14	Unimpler	nented: Read as '0'		
bit 13	TSIDL: Ti	mery Stop in Idle Mode bit ⁽²	2)	
	1 = Disco 0 = Contir	ntinues module operation w nues module operation in Id	/hen device enters Idle mode lle mode	
bit 12-7	Unimpler	nented: Read as '0'		
bit 6	TGATE: 1	imery Gated Time Accumu	lation Enable bit ⁽¹⁾	
	When TC	<u>S = 1:</u>		
	This bit is	ignored.		
	When TC	$\underline{S} = 0$:	lad	
	\perp = Gated	time accumulation is enab	led	
hit 5_4		I:0>: Timery Input Clock Pr	escale Select hits(1)	
511 0 4	11 = 1:25	6		
	10 = 1:64	•		
	01 = 1:8			
	00 = 1:1			
bit 3-2	Unimpler	nented: Read as '0'		
oit 1	TCS: Tim	ery Clock Source Select bit	(1,3)	
	1 = Extern 0 = Intern	nal clock is from pin, TyCK (al clock (FP)	(on the rising edge)	
oit O	Unimpler	nented: Read as '0'		
Note 1:	When 32-bit op functions are s	peration is enabled (T2CON et through TxCON.	<3> = 1), these bits have no ef	fect on Timery operation; all tir

2: When 32-bit timer operation is enabled (T32 = 1) in the Timerx Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

3: The TyCK pin is not available on all timers. See the "Pin Diagrams" section for the available pins.

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC				
ACKSTAT	TRSTAT	_	—	—	BCL	GCSTAT	ADD10				
bit 15					•		bit 8				
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC				
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF				
bit 7							bit 0				
Legend:		C = Clearab	le bit	HS = Hardwa	re Settable bit	HSC = Hardware S	ettable/Clearable bit				
R = Readable bit V		W = Writable	e bit	U = Unimplen	nented bit, read	as '0'					
-n = Value at POR		'1' = Bit is se	et	'0' = Bit is clea	ared	x = Bit is unknown					

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

bit 15	ACKSTAT: Acknowledge Status bit (when operating as I^2C^{TM} master, applicable to master transmit operation)
	1 = NACK received from slave 0 = ACK received from slave
	Hardware is set or clear at the end of slave Acknowledge.
bit 14	TRSTAT: Transmit Status bit (when operating as I^2C master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK)
	0 = Master transmit is not in progress Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
bit 13-11	Unimplemented: Read as '0'
bit 10	BCL: Master Bus Collision Detect bit
	1 = A bus collision has been detected during a master operation0 = No bus collision detected
	Hardware is set at detection of a bus collision.
bit 9	GCSTAT: General Call Status bit
	1 = General call address was received
	0 = General call address was not received
1.11.0	Hardware is set when address matches general call address. Hardware is clear at Stop detection.
DIT 8	ADD10: 10-Bit Address Status bit
	I = 10-bit address was matched 0 = 10-bit address was not matched
	Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
bit 7	IWCOL: I2Cx Write Collision Detect bit
	1 = An attempt to write to the I2CxTRN register failed because the I^2 C module is busy 0 = No collision
	Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
bit 6	I2COV: I2Cx Receive Overflow Flag bit
	 1 = A byte was received while the I2CxRCV register was still holding the previous byte 0 = No overflow
	Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
bit 5	D_A: Data/Address bit (when operating as I ² C slave)
	1 = Indicates that the last byte received was data
	 Indicates that the last byte received was a device address Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
	WAKFIL		—		SEG2PH2	SEG2PH1	SEG2PH0
bit 15			•	•			bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEG2PHTS	SAM	SEG1PH2	SEG1PH1	SEG1PH0	PRSEG2	PRSEG1	PRSEG0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown
bit 15	Unimplemen	nted: Read as '	0'				
bit 14	WAKFIL: Sel	lect CAN Bus L	ine Filter for V	Vake-up bit			
	1 = Uses CAI	N bus line filter	for wake-up	a-un			
bit 13-11		ted. Pead as '		e-up			
bit 10-8	SEG2PH-2.0		u nent 2 hits				
511 10-0	111 = 1 enoth	is 8 x To					
	•						
	•						
	•						
	000 = Length	n is 1 x Tq					
bit 7	SEG2PHTS:	Phase Segmer	nt 2 Time Sele	ect bit			
	1 = Freely pro	ogrammable					-4
hit C		1 OF SEGIPHX	Dits or informa	ation Processin	g Time (IPT), w	nicnever is gre	eater
DIL 6	J = Rus lino i	e of the CAN B	us Line bit a timos at tha	complo point			
	0 = Bus line i	s sampled once	e at the sampl	e point			
bit 5-3	SEG1PH<2:0)>: Phase Segr	nent 1 bits	•			
	111 = Length	n is 8 x Tq					
	•						
	•						
	•						
	000 = Length	n is 1 x Tq					
bit 2-0	PRSEG<2:0>	>: Propagation	Time Segmen	t bits			
	111 = Length	n is 8 x TQ					
	•						
	•						
	-						

REGISTER 21-10: CxCFG2: ECANx BAUD RATE CONFIGURATION REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0		
			_	—	—		ADDMAEN		
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0		
—	—	—	—	—	DMABL2	DMABL1	DMABL0		
bit 7							bit 0		
Legend:									
R = Readable	e bit	W = Writable b	pit	U = Unimple	mented bit, read	d as '0'			
-n = Value at POR		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown			
L									
bit 15-9	Unimplemen	ted: Read as 'o)'						
bit 8	ADDMAEN: A	ADC1 DMA Ena	able bit						
	1 = Conversio	on results are st	ored in the Al	DC1BUF0 regi	ster for transfer	to RAM using	DMA		
	0 = Conversio	on results are st	ored in ADC1	BUF0 through	ADC1BUFF reg	gisters; DMA w	vill not be used		
bit 7-3	Unimplemented: Read as '0'								
bit 2-0	DMABL<2:0>: Selects Number of DMA Buffer Locations per Analog Input bits								
	111 = Allocat	es 128 words o	f buffer to eac	h analog input	t				
	110 = Allocates 64 words of buffer to each analog input								
	101 = Allocates 32 words of buffer to each analog input								
	100 = Allocat	es 16 words of	buffer to each	analog input					
		es 8 words of b	uffer to each a	analog input					
		es 2 words of h	uffer to each :	analog input					
	000 = Allocates 1 word of buffer to each analog input								
	000 - Allocates i word of buller to each analog liput								

REGISTER 23-4: AD1CON4: ADC1 CONTROL REGISTER 4

24.0 PERIPHERAL TRIGGER GENERATOR (PTG) MODULE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Peripheral Trigger Generator (PTG)" (DS70669) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

24.1 Module Introduction

The Peripheral Trigger Generator (PTG) provides a means to schedule complex high-speed peripheral operations that would be difficult to achieve using software. The PTG module uses 8-bit commands, called "Steps", that the user writes to the PTG Queue registers (PTGQUE0-PTGQUE7), which perform operations, such as wait for input signal, generate output trigger and wait for timer.

The PTG module has the following major features:

- Multiple clock sources
- Two 16-bit general purpose timers
- Two 16-bit general limit counters
- Configurable for rising or falling edge triggering
- Generates processor interrupts to include:
 - Four configurable processor interrupts
 - Interrupt on a Step event in Single-Step modeInterrupt on a PTG Watchdog Timer time-out
- Able to receive trigger signals from these peripherals:
 - ADC
 - PWM
 - Output Compare
 - Input Capture
 - Op Amp/Comparator
 - INT2
- Able to trigger or synchronize to these peripherals:
 - Watchdog Timer
 - Output Compare
 - Input Capture
 - ADC
 - PWM
- Op Amp/Comparator

25.3 Op Amp/Comparator Registers

R/W-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	
PSIDL				C4EVT ⁽¹⁾	C3EVT ⁽¹⁾	C2EVT ⁽¹⁾	C1EVT ⁽¹⁾	
bit 15						bit 8		
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	
		—		C4OUT ⁽²⁾	C3OUT ⁽²⁾	C2OUT ⁽²⁾	C10UT ⁽²⁾	
bit 7							bit 0	
r								
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'		
-n = Value at P	POR	'1' = Bit is set		0° = Bit is cle	ared	x = Bit is unknown		
hit 15		arator Stop in	dla Mada hit					
DIL 15	1 = Discontinu	ues operation of	of all comparat	tors when devi	ce enters Idle n	node		
	0 = Continues	operation of a	Il comparators	s in Idle mode				
bit 14-12	Unimplement	ted: Read as ')'					
bit 11	C4EVT: Op A	mp/Comparato	r 4 Event Stat	us bit ⁽¹⁾				
	1 = Op amp/c	omparator eve	nt occurred					
h# 40	0 = Op amp/c	omparator eve		ur				
DIE TU	1 = Comparat	or event occur	Status Diter					
	0 = Comparat	or event did no	ot occur					
bit 9	C2EVT: Comp	parator 2 Event	: Status bit ⁽¹⁾					
	1 = Comparat	or event occur	red					
	0 = Comparator event did not occur							
bit 8	C1EVT: Comparator 1 Event Status bit ⁽¹⁾							
	1 = Comparat	or event occur	rea ot occur					
bit 7-4	Unimplement	ted: Read as ')'					
bit 3	C4OUT: Com	parator 4 Outp	ut Status bit ⁽²⁾					
	When CPOL =	<u>= 0:</u>						
	1 = VIN + > VIN	N-						
	0 = VIN + < VIN	N- = 1 ·						
	1 = VIN + < VIN	<u> </u>						
	0 = VIN + > VIN	N-						
bit 2	C3OUT: Com	parator 3 Outp	ut Status bit ⁽²⁾					
	When CPOL = $1 = V_{\rm IN} + > V_{\rm IN}$	<u>= 0:</u>						
	0 = VIN + < VIN	N- N-						
	When CPOL =	= 1:						
	1 = VIN+ < VIN-							
	v = v i N + > V I N	N-						

REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

- **Note 1:** Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON<9>.
 - 2: Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON<8>.

29.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

29.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

29.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a highspeed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

29.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a fullspeed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming[™] (ICSP[™]).

29.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.





TABLE 30-34: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK2 Frequency	—	_	15	MHz	(Note 3)
SP20	TscF	SCK2 Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK2 Output Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	_	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

TABLE 30-39:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency			15	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—		_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—		_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—		—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—		_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30		_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120		_	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

Revision D (December 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

TABLE A-3: MAJOR SECTION UPDATES

Section Name	Update Description
"16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High- Speed PWM, Op amps, and Advanced Analog"	Removed the Analog Comparators column and updated the Op amps/Comparators column in Table 1 and Table 2.
Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
Section 30.0 "Electrical Characteristics"	Updated the VBOR specifications and/or its related note in the following electrical characteristics tables: • Table 30-1 • Table 30-4 • Table 30-12 • Table 30-14 • Table 30-15 • Table 30-16 • Table 30-56 • Table 30-57 • Table 30-58 • Table 30-59 • Table 30-60

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

PMD (PIC24EPXXXIVC20X Devices)	
PORTA (PIC24EPXXXGP/MC202,	
dsPIC33EPXXXGP/MC202/502 Devices) 104	
PORTA (PIC24EPXXXGP/MC203,	
dsPIC33EPXXXGP/MC203/503 Devices) 103	
PORTA (PIC24EPXXXGP/MC204,	
dsPIC33EPXXXGP/MC204/504 Devices) 102	
dsPIC33EPXXXGP/MC206/506 Devices)	
PORTB (PIC24EPXXXGP/MC202,	
dsPIC33EPXXXGP/MC202/502 Devices) 104	
PORTB (PIC24EPXXXGP/MC203,	
dsPIC33EPXXXGP/MC203/503 Devices) 103	
PORTB (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices)	
PORTC (PIC23EPXXXGP/MC203,	
dsPIC33EPXXXGP/MC203/503 Devices) 103	
PORTC (PIC24EPXXXGP/MC204	
doDIC22EDXXXCD/MC204/504 Dovideos) 102	
PORTC (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices)	
PORTD (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices) 100	
PORTE (PIC24EPXXXGP/MC206	
doDIC22EDXXXCD/MC206/506 Dovideos) 100	
PORTF (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices) 100	
PORTG (PIC24EPXXXGP/MC206 and	
dsPIC33EPXXXGP/MC206/506 Devices) 101	
PTC 79	
FINI (0	
PWM (dsPIC33EPXXXMC20X/50X,	
PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices)	
PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXMC20X Devices) 79 PWM Generator 1 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) PWM Generator 2 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) PU24EPXXMC20X Devices) 80 PWM Generator 3 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) 80 QEI1 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) 80 QEI1 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) 81 Reference Clock	
PIG	
PIG 76 PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) PWM Generator 1 (dsPIC33EPXXXMC20X/50X, 79 PWM Generator 2 (dsPIC33EPXXXMC20X/50X, 79 PWM Generator 2 (dsPIC33EPXXXMC20X/50X, 79 PUC24EPXXXMC20X Devices) 80 PWM Generator 3 (dsPIC33EPXXXMC20X/50X, 80 PUC24EPXXXMC20X Devices) 80 QEI1 (dsPIC33EPXXMC20X/50X, 81 Reference Clock 93 SPI1 and SPI2 83 System Control 93	
PIG 76 PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) PWM Generator 1 (dsPIC33EPXXXMC20X/50X, 79 PWM Generator 2 (dsPIC33EPXXXMC20X/50X, 79 PWM Generator 2 (dsPIC33EPXXXMC20X/50X, 79 PWM Generator 3 (dsPIC33EPXXXMC20X/50X, 80 PWM Generator 3 (dsPIC33EPXXXMC20X/50X, 80 PUC24EPXXXMC20X Devices) 80 QEI1 (dsPIC33EPXXXMC20X/50X, 81 Reference Clock 93 SPI1 and SPI2 83 System Control 93 Time1 through Time5 75	
PIG 70 PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) PWM Generator 1 (dsPIC33EPXXXMC20X/50X, 79 PWM Generator 2 (dsPIC33EPXXXMC20X/50X, 79 PWM Generator 2 (dsPIC33EPXXXMC20X/50X, 79 PUC24EPXXXMC20X Devices) 80 PWM Generator 3 (dsPIC33EPXXXMC20X/50X, 81 PIC24EPXXXMC20X Devices) 80 QEI1 (dsPIC33EPXXXMC20X/50X, 81 Reference Clock 93 SPI1 and SPI2 83 System Control 93 Time1 through Time5 75	
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PIG 76 PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) PWM Generator 1 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) PWM Generator 2 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) PUC24EPXXXMC20X Devices) 80 PWM Generator 3 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) PIC24EPXXXMC20X Devices) 80 QEI1 (dsPIC33EPXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) 81 Reference Clock 93 SPI1 and SPI2 83 System Control 93 Time1 through Time5 75 UART1 and UART2 82 Registers AD1CHS0 (ADC1 Input Channel 0 Select) 333 AD1CHS123 (ADC1 Input Channel 1, 2, 3 Select) 331	
PIG 70 PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) 79 PWM Generator 1 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) 79 PWM Generator 2 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) 80 PWM Generator 3 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) 80 PWM Generator 3 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices) 80 QEI1 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, 81 Reference Clock 93 93 81 Reference Clock 93 93 31 System Control 93 93 333 AD1CHS0 (ADC1 Input Channel 0 Select) 333 333 AD1CHS123 (ADC1 Input 331 AD1CHS123 (ADC1 Input 331 Channel 1, 2, 3 Select) 331 331	
PIG	
PIG	
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PIC376PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXMC20X Devices)79PWM Generator 1 (dsPIC33EPXXXMC20X/50X, PIC24EPXXMC20X Devices)79PWM Generator 2 (dsPIC33EPXXXMC20X/50X, PIC24EPXXMC20X Devices)80PWM Generator 3 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices)80QEI1 (dsPIC33EPXXMC20X/50X, PIC24EPXXXMC20X/50X, 	
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PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXMC20X Devices)79PWM Generator 1 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)79PWM Generator 2 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)80PWM Generator 3 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)80PWM Generator 3 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)80QEI1 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)81Reference Clock93SPI1 and SPI283System Control93Time1 through Time575UART1 and UART282RegistersAD1CHS0 (ADC1 Input Channel 1, 2, 3 Select)331AD1CON1 (ADC1 Control 1)325AD1CON2 (ADC1 Control 2)327AD1CON3 (ADC1 Control 3)329AD1CON4 (ADC1 Control 4)330AD1CSSH (ADC1 Input Scan Select High)335AD1CSSL (ADC1 Input Scan Select Low)336	
PIG	
PIG	
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