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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gp506-h-pt">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gp506-h-pt</a>

## 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Program Memory**” (DS70613) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

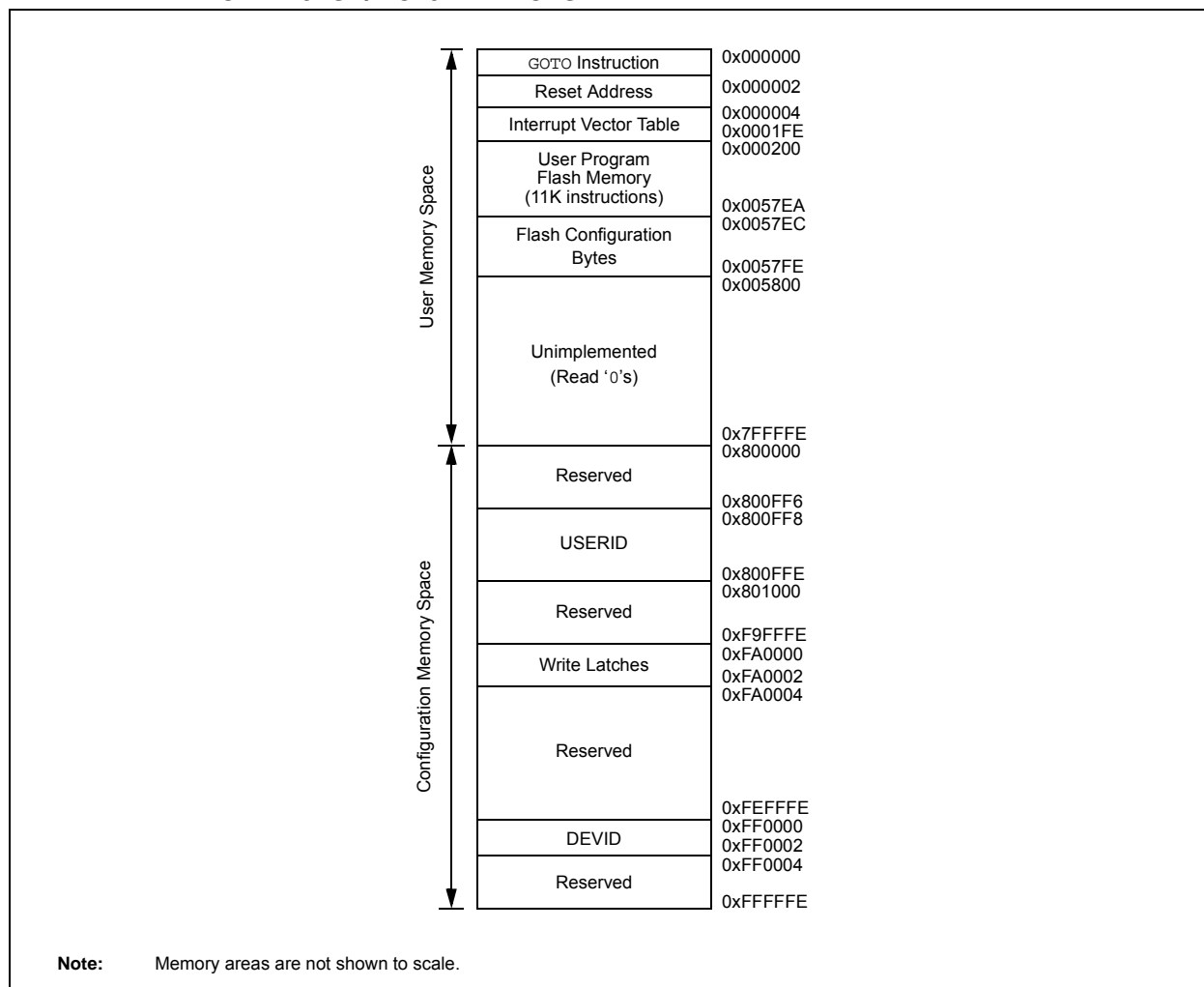
## 4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in **Section 4.8 “Interfacing Program and Data Memory Spaces”**.

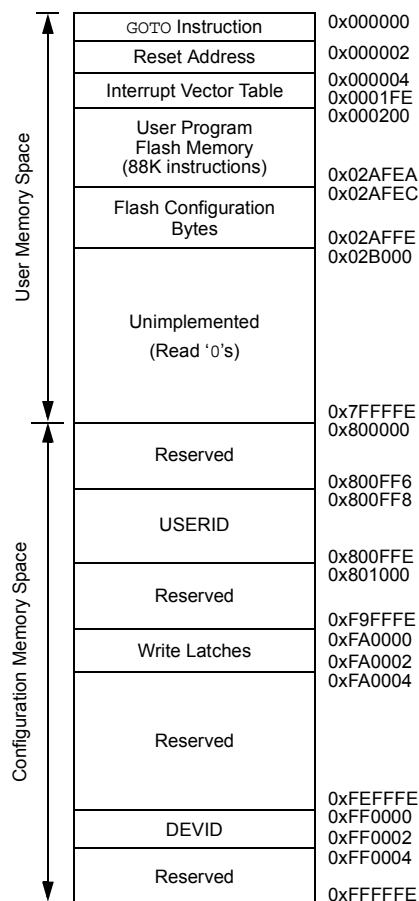
User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-5.

**FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X AND PIC24EP32GP/MC20X DEVICES**

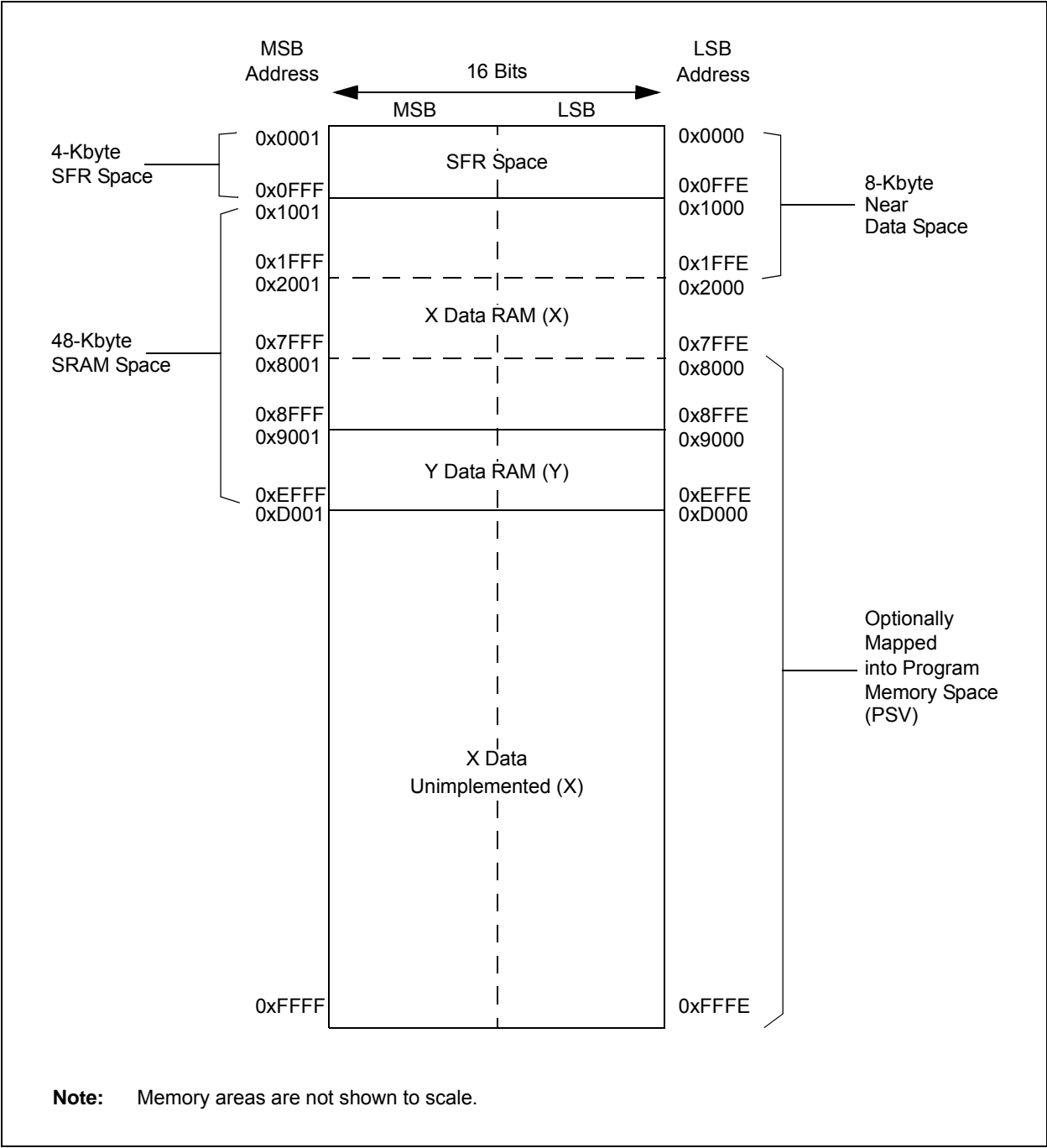


**FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X AND PIC24EP256GP/MC20X DEVICES**

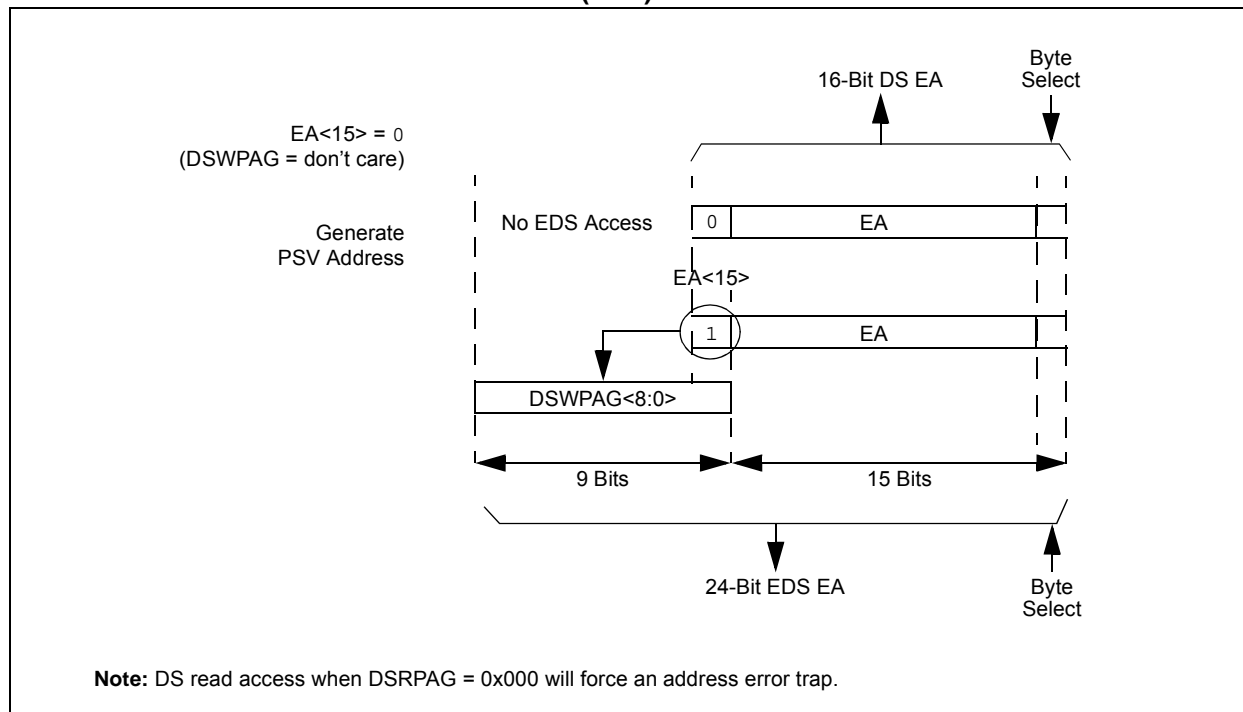


**Note:** Memory areas are not shown to scale.

FIGURE 4-11: DATA MEMORY MAP FOR dsPIC33EP512MC20X/50X AND dsPIC33EP512GP50X DEVICES



**EXAMPLE 4-2: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION**



The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS only. The Data Space and EDS can be read from, and written to, using DSRPAG and DSWPAG, respectively.

**FIGURE 7-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X INTERRUPT VECTOR TABLE**

<div style="display: flex; align-items: center;"> <div style="writing-mode: vertical-rl; transform: rotate(180deg); margin-right: 5px;">Decreasing Natural Order Priority</div> <div style="flex-grow: 1; border-left: 1px solid black; border-right: 1px solid black; position: relative;"> <div style="position: absolute; top: 0; left: 0; right: 0; height: 10px; background: linear-gradient(to right, transparent 49%, black 49% 51%, black 51% 52%, transparent 52%);"></div> <div style="position: absolute; bottom: 0; left: 0; right: 0; height: 10px; background: linear-gradient(to right, transparent 49%, black 49% 51%, black 51% 52%, transparent 52%);"></div> <div style="position: absolute; top: 50%; left: 50%; transform: translate(-50%, -50%);">IVT</div> </div> </div>	Reset – GOTO Instruction	0x000000	<div style="display: flex; align-items: center;"> <div style="writing-mode: vertical-rl; transform: rotate(180deg); margin-right: 5px;">See Table 7-1 for Interrupt Vector Details</div> <div style="flex-grow: 1; border-left: 1px solid black; border-right: 1px solid black; position: relative;"> <div style="position: absolute; top: 0; left: 0; right: 0; height: 10px; background: linear-gradient(to right, transparent 49%, black 49% 51%, black 51% 52%, transparent 52%);"></div> <div style="position: absolute; bottom: 0; left: 0; right: 0; height: 10px; background: linear-gradient(to right, transparent 49%, black 49% 51%, black 51% 52%, transparent 52%);"></div> </div> </div>
	Reset – GOTO Address	0x000002	
	Oscillator Fail Trap Vector	0x000004	
	Address Error Trap Vector	0x000006	
	Generic Hard Trap Vector	0x000008	
	Stack Error Trap Vector	0x00000A	
	Math Error Trap Vector	0x00000C	
	DMAC Error Trap Vector	0x00000E	
	Generic Soft Trap Vector	0x000010	
	Reserved	0x000012	
	Interrupt Vector 0	0x000014	
	Interrupt Vector 1	0x000016	
	:	:	
	:	:	
	:	:	
	Interrupt Vector 52	0x00007C	
	Interrupt Vector 53	0x00007E	
	Interrupt Vector 54	0x000080	
	:	:	
	:	:	
	:	:	
	Interrupt Vector 116	0x0000FC	
	Interrupt Vector 117	0x0000FE	
	Interrupt Vector 118	0x000100	
	Interrupt Vector 119	0x000102	
	Interrupt Vector 120	0x000104	
	:	:	
	:	:	
	:	:	
	Interrupt Vector 244	0x0001FC	
	Interrupt Vector 245	0x0001FE	
	START OF CODE	0x000200	

**REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)**

bit 4-0      **PLLPRE<4:0>**: PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)

11111 = Input divided by 33

•

•

•

00001 = Input divided by 3

00000 = Input divided by 2 (default)

- Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
- 2:** This bit is cleared when the ROI bit is set and an interrupt occurs.
- 3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

**REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	OCFAR<6:0>						
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7

**Unimplemented:** Read as '0'

bit 6-0

**OCFAR<6:0>:** Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss



**REGISTER 11-18: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP35R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP20R<5:0>					
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-14            **Unimplemented:** Read as '0'  
bit 13-8            **RP35R<5:0>:** Peripheral Output Function is Assigned to RP35 Output Pin bits  
(see Table 11-3 for peripheral function numbers)  
bit 7-6            **Unimplemented:** Read as '0'  
bit 5-0            **RP20R<5:0>:** Peripheral Output Function is Assigned to RP20 Output Pin bits  
(see Table 11-3 for peripheral function numbers)

**REGISTER 11-19: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP37R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP36R<5:0>					
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-14            **Unimplemented:** Read as '0'  
bit 13-8            **RP37R<5:0>:** Peripheral Output Function is Assigned to RP37 Output Pin bits  
(see Table 11-3 for peripheral function numbers)  
bit 7-6            **Unimplemented:** Read as '0'  
bit 5-0            **RP36R<5:0>:** Peripheral Output Function is Assigned to RP36 Output Pin bits  
(see Table 11-3 for peripheral function numbers)

## 17.1 QEI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

<p><b>Note:</b> In the event you are not able to access the product page using the link above, enter this URL in your browser: <a href="http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464">http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464</a></p>
--

### 17.1.1 KEY RESOURCES

- **“Quadrature Encoder Interface”** (DS70601) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

## 21.2 Modes of Operation

The ECAN module can operate in one of several operation modes selected by the user. These modes include:

- Initialization mode
- Disable mode
- Normal Operation mode
- Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

## 21.3 ECAN Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 21.3.1 KEY RESOURCES

- **“Enhanced Controller Area Network (ECAN™)”** (DS70353) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

**BUFFER 21-5: ECAN™ MESSAGE BUFFER WORD 4**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 3							
bit 15							
bit 8							

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 2							
bit 7							
bit 0							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Byte 3<15:8>**: ECAN Message Byte 3 bitsbit 7-0 **Byte 2<7:0>**: ECAN Message Byte 2 bits**BUFFER 21-6: ECAN™ MESSAGE BUFFER WORD 5**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 5							
bit 15							
bit 8							

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 4							
bit 7							
bit 0							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

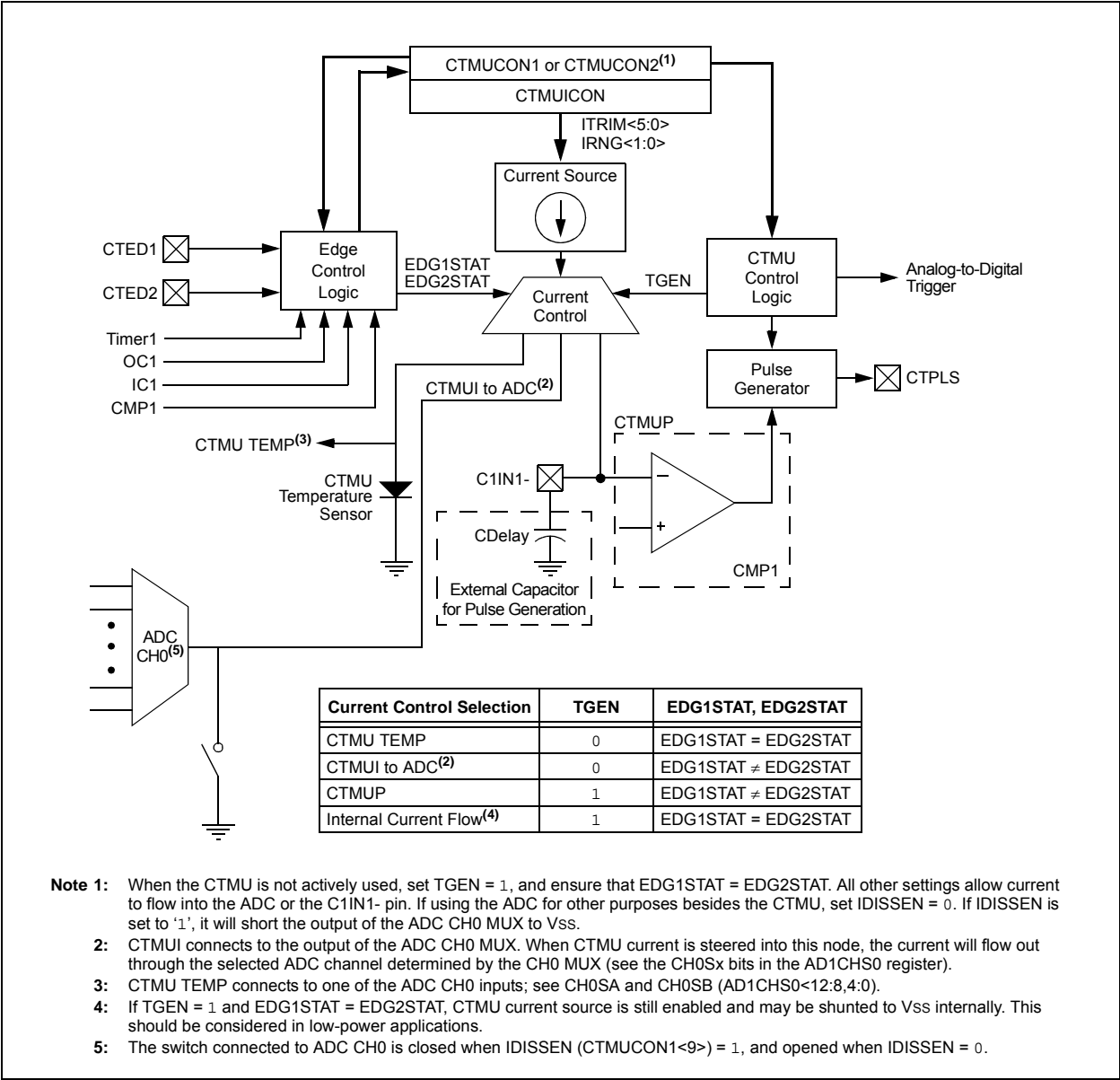
'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Byte 5<15:8>**: ECAN Message Byte 5 bitsbit 7-0 **Byte 4<7:0>**: ECAN Message Byte 4 bits

FIGURE 22-1: CTMU BLOCK DIAGRAM



22.1 CTMU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

22.1.1 KEY RESOURCES

- “Charge Time Measurement Unit (CTMU)” (DS70661) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)

bit 3-0	Step Command	OPTION<3:0>	Option Description
	PTGWHI <sup>(1)</sup> or PTGWLO <sup>(1)</sup>	0000	PWM Special Event Trigger. <sup>(3)</sup>
		0001	PWM master time base synchronization output. <sup>(3)</sup>
		0010	PWM1 interrupt. <sup>(3)</sup>
		0011	PWM2 interrupt. <sup>(3)</sup>
		0100	PWM3 interrupt. <sup>(3)</sup>
		0101	Reserved.
		0110	Reserved.
		0111	OC1 Trigger event.
		1000	OC2 Trigger event.
		1001	IC1 Trigger event.
		1010	CMP1 Trigger event.
		1011	CMP2 Trigger event.
		1100	CMP3 Trigger event.
		1101	CMP4 Trigger event.
		1110	ADC conversion done interrupt.
		1111	INT2 external interrupt.
	PTGIRQ <sup>(1)</sup>	0000	Generate PTG Interrupt 0.
		0001	Generate PTG Interrupt 1.
		0010	Generate PTG Interrupt 2.
		0011	Generate PTG Interrupt 3.
		0100	Reserved.
		.	.
		.	.
		1111	Reserved.
	PTGTRIG <sup>(2)</sup>	00000	PTGO0.
		00001	PTGO1.
		.	.
		.	.
		.	.
		11110	PTGO30.
		11111	PTGO31.

**Note 1:** All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

**2:** Refer to Table 24-2 for the trigger output descriptions.

**3:** This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3)**

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
CON	COE <sup>(2)</sup>	CPOL	—	—	OPMODE	CEVT	COUT
bit 15						bit 8	

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0	—	CREF <sup>(1)</sup>	—	—	CCH1 <sup>(1)</sup>	CCH0 <sup>(1)</sup>
bit 7						bit 0	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **CON:** Op Amp/Comparator Enable bit

1 = Op amp/comparator is enabled

0 = Op amp/comparator is disabled

bit 14 **COE:** Comparator Output Enable bit<sup>(2)</sup>

1 = Comparator output is present on the CxOUT pin

0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit

1 = Comparator output is inverted

0 = Comparator output is not inverted

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **OPMODE:** Op Amp/Comparator Operation Mode Select bit

1 = Circuit operates as an op amp

0 = Circuit operates as a comparator

bit 9 **CEVT:** Comparator Event bit

1 = Comparator event according to the EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared

0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit

When CPOL = 0 (non-inverted polarity):

1 = VIN+ > VIN-

0 = VIN+ < VIN-

When CPOL = 1 (inverted polarity):

1 = VIN+ < VIN-

0 = VIN+ > VIN-

**Note 1:** Inputs that are selected and not available will be tied to Vss. See the “Pin Diagrams” section for available inputs for each package.

**2:** This output is not available when OPMODE (CMxCON<10>) = 1.

**FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)  
TIMING CHARACTERISTICS**

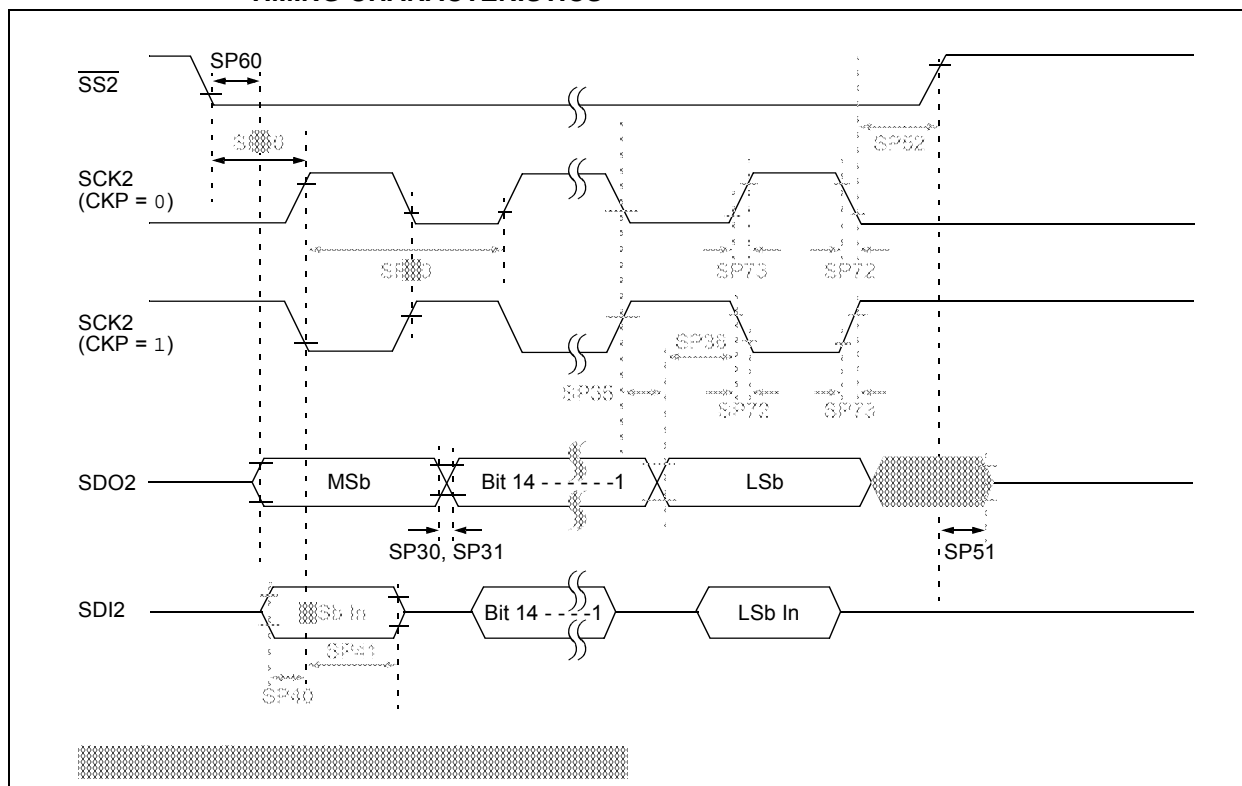




TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS

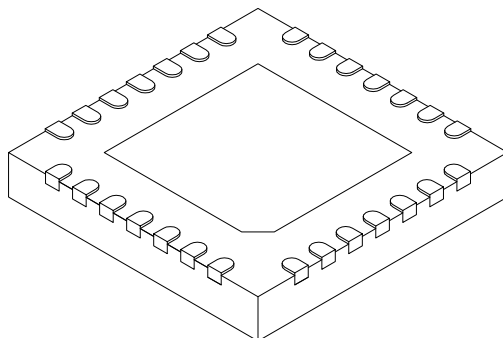
DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) <sup>(1)</sup> Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
<b>Comparator AC Characteristics</b>							
CM10	TRESP	Response Time <sup>(3)</sup>	—	19	—	ns	V+ input step of 100 mV, V- input held at VDD/2
CM11	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	μs	
<b>Comparator DC Characteristics</b>							
CM30	VOFFSET	Comparator Offset Voltage	—	±10	40	mV	
CM31	VHYST	Input Hysteresis Voltage <sup>(3)</sup>	—	30	—	mV	
CM32	TRISE/ TFALL	Comparator Output Rise/ Fall Time <sup>(3)</sup>	—	20	—	ns	1 pF load capacitance on input
CM33	VGAIN	Open-Loop Voltage Gain <sup>(3)</sup>	—	90	—	db	
CM34	VICM	Input Common-Mode Voltage	AVSS	—	AVDD	V	
<b>Op Amp AC Characteristics</b>							
CM20	SR	Slew Rate <sup>(3)</sup>	—	9	—	V/μs	10 pF load
CM21a	PM	Phase Margin (Configuration A) <sup>(3,4)</sup>	—	55	—	Degree	G = 100V/V; 10 pF load
CM21b	PM	Phase Margin (Configuration B) <sup>(3,5)</sup>	—	40	—	Degree	G = 100V/V; 10 pF load
CM22	GM	Gain Margin <sup>(3)</sup>	—	20	—	db	G = 100V/V; 10 pF load
CM23a	GBW	Gain Bandwidth (Configuration A) <sup>(3,4)</sup>	—	10	—	MHz	10 pF load
CM23b	GBW	Gain Bandwidth (Configuration B) <sup>(3,5)</sup>	—	6	—	MHz	10 pF load

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.
- 3:** Parameter is characterized but not tested in manufacturing.
- 4:** See Figure 25-6 for configuration information.
- 5:** See Figure 25-7 for configuration information.
- 6:** Resistances can vary by ±10% between op amps.

## 28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.70
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.70
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K	0.20	-	-

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124C Sheet 2 of 2

**Revision D (December 2011)**

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

**TABLE A-3: MAJOR SECTION UPDATES**

Section Name	Update Description
<b>“16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High-Speed PWM, Op amps, and Advanced Analog”</b>	Removed the Analog Comparators column and updated the Op amps/Comparators column in Table 1 and Table 2.
<b>Section 21.0 “Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)”</b>	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
<b>Section 30.0 “Electrical Characteristics”</b>	Updated the VBOR specifications and/or its related note in the following electrical characteristics tables: <ul style="list-style-type: none"><li>• Table 30-1</li><li>• Table 30-4</li><li>• Table 30-12</li><li>• Table 30-14</li><li>• Table 30-15</li><li>• Table 30-16</li><li>• Table 30-56</li><li>• Table 30-57</li><li>• Table 30-58</li><li>• Table 30-59</li><li>• Table 30-60</li></ul>

**NOTES:**

**NOTES:**