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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Ξ·ΧΕΙ

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K × 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mc204-i-mv

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls.

3.2 Instruction Set

The instruction set for dsPIC33EPXXXGP50X and dsPIC33EPXXXMC20X/50X devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The instruction set for PIC24EPXXXGP/MC20X devices has the MCU class of instructions only and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The base Data Space can be addressed as 64 Kbytes (32K words).

The Data Space includes two ranges of memory, referred to as X and Y data memory. Each memory range is accessible through its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Spaces have memory locations that are device-specific, and are described further in the data memory maps in **Section 4.2 "Data Address Space"**.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 32-Kbyte aligned program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to the "**Data Memory**" (DS70595) and "**Program Memory**" (DS70613) sections in the "*dsPIC33/PIC24 Family Reference Manual*" for more details on EDS, PSV and table accesses.

On the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms. PIC24EPXXXGP/MC20X devices do not support Modulo and Bit-Reversed Addressing.

3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- · Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

TABLE 4-19: SPI1 AND SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	_	SPISIDL	_	_	5	SPIBEC<2:0	>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI1CON1	0242	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	_	_		_	_	—	_	_	_	_	_	FRMDLY	SPIBEN	0000
SPI1BUF	0248							SPI1 Tra	insmit and R	eceive Buff	er Registe	r						0000
SPI2STAT	0260	SPIEN	_	SPISIDL	_	_	ŝ	SPIBEC<2:0	>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI2CON1	0262	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	_	_		_	_	—	_	_	_	_	_	FRMDLY	SPIBEN	0000
SPI2BUF	0268		SPI2 Transmit and Receive Buffer Register 00									0000						

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4	4-31:	PER	IPHERA	L PIN S	ELECT	INPUT F	REGISTI	ER MAP	FOR de	sPIC33E	EPXXXG	P50X D	EVICES	SONLY	

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—				INT1R<6:0>				_	_	—	—	—	—	—	_	0000
RPINR1	06A2		_	_	_	_	_	_	_	_				INT2R<6:0>	•			0000
RPINR3	06A6		_	_	_	_	_	_	_	_			٦	[2CKR<6:0	>			0000
RPINR7	06AE					IC2R<6:0>				_				IC1R<6:0>				0000
RPINR8	06B0					IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6		_	_	_	_	_	_	_	_			(DCFAR<6:0	>			0000
RPINR18	06C4		_	_	_	_	_	_	_	_			ι	J1RXR<6:0	>			0000
RPINR19	06C6		_	_	_	_	_	_	_	_			ι	J2RXR<6:0	>			0000
RPINR22	06CC				S	CK2INR<6:0)>			_			:	SDI2R<6:0>	•			0000
RPINR23	06CE	_	_	_	—	—	_	_	—	—				SS2R<6:0>				0000
RPINR26	06D4	—	_	_	-	_	_	—		—			(C1RXR<6:0	>			0000

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	_				INT1R<6:0>				—	—	—	—	—	—	—	_	0000
RPINR1	06A2		_							_	INT2R<6:0>					0000		
RPINR3	06A6		_	_	_	_	_	_	_	_			-	F2CKR<6:0	>			0000
RPINR7	06AE					IC2R<6:0>				_				IC1R<6:0>				0000
RPINR8	06B0					IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6		_	_	_	_	_	_	_	_			(DCFAR<6:0	>			0000
RPINR12	06B8					FLT2R<6:0>	•			_				FLT1R<6:0>	•			0000
RPINR14	06BC				(QEB1R<6:0	>			_	QEA1R<6:0>					0000		
RPINR15	06BE				Н	OME1R<6:0)>			_	INDX1R<6:0>						0000	
RPINR18	06C4		_	_	_	_	_	_	_	_	U1RXR<6:0>						0000	
RPINR19	06C6		_	_	_	_	_	_	_	_			ι	J2RXR<6:0	>			0000
RPINR22	06CC	_			S	CK2INR<6:()>			—				SDI2R<6:0>	•			0000
RPINR23	06CE	_	—	—		—	—		—	—				SS2R<6:0>				0000
RPINR26	06D4	_						—	—	C1RXR<6:0>					0000			
RPINR37	06EA	_	SYNCI1R<6:0>						—	—	—	—	—				0000	
RPINR38	06EC	_	DTCMP1R<6:0>						—						0000			
RPINR39	06EE	_	DTCMP3R<6:0>						_			D	CMP2R<6:	0>			0000	

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 11-7: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				FLT2R<6:0>			
bit 15							bit 8
	D 444 A	D 444 0	D 444 A	Date	D 444 0	D M M A	D # 44 0
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				FLT1R<6:0>			
bit 7							bit C
Legend:							
R = Readabl	le bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 14-8	FLT2R<6:0> (see Table 11	-2 for input pin	Fault 2 (FLT2)) to the Corresp nbers)	onding RPn F	Pin bits	
bit 14-8	FLT2R<6:0> (see Table 11 1111001 = h	: Assign PWM I	Fault 2 (FLT2) selection nur 121		onding RPn F	Pin bits	
bit 14-8	FLT2R<6:0> (see Table 11 1111001 = h	: Assign PWM I I-2 for input pin nput tied to RPI	Fault 2 (FLT2) selection nur 121 P1		onding RPn F	Pin bits	
bit 14-8 bit 7	FLT2R<6:0> (see Table 11 1111001 = h	: Assign PWM I I-2 for input pin nput tied to RPI nput tied to CM	Fault 2 (FLT2 selection nur 121 P1		onding RPn F	Pin bits	

16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support a dedicated Pulse-Width Modulation (PWM) module with up to 6 outputs.

The high-speed PWMx module consists of the following major features:

- Three PWM generators
- Two PWM outputs per PWM generator
- Individual period and duty cycle for each PWM pair
- Duty cycle, dead time, phase shift and frequency resolution of Tcy/2 (7.14 ns at Fcy = 70MHz)
- Independent Fault and current-limit inputs for six PWM outputs
- · Redundant output
- Center-Aligned PWM mode
- Output override control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Prescaler for input clock
- PWMxL and PWMxH output pin swapping
- Independent PWM frequency, duty cycle and phase-shift changes for each PWM generator
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB) functionality
- Frequency resolution enhancement
- PWM capture functionality

Note: In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 8.32 ns.

The high-speed PWMx module contains up to three PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWMx can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADC module based on either of the two master time bases.

The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 input pin that utilizes PPS, can synchronize the high-speed PWMx module with an external signal. The SYNC01 pin is an output pin that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

16.1 PWM Faults

The PWMx module incorporates multiple external Fault inputs to include FLT1 and FLT2 which are remappable using the PPS feature, FLT3 and FLT4 which are available only on the larger 44-pin and 64-pin packages, and FLT32 which has been implemented with Class B safety features, and is available on a fixed pin on all dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

16.1.1 PWM FAULTS AT RESET

During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the highspeed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled low externally or the internal pull-down resistor in the CNPDx register can be enabled.

Note: The Fault mode may be changed using the FLTMOD<1:0> bits (FCLCON<1:0>), regardless of the state of FLT32.

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Quadrature Encoder Interface (QEI)" (DS70601) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High register
- 32-Bit Position Compare Low register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0
bit 7							bit 0
Legend:		C = Writable b	oit, but only '0'	can be writter	n to clear the bit		

Legend:	C = Writable bit, but only '0'	can be written to clear the bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 RXOVF<15:0>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but or	C = Writable bit, but only '0' can be written to clear the bit							
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'						
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown						

bit 15-0 RXOVF<31:16>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0								
—	_	—		—	_	—	ADDMAEN								
bit 15							bit 8								
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0								
0-0	0-0	0-0	0-0	0-0			-								
	—	—	—	—	DMABL2	DMABL1	DMABL0								
bit 7							bit 0								
Legend:															
R = Readab	le bit	W = Writable b	bit	U = Unimpler	mented bit, read	1 as '0'									
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle		x = Bit is unk	nown								
bit 15-9	Unimplemen	ted: Read as '0	3												
bit 8	ADDMAEN: A	ADC1 DMA Ena	ıble bit												
				0	ster for transfer ADC1BUFF reg	0									
bit 7-3	Unimplemen	ted: Read as '0	,												
bit 2-0	DMABL<2:0>	Selects Numb	per of DMA B	uffer Locations	per Analog Inpu	ut bits									
	110 = Allocat 101 = Allocat 100 = Allocat 011 = Allocat 010 = Allocat 001 = Allocat	es 64 words of l es 32 words of l es 16 words of l es 8 words of b es 4 words of b	buffer to each buffer to each buffer to each uffer to each uffer to each a uffer to each a	analog input analog input analog input analog input analog input analog input analog input		 0 = Conversion results are stored in ADC1BUF0 through ADC1BUFF registers; DMA will not be used Unimplemented: Read as '0' DMABL<2:0>: Selects Number of DMA Buffer Locations per Analog Input bits 111 = Allocates 128 words of buffer to each analog input 110 = Allocates 64 words of buffer to each analog input 101 = Allocates 32 words of buffer to each analog input 100 = Allocates 16 words of buffer to each analog input 101 = Allocates 4 words of buffer to each analog input 100 = Allocates 4 words of buffer to each analog input 111 = Allocates 8 words of buffer to each analog input 112 = Allocates 92 words of buffer to each analog input 113 = Allocates 92 words of buffer to each analog input 114 = Allocates 92 words of buffer to each analog input 115 = Allocates 92 words of buffer to each analog input 115 = Allocates 92 words of buffer to each analog input 115 = Allocates 92 words of buffer to each analog input 115 = Allocates 92 words of buffer to each analog input 115 = Allocates 92 words of buffer to each analog input 115 = Allocates 92 words of buffer to each analog input 115 = Allocates 92 words of buffer to each analog input 115 = Allocates 92 words of buffer to each analog input 115 = Allocates 92 words of buffer to each analog input 115 = Allocates 92 words of buffer to each analog input 115 = Allocates 92 words of buffer to each analog input 									

REGISTER 23-4: AD1CON4: ADC1 CONTROL REGISTER 4

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)

bit 4-0	CH0SA<4:0>: Channel 0 Positive Input Select for Sample MUXA bits ⁽¹⁾
	11111 = Open; use this selection with CTMU capacitive and time measurement
	11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)
	11101 = Reserved
	11100 = Reserved
	11011 = Reserved
	11010 = Channel 0 positive input is the output of OA3/AN6 ^(2,3)
	11001 = Channel 0 positive input is the output of OA2/AN0 ⁽²⁾
	11000 = Channel 0 positive input is the output of OA1/AN3 ⁽²⁾
	10110 = Reserved
	•
	•
	10000 = Reserved
	01111 = Channel 0 positive input is AN15 ^(1,3)
	01110 = Channel 0 positive input is AN14 ^(1,3)
	01101 = Channel 0 positive input is AN13 ^(1,3)
	•
	00010 = Channel 0 positive input is AN2 ^(1,3)
	00001 = Channel 0 positive input is AN1 ^(1,3)
	00000 = Channel 0 positive input is AN0(1,3)

- **Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
 - 2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.
 - 3: See the "Pin Diagrams" section for the available analog channels for each device.

NOTES:

00.4FC 64 <th< th=""><th>File Name</th><th>Address</th><th>Device Memory Size (Kbytes)</th><th>Bits 23-8</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></th<>	File Name	Address	Device Memory Size (Kbytes)	Bits 23-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
004FC 64 <td>Reserved</td> <td>0057EC</td> <td>32</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>-</td> <td></td> <td></td> <td></td>	Reserved	0057EC	32						-				
1157EC 128 <			64										
1024FC 256 1<		0157EC	128	_	_	_	_		_	_	_	_	
0557°C 612 0<													
Reserved 007FE 027FE 12 00 00FFE 12 00 00 00 00 000FF0 12 00 00 00 000FF0 12 00 00 00 000FF0 12 00 00 00 000FF0 12 00 00 00 000FF0 12 00 00 00 00 000FF0 12 00 00 00 00 00 00 00 00 00 00 00 00 00													
DAFE 64 01752 128 00576 512 005770 128 005770 128 005770 512 005770 512 005770 512 005770 512 005772 52 005772 52 005772 512 005772 512 005772 512 005772 512 005772 512 005772 512 005772 512 005772 512 005772 512 005772 512 005774 512 005774 512 005774 512 005774 512 005776 512 005776 512 005776 512 005776 512 005776 512 005776 512 005776 512	Reserved												
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00AFF2 64 WDTWIN<1.0> ALTI2C2 ALTI2C1 Reserved ⁽⁹⁾ FWDT 0057F2 512 FWDT 0057F4 32 FWDT WDTWIN<10> PLKEN WDTPRE WDTPOST<3.0>	FDOD												
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FOSCSEL 0057F8 32 00AFF8 64 0157F8 128 128 — IESO PWMLOCK ⁽¹⁾ — — — — FNOSC<2:0> FGS 0057F8 512 - - - - - FNOSC<2:0> FGS 0057FA 32 - - - - - - - FNOSC<2:0> FGS 0057FA 32 - - - - - - - - - - - FNOSC<2:0> FGS 0057FA 32 - <td></td> <td></td> <td>256</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td colspan="2"></td>			256										
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0157FA 128 GCP GWRP 02AFFA 256 GCP GWRP 02AFFA 512 GCP GWRP Reserved 0057FC 128		00AFFA	64										
0557FA 512 Image: Constraint of the symbolic definition of the symbol definitity of the s		0157FA	128	—	—	—	—	—	—	—	GCP	GWRP	
Reserved 0057FC 32 00AFFC 64 0157FC 128 02AFFC 256 0557FC 512 Reserved 057FFE 00AFFE 64 0157FE 128 00AFFE 64 0157FE 128 00AFFE 64 0157FE 128 02AFFE 256		02AFFA	256										
00AFFC 64 0157FC 128 02AFFC 256 0557FC 512 Reserved 057FFE 32 00AFFE 64 0157FE 128 00AFFE 256		0557FA	512										
0157FC 128 -<	Reserved	0057FC	32										
02AFFC 256 0557FC 512 Reserved 057FFE 32 00AFFE 64 0157FE 128 02AFFE 256		00AFFC	64										
02AFFC 256 0557FC 512 Reserved 057FFE 32 00AFFE 64 0157FE 128 02AFFE 256		0157FC	128	_	_	—	_	_	_	_	_	_	
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00AFFE 64 0157FE 128 02AFFE 256	Reserved	057FFE	32										
0157FE 128 — — — — — — — — — — — — — — —													
02AFFE 256				_	_	_	_	_	_	_	_	_	
		0557FE	512										

TABLE 27-1: CONFIGURATION BYTE REGISTER MAP

Legend: — = unimplemented, read as '1'.

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: This bit is reserved and must be programmed as '0'.

3: These bits are reserved and must be programmed as '1'.

27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3:USER ID WORDS REGISTER
MAP

File Name	Address	Bits 23-16	Bits 15-0
FUID0	0x800FF8	_	UID0
FUID1	0x800FFA	_	UID1
FUID2	0x800FFC	_	UID2
FUID3	0x800FFE	_	UID3

Legend: — = unimplemented, read as '1'.

27.3 On-Chip Voltage Regulator

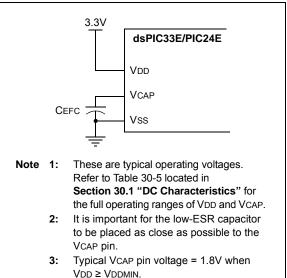
All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an onchip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE

REGULATOR^(1,2,3)



27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

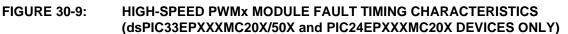
DC CHARACT	ERISTICS		$\begin{array}{ll} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$				
Parameter No.	Тур.	Max.	Units		Conditions		
Operating Cur	rent (IDD) ⁽¹⁾						
DC20d	9	15	mA	-40°C			
DC20a	9	15	mA	+25°C	3.3V	10 MIPS	
DC20b	9	15	mA	+85°C	3.3V		
DC20c	9	15	mA	+125°C			
DC22d	16	25	mA	-40°C			
DC22a	16	25	mA	+25°C	3.3V	20 MIPS	
DC22b	16	25	mA	+85°C		20 1011-5	
DC22c	16	25	mA	+125°C			
DC24d	27	40	mA	-40°C			
DC24a	27	40	mA	+25°C	3.3V	40 MIPS	
DC24b	27	40	mA	+85°C	3.3V	40 1011-5	
DC24c	27	40	mA	+125°C			
DC25d	36	55	mA	-40°C			
DC25a	36	55	mA	+25°C	3.3V	60 MIPS	
DC25b	36	55	mA	+85°C	3.3V	OU IVIIPS	
DC25c	36	55	mA	+125°C	7		
DC26d	41	60	mA	-40°C			
DC26a	41	60	mA	+25°C	3.3V	70 MIPS	
DC26b	41	60	mA	+85°C			

TABLE 30-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

• Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration Word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing while(1) {NOP(); } statement
- · JTAG is disabled



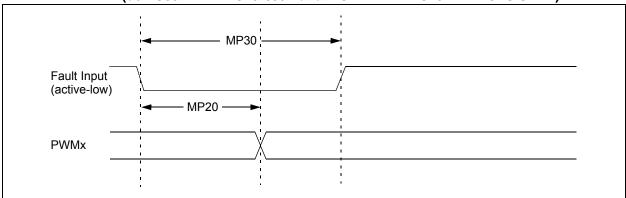


FIGURE 30-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

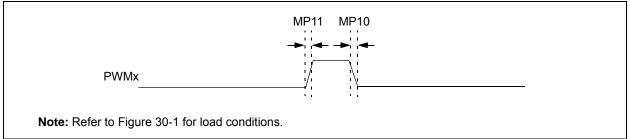


TABLE 30-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Symbol	Characteristic ⁽¹⁾	Min. Typ. Max. Units Conditions				Conditions	
MP10	TFPWM	PWMx Output Fall Time		—	_	ns	See Parameter DO32	
MP11	TRPWM	PWMx Output Rise Time	_	—	_	ns	See Parameter DO31	
MP20	Tfd	Fault Input ↓ to PWMx I/O Change	— — 15 ns					
MP30	Tfh	Fault Input Pulse Width	15	_	_	ns		

Note 1: These parameters are characterized but not tested in manufacturing.

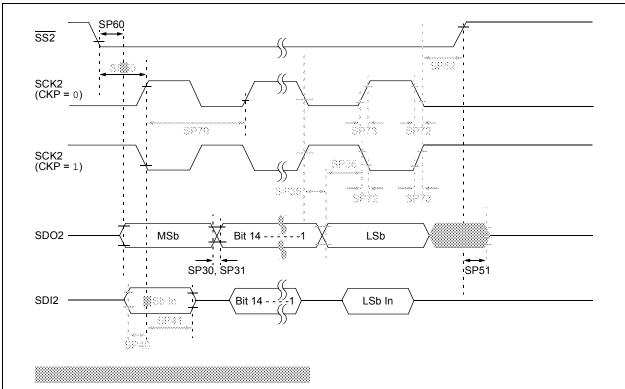


FIGURE 30-19: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

TABLE 30-48:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)TIMING REQUIREMENTS

АС СНА	AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industr} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Exter} \end{array}$					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Min. Typ. ⁽²⁾ Max.		Units	Conditions		
SP70	FscP	Maximum SCK1 Input Frequency	—		11	MHz	(Note 3)		
SP72	TscF	SCK1 Input Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)		
SP73	TscR	SCK1 Input Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)		
SP30	TdoF	SDO1 Data Output Fall Time	_	—	_	ns	See Parameter DO32 (Note 4)		
SP31	TdoR	SDO1 Data Output Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)		
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns			
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	_	ns			
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	_	ns			
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	_	ns			
SP50	TssL2scH, TssL2scL	SS1 ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	_	ns			
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)		
SP52	TscH2ssH, TscL2ssH	SS1	1.5 TCY + 40	—		ns	(Note 4)		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

31.1 High-Temperature DC Characteristics

TABLE 31-1: OPERATING MIPS VS. VOLTAGE

			Max MIPS
Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X
HDC5	3.0 to 3.6V ⁽¹⁾	-40°C to +150°C	40

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules, such as the ADC, may have degraded performance. Device functionality is tested but not characterized.

TABLE 31-2: THERMAL OPERATING CONDITIONS

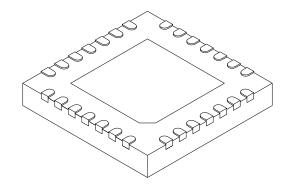
Rating	Symbol	Min	Тур	Max	Unit
High-Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+155	°C
Operating Ambient Temperature Range	TA	-40	_	+150	°C
Power Dissipation: Internal Chip Power Dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ I/O Pin Power Dissipation: $I/O = \Sigma (\{VDD - VOH\} x IOH) + \Sigma (VOL x IOL)$	PD	I	Pint + Pi/c)	W
Maximum Allowed Power Dissipation	n Pdmax (Tj – Ta)/θja			W	

TABLE 31-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$						
Parameter No.	Symbol Characteristic Min Typ Max Units Conditio						Conditions		
Operating V	/oltage								
HDC10	Supply Voltage								
	Vdd	✓DD — 3.0 3.3 3.6 V -40°C to +150°C							

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units					
Dimension	Dimension Limits					
Number of Pins	Ν		28			
Pitch	е		0.65 BSC			
Overall Height	А	0.80	0.90	1.00		
Standoff	A1	0.00	0.02	0.05		
Terminal Thickness	A3		0.20 REF			
Overall Width	Е		6.00 BSC			
Exposed Pad Width	E2	3.65	3.70	4.70		
Overall Length	D		6.00 BSC			
Exposed Pad Length	D2	3.65	3.70	4.70		
Terminal Width	b	0.23	0.30	0.35		
Terminal Length	L	0.30	0.40	0.50		
Terminal-to-Exposed Pad	К	0.20	-	-		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

 $\label{eq:REF:Reference} \ensuremath{\mathsf{REF:}} \ensuremath{\mathsf{Reference}}\xspace \ensuremath{\mathsf{Dimension}}, \ensuremath{\mathsf{usually}}\xspace \ensuremath{\mathsf{vithout}}\xspace \ensuremath{\mathsf{toterance}}\xspace, \ensuremath{\mathsf{for}}\xspace \ensuremath{\mathsf{oterance}}\xspace \ensuremath{\mathsf{vithout}}\xspace \ensuremath{\mathsf{toterance}}\xspace \ensuremath{\mathsf{vithout}}\xspace \ensuremath{\mathsf{vithout}}\xspace \ensuremath{\mathsf{vithout}}\xspace \ensuremath{\mathsf{rescale}}\xspace \ensuremath{\mathsf{vithout}}\xspace \ensuremath{\mathsf{vithout}}\xspace \ensuremath{\mathsf{vithout}}\xspace \ensuremath{\mathsf{vithout}}\xspace \ensuremath{\mathsf{toterance}}\xspace \ensuremath{\mathsf{vithout}}\xspace \ensuremath{$

Microchip Technology Drawing C04-124C Sheet 2 of 2

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units				
Dimensior	Dimension Limits				
Contact Pitch	E		0.40 BSC		
Optional Center Pad Width	W2			4.45	
Optional Center Pad Length	T2			4.45	
Contact Pad Spacing	C1		6.00		
Contact Pad Spacing	C2		6.00		
Contact Pad Width (X28)	X1			0.20	
Contact Pad Length (X28) Y1				0.80	
Distance Between Pads	0.20				

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

PMD (PIC24EPXXXMC20X Devices)	
PORTA (PIC24EPXXXGP/MC202,	
dsPIC33EPXXXGP/MC202/502 Devices) 104	,
PORTA (PIC24EPXXXGP/MC203,	
dsPIC33EPXXXGP/MC203/503 Devices) 103	5
PORTA (PIC24EPXXXGP/MC204,	
dsPIC33EPXXXGP/MC204/504 Devices) 102	,
PORTA (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices)	,
PORTB (PIC24EPXXXGP/MC202,	,
dsPIC33EPXXXGP/MC202/502 Devices) 104	
PORTB (PIC24EPXXXGP/MC203,	
dsPIC33EPXXXGP/MC203/503 Devices) 103	5
PORTB (PIC24EPXXXGP/MC204,	
dsPIC33EPXXXGP/MC204/504 Devices) 102	2
PORTB (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices)	,
PORTC (PIC23EPXXXGP/MC203,	
dsPIC33EPXXXGP/MC203/503 Devices) 103	ł
PORTC (PIC24EPXXXGP/MC204,	,
dsPIC33EPXXXGP/MC204/504 Devices) 102	
PORTC (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices))
PORTD (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices) 100)
PORTE (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices) 100)
PORTF (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices) 100	`
,	,
PORTG (PIC24EPXXXGP/MC206 and	
dsPIC33EPXXXGP/MC206/506 Devices) 101	
PTG78	5
PWM (dsPIC33EPXXXMC20X/50X,	
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PIC24EPXXXMC20X Devices)79 PWM Generator 1 (dsPIC33EPXXXMC20X/50X,	
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