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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8×8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mc204t-i-ml

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## **Pin Diagrams (Continued)**



Pin Name <sup>(4)</sup>	Pin Type	Buffer Type	PPS	Description
U2CTS	1	ST	No	UART2 Clear-To-Send.
U2RTS	0		No	UART2 Ready-To-Send.
U2RX	I.	ST	Yes	UART2 receive.
U2TX	Ó	_	Yes	UART2 transmit.
BCLK2	Ō	ST	No	UART2 IrDA <sup>®</sup> baud clock output.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	0	—	No	SPI1 data out.
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	0	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS <sup>(5)</sup>	Ι	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	0	_	No	JTAG test data output pin.
C1RX <sup>(2)</sup>	I	ST	Yes	ECAN1 bus receive pin.
C1TX <sup>(2)</sup>	0	_	Yes	ECAN1 bus transmit pin.
FLT1 <sup>(1)</sup> , FLT2 <sup>(1)</sup>	I	ST	Yes	PWM Fault Inputs 1 and 2.
FLT3 <sup>(1)</sup> , FLT4 <sup>(1)</sup>	I	ST	No	PWM Fault Inputs 3 and 4.
FLT32 <sup>(1,3)</sup>	I	ST	No	PWM Fault Input 32 (Class B Fault).
DTCMP1-DTCMP3 <sup>(1)</sup>	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 through 3.
PWM1L-PWM3L <sup>(1)</sup>	0	—	No	PWM Low Outputs 1 through 3.
PWM1H-PWM3H <sup>(1)</sup>	0	—	No	PWM High Outputs 1 through 3.
SYNCI1 <sup>(1)</sup>	I	ST	Yes	PWM Synchronization Input 1.
SYNCO1 <sup>(1)</sup>	0	—	Yes	PWM Synchronization Output 1.
INDX1 <sup>(1)</sup>	Ι	ST	Yes	Quadrature Encoder Index1 pulse input.
HOME1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Home1 pulse input.
QEA1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer
(4)				external clock/gate input in Timer mode.
QEB1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Phase B input in QEI1 mode. Auxiliary timer
				external clock/gate input in Timer mode.
CNTCMP1''	υ	—	Yes	Quadrature Encoder Compare Output 1.

## TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

 Legend:
 CMOS = CMOS compatible input or output
 Analog = Analog input

 ST = Schmitt Trigger input with CMOS levels
 O = Output

 PPS = Peripheral Pin Select
 TTL = TTL input buffer

P = Power I = Input

Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This pin is available on dsPIC33EPXXXGP/MC50X devices only.

3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)" for more information.

4: Not all pins are available in all packages variants. See the "Pin Diagrams" section for pin availability.

5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.





## TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL		0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	_		_	_	_	_	_	_	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	_	_	_	_	_		_	_	_	_	DAE	DOOVR	_	_	_	_	0000
INTCON4	08C6					_	_			_				_	—		SGHT	0000
INTTREG	08C8						ILR<	3:0>					VECNU	M<7:0>				0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## TABLE 4-19: SPI1 AND SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	:	SPIBEC<2:0	)>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI1CON1	0242	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	—	_	_	_	FRMDLY	SPIBEN	0000
SPI1BUF	0248							SPI1 Tra	ansmit and F	Receive Buf	fer Registe	r						0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	:	SPIBEC<2:0	)>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI2CON1	0262	_	—		DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	—	_	_	_	FRMDLY	SPIBEN	0000
SPI2BUF	0268							SPI2 Tra	ansmit and F	Receive Buf	fer Registe	r						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# TABLE 4-27: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC204/504 AND PIC24EPXXXGP/MC204 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
RPOR0	0680					RP35	R<5:0>			_	_			RP20	R<5:0>			0000	
RPOR1	0682	—	—			RP37I	R<5:0>			—				RP36	R<5:0>				
RPOR2	0684	—	—			RP39	R<5:0>			_	_	RP38R<5:0>						0000	
RPOR3	0686	_	_			RP41	R<5:0>			—	_			RP40	R<5:0>			0000	
RPOR4	0688	_	_			RP43	R<5:0>			—	_	RP42R<5:0>						0000	
RPOR5	068A	_	_			RP55I	R<5:0>	— — RP54R<5:0>								0000			
RPOR6	068C	_	_			RP57	R<5:0>			_	—			RP56	R<5:0>			0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## TABLE 4-28: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC206/506 AND PIC24EPXXXGP/MC206 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—			RP35	R<5:0>			_	_			RP20I	R<5:0>			0000
RPOR1	0682	_	_			RP37	R<5:0>			_	_			RP36	R<5:0>			0000
RPOR2	0684	_	_			RP39	R<5:0>			—	—			RP38	R<5:0>			0000
RPOR3	0686	_	_			RP41	R<5:0>			—	—			RP40	R<5:0>			0000
RPOR4	0688	_	_			RP43	R<5:0>			—	—			RP42I	R<5:0>			0000
RPOR5	068A	_	_			RP55I	R<5:0>			—	—			RP54I	R<5:0>			0000
RPOR6	068C	_	_			RP57I	R<5:0>			—	—			RP56I	R<5:0>			0000
RPOR7	068E	_	_			RP97	R<5:0>			—	—	_	_	_	_	_	_	0000
RPOR8	0690	_	_			RP118	R<5:0>			—	—	_	_	_	_	_	_	0000
RPOR9	0692	_	_	_	_	_	_	_	_	_	_			RP120	R<5:0>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



## TABLE 4-64: BIT-REVERSED ADDRESSING SEQUENCE (16-ENTRY)

		Norma	al Addre	SS			Bit-Rev	ersed Ac	ldress
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

## 4.8 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture uses a 24-bit-wide Program Space (PS) and a 16-bit-wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices provides two methods by which Program Space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

## TABLE 4-65: PROGRAM SPACE ADDRESS CONSTRUCTION

	Access	Program Space Address									
Access Type	Space	<23>	<22:16>	<15>	<14:1>	<0>					
Instruction Access	User	0		PC<22:1>		0					
(Code Execution)			0xx xxxx xx	xx xxxx	xxxx xxx0						
TBLRD/TBLWT	D/TBLWT User TBLPAG<7:0> Data EA<15										
(Byte/Word Read/Write)		0	xxx xxxx	xxxx xxx	x xxxx xxxx						
	Configuration	TB	LPAG<7:0>		Data EA<15:0>						
		1	XXX XXXX	XXXX XX	xx xxxx xxxx						

## FIGURE 4-22: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR <sup>(1)</sup>	OVBERR <sup>(1)</sup>	COVAERR <sup>(1)</sup>	COVBERR <sup>(1)</sup>	OVATE <sup>(1)</sup>	OVBTE <sup>(1)</sup>	COVTE <sup>(1)</sup>
bit 15							bit 8
r							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR <sup>(1</sup>	) DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0
[							
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpleme	ented bit, read a	as '0'	
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is clea	red	x = Bit is unk	nown
bit 15	NSTDIS: Inte	errupt Nesting	Disable bit				
	$\perp$ = Interrupt 0 = Interrupt	nesting is disa	ibled				
bit 14	OVAFRR: A	ccumulator A (	Overflow Trap F	lag bit(1)			
2	1 = Trap was	s caused by ov	erflow of Accur	nulator A			
	0 = Trap was	s not caused b	y overflow of A	ccumulator A			
bit 13	OVBERR: A	ccumulator B (	Overflow Trap F	lag bit <sup>(1)</sup>			
	1 = Trap was	s caused by ow	erflow of Accur	nulator B			
	0 = Irap was	s not caused b	y overflow of A	ccumulator B	(1)		
bit 12	COVAERR:	Accumulator A	Catastrophic (	Jverflow Trap FI	ag bit("		
	1 = Trap was 0 = Trap was	s not caused by ca	v catastrophic over	overflow of Accu	mulator A		
bit 11	COVBERR:	Accumulator E	Catastrophic (	Overflow Trap Fl	ag bit <sup>(1)</sup>		
	1 = Trap was	s caused by ca	tastrophic over	flow of Accumul	ator B		
	0 = Trap was	s not caused b	y catastrophic o	overflow of Accu	mulator B		
bit 10	OVATE: Acc	umulator A Ov	erflow Trap En	able bit <sup>(1)</sup>			
	1 = Trap ove	rflow of Accun	nulator A				
hit 0			orflow Tran En	able bit(1)			
DIL 9	1 = Tran ove	rflow of Accun	nulator B				
	0 = Trap is d	isabled					
bit 8	COVTE: Cat	astrophic Ove	rflow Trap Enat	ole bit <sup>(1)</sup>			
	1 = Trap on o	catastrophic ov	erflow of Accu	mulator A or B is	s enabled		
	0 = Trap is d	isabled					
bit 7	SFTACERR:	Shift Accumu	lator Error Statu	us bit <sup>(1)</sup>			
	1 = Math erro	or trap was ca or trap was po	used by an inva t caused by an	alid accumulator	shift ator shift		
bit 6		ivide-hv-Zero	Error Status bit				
bit o	1 = Math erro	or trap was ca	used by a divide	e-bv-zero			
	0 = Math erro	or trap was no	t caused by a d	ivide-by-zero			
bit 5	DMACERR:	DMAC Trap F	lag bit				
	1 = DMAC tr	ap has occurre	ed				
	0 = DMAC tr	ap has not occ	curred				
Note 1: The	ese bits are ava	ailable on dsPl	C33EPXXXMC	20X/50X and de	PIC33EPXXX	GP50X devices	s only.

## REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

## 11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See the **"Pin Diagrams"** section for the available 5V tolerant pins and Table 30-11 for the maximum VIH specification for each pin.

## 11.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

### 11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP, as shown in Example 11-1.

## **11.3** Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the Change Notification (CN) functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pulldowns act as a current source or sink source connected to the pin and eliminate the need for external resistors when push button, or keypad devices are connected. The pull-ups and pull-downs are enabled separately, using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note:	Pull-ups and pull-downs on Change Noti-
	fication pins should always be disabled
	when the port pin is configured as a digital
	output.

#### EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

MOV	0xFF00, W0	; Configure PORTB<15:8>
		; as inputs
MOV	W0, TRISB	; and PORTB<7:0>
		; as outputs
NOP		; Delay 1 cycle
BTSS	PORTB, #13	; Next Instruction

## REGISTER 11-15: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

	5444.0	D 44/ 0	<b>D</b> 444 0		D 44/ 0	D 444 0			
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—				SYNCI1R<6:0	)>				
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	—		—	—	—	—		
bit 7				-	•		bit 0		
Legend:									
R = Readabl	le bit	W = Writable b	oit	U = Unimpler	mented bit, read	l as '0'	· <b>'</b> 0'		
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkn	iown		
bit 15	Unimplemer	nted: Read as '0	)'						
bit 14-8	SYNCI1R<6: (see Table 11	• <b>0&gt;:</b> Assign PWI I-2 for input pin :	VI Synchroniz selection nur	zation Input 1 to nbers)	o the Correspon	ding RPn Pin b	its		
	1111001 <b>=  </b>	nput tied to RPI	121						
	•								
	•								
	0000001 = I	nout tied to CME	21						
	0000000 = 1	nput tied to Vss							
bit 7-0	Unimplemer	nted: Read as '0	)'						

### REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER<sup>(1)</sup>

- bit 7-3 FLTSRC<4:0>: Fault Control Signal Source Select for PWM Generator # bits 11111 = Fault 32 (default) 11110 = Reserved . . 01100 = Reserved 01011 = Comparator 4 01010 = Op Amp/Comparator 3
  - 01001 = Op Amp/Comparator 2
  - 01000 = Op Amp/Comparator 1
  - 00111 = Reserved
  - 00110 = Reserved
  - 00101 = Reserved
  - 00100 = Reserved
  - 00011 = Fault 4
  - 00010 = Fault 3
  - 00001 = Fault 2 00000 = Fault 1
- bit 2 **FLTPOL:** Fault Polarity for PWM Generator # bit<sup>(2)</sup>
  - 1 = The selected Fault source is active-low
    - 0 = The selected Fault source is active high
- bit 1-0 **FLTMOD<1:0>:** Fault Mode for PWM Generator # bits
  - 11 = Fault input is disabled
  - 10 = Reserved
  - 01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
  - 00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)
- **Note 1:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.
  - **2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXH	LD<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXH	HLD<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkı	nown

## REGISTER 17-10: INDX1HLD: INDEX COUNTER 1 HOLD REGISTER

bit 15-0 INDXHLD<15:0>: Hold Register for Reading and Writing INDX1CNTH bits

## REGISTER 17-11: QEI1ICH: QEI1 INITIALIZATION/CAPTURE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIIC	<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIIC	<23:16>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'			
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is			x = Bit is unkr	nown			
1							

bit 15-0 **QEIIC<31:16>:** High Word Used to Form 32-Bit Initialization/Capture Register (QEI1IC) bits

### REGISTER 17-12: QEI1ICL: QEI1 INITIALIZATION/CAPTURE LOW WORD REGISTER

				10000	17/04-0	R/W-U	R/W-0
			QEIIO	C<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEII	C<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit		W = Writable b	it	U = Unimplen	nented bit, rea	d as '0'	
-n = Value at POR (1' = Bit is set			'0' = Bit is clea	ared	x = Bit is unkr	nown	

bit 15-0 **QEIIC<15:0>:** Low Word Used to Form 32-Bit Initialization/Capture Register (QEI1IC) bits

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—		—	AMSK9	AMSK8
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0
bit 7							bit 0

## REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 Unimplemented: Read as '0'

bit 9-0

AMSK<9:0>: Address Mask Select bits

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax + 1; bit match is required in this position

# REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER (CONTINUED)

bit 3 ABEN: AND Gate B Input Enable bit 1 = MBI is connected to AND gate 0 = MBI is not connected to AND gate bit 2 ABNEN: AND Gate B Input Inverted Enable bit 1 = Inverted MBI is connected to AND gate 0 = Inverted MBI is not connected to AND gate bit 1 AAEN: AND Gate A Input Enable bit 1 = MAI is connected to AND gate 0 = MAI is not connected to AND gate bit 0 AANEN: AND Gate A Input Inverted Enable bit 1 = Inverted MAI is connected to AND gate 0 = Inverted MAI is not connected to AND gate

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	
_	CVR2OE <sup>(1)</sup>	—	—	—	VREFSEL	—	—	
bit 15							bit 8	
R/W-0	) R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
CVRE	N CVR1OE <sup>(1)</sup>	CVRR	CVRSS <sup>(2)</sup>	CVR3	CVR2	CVR1	CVR0	
bit 7							bit 0	
Legend:								
R = Read	able bit	W = Writable	bit	U = Unimple	mented bit, read	i as '0'		
-n = Value	e at POR	'1' = Bit is set	t	'0' = Bit is cle	eared	x = Bit is unkr	Iown	
bit 15	Unimplemen	ted: Read as '	0'		(1)			
bit 14	CVR2OE: Co	mparator Volta	ige Reference	2 Output Ena	ble bit <sup>(1)</sup>			
	1 = (AVDD - A 0 = (AVDD - A	AVSS)/2 is conr AVSS)/2 is disce	nected to the C	VREF20 pin the CVREF20	pin			
bit 13-11	Unimplemen	ted: Read as '	0'		•			
bit 10	VREFSEL: C	omparator Voli	tage Reference	e Select bit				
	1 = CVREFIN :	= VREF+	-					
	0 = CVREFIN i	s generated by	y the resistor n	etwork				
bit 9-8	Unimplemen	ted: Read as '	0'					
bit 7	CVREN: Con	nparator Voltag	je Reference E	nable bit				
	1 = Compara	tor voltage refe	erence circuit is	s powered on	wn			
bit 6	CVR1OF: Co	mparator Volta	age Reference	1 Output Ena	ble bit(1)			
bit o	1 = Voltage le	evel is output o	n the CVRFF10					
	0 = Voltage le	evel is disconne	ected from the	n CVREF10 pi	'n			
bit 5	CVRR: Comp	arator Voltage	Reference Ra	inge Selectior	n bit			
	1 = CVRSRC/2	24 step-size						
	0 = CVRSRC/3	32 step-size						
bit 4	CVRSS: Com	parator Voltag	e Reference S	ource Selecti	on bit <sup>(2)</sup>			
	1 = Compara 0 = Compara	1 = Comparator voltage reference source, CVRSRC = (VREF+) – (AVSS) 0 = Comparator voltage reference source, CVRSPC = AVDD – AVSS						
bit 3-0	CVR<3:0> Co	CVR<3.0> Comparator Voltage Reference Value Selection $0 < CVR<3.0> < 15$ hits						
	When $CVRR = 1$ :							
	CVREFIN = (C	VR<3:0>/24) •	(CVRSRC)					
	When CVRR	= 0:						
	CVREFIN = (C	VRSRC/4) + (C	VR<3:0>/32) •	(CVRSRC)				
Note 1:	CVRxOE overrides	s the TRISx an	d the ANSELx	bit settinas.				

## REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

- 2: In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

## REGISTER 27-1: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R
			DEVID<2	3:16> <b>(1)</b>			
bit 23							bit 16
R	R	R	R	R	R	R	R
			DEVID<1	15:8> <b>(1)</b>			
bit 15							bit 8
R	R	R	R	R	R	R	R
			DEVID<	7:0>(1)			
bit 7							bit 0
Legend:	R = Read-Only bit			U = Unimplen	nented bit		

bit 23-0 **DEVID<23:0>:** Device Identifier bits<sup>(1)</sup>

**Note 1:** Refer to the "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration *Bits*" (DS70663) for the list of device ID values.

## **REGISTER 27-2: DEVREV: DEVICE REVISION REGISTER**

R	R	R	R	R	R	R	R
			DEVREV<	<23:16> <sup>(1)</sup>			
bit 23							bit 16
R	R	R	R	R	R	R	R
			DEVREV	<15:8> <b>(1)</b>			
bit 15							bit 8
R	R	R	R	R	R	R	R
			DEVRE	/<7:0> <sup>(1)</sup>			
bit 7							bit 0
Legend:	R = Read-only bit			U = Unimpler	nented bit		

## bit 23-0 **DEVREV<23:0>:** Device Revision bits<sup>(1)</sup>

**Note 1:** Refer to the "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration *Bits*" (DS70663) for the list of device revision values.



#### **FIGURE 30-3: I/O TIMING CHARACTERISTICS**

## TABLE 30-21: I/O TIMING REQUIREMENTS

AC CHAR	ACTERISTI	CS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature } -40^\circ C \leq T_A \leq +85^\circ C \mbox{ for Industrial} \\ -40^\circ C \leq T_A \leq +125^\circ C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic	Min. Typ. <sup>(1)</sup> Max. Units Conditions			Conditions	
DO31	TIOR	Port Output Rise Time	_	5	10	ns	
DO32	TIOF	Port Output Fall Time	—	5	10	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	_		ns	
DI40	TRBP	CNx High or Low Time (input)	2		_	TCY	

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

#### FIGURE 30-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS





## FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

## **Revision D (December 2011)**

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

## TABLE A-3: MAJOR SECTION UPDATES

Section Name	Update Description
"16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High- Speed PWM, Op amps, and Advanced Analog"	Removed the Analog Comparators column and updated the Op amps/Comparators column in Table 1 and Table 2.
Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
Section 30.0 "Electrical Characteristics"	Updated the VBOR specifications and/or its related note in the following electrical characteristics tables: • Table 30-1 • Table 30-4 • Table 30-12 • Table 30-14 • Table 30-15 • Table 30-16 • Table 30-56 • Table 30-57 • Table 30-58 • Table 30-59 • Table 30-60