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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mc206t-e-mr

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4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in wordaddressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-6).

Program memory addresses are always word-aligned on the lower word and addresses are incremented, or decremented by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices reserve the addresses between 0x000000 and 0x000200 for hardcoded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 7.1** "Interrupt Vector Table".



FIGURE 4-6: PROGRAM MEMORY ORGANIZATION

REGISTER 8-3: DMAXSTAH: DMA CHANNEL X START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—		—	—	—	—	—	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STA<	23:16>			
bit 7							bit 0
Legend:							
R = Readable b	it	W = Writable bi	t	U = Unimplei	mented bit read	d as '0'	

•••			-		
-n =	= Value at POR	'1' = Bit is set	'0' =	Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 STA<23:16>: Primary Start Address bits (source or destination)

REGISTER 8-4: DMAXSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STA	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STA	<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at P	' OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown

bit 15-0 STA<15:0>: Primary Start Address bits (source or destination)

9.1 CPU Clocking System

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X family of devices provides six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase Locked Loop (PLL)
- · FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- · Low-Power RC (LPRC) Oscillator

Instruction execution speed or device operating frequency, FCY, is given by Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

FCY = Fosc/2

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (FIN) and output frequency (FPLLO). In clock modes S1 and S3, when the PLL output is selected, FOSC = FPLLO.

Equation 9-3 provides the relationship between input frequency (FIN) and VCO frequency (FVCO).



EQUATION 9-2: FPLLO CALCULATION

$$FPLLO = FIN \times \left(\frac{M}{N1 \times N2}\right) = FIN \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)}\right)$$

Where:

N1 = PLLPRE + 2 $N2 = 2 \times (PLLPOST + 1)$

M = PLLDIV + 2

EQUATION 9-3: Fvco CALCULATION

$$Fvco = FIN \times \left(\frac{M}{N1}\right) = FIN \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)}\right)$$

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FIGURE 9-2: PLL BLOCK DIAGRAM

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—			RP57	R<5:0>		
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—			RP56	R<5:0>		
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimplem	nented bit, rea	d as '0'	
-n = Value a	t POR	'1' = Bit is set	t	'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-14	Unimpleme	nted: Read as '	0'				
bit 13-8	RP57R<5:0> (see Table 1 [*]	 Peripheral Out 1-3 for peripheral 	utput Functior al function nu	n is Assigned to mbers)	RP57 Output	Pin bits	
bit 7-6	Unimpleme	nted: Read as '	0'				

REGISTER 11-24: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

(see Table	11-3 for peripheral function numbers)	

REGISTER 11-25: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP97	R<5:0>		
bit 15							bit 8

RP56R<5:0>: Peripheral Output Function is Assigned to RP56 Output Pin bits

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8 **RP97R<5:0>:** Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-0 Unimplemented: Read as '0'

bit 5-0

16.1.2 WRITE-PROTECTED REGISTERS

On dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FOSCSEL<6>). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring, PWMLOCK = 0. To gain write access to these locked registers, the user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

The correct unlocking sequence is described in Example 16-1.

EXAMPLE 16-1: PWMx WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

; FLT32 pin must be p	ulled low externally in order to clear and disable the fault
; Writing to FCLCON1 :	register requires unlock sequence
<pre>mov #0xabcd,w10 mov #0x4321,w11 mov #0x0000,w0 mov w10, PWMKEY mov w11, PWMKEY mov w0,FCLCON1</pre>	<pre>; Load first unlock key to w10 register ; Load second unlock key to w11 register ; Load desired value of FCLCON1 register in w0 ; Write first unlock key to PWMKEY register ; Write second unlock key to PWMKEY register ; Write desired value to FCLCON1 register</pre>
; Set PWM ownership as	nd polarity using the IOCON1 register
; Writing to IOCON1 re	egister requires unlock sequence
<pre>mov #0xabcd,w10 mov #0x4321,w11 mov #0xF000,w0 mov w10, PWMKEY mov w11, PWMKEY mov w0,IOCON1</pre>	<pre>; Load first unlock key to w10 register ; Load second unlock key to w11 register ; Load desired value of IOCON1 register in w0 ; Write first unlock key to PWMKEY register ; Write second unlock key to PWMKEY register ; Write desired value to IOCON1 register</pre>

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	_		DTRx<13:8>					
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			DTR	2x<7:0>				
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			oit	U = Unimplemented bit, read as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown				

REGISTER 16-10: DTRx: PWMx DEAD-TIME REGISTER

bit 15-14 Unimplemented: Read as '0'

bit 13-0 DTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 16-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
—	—		ALTDTRx<13:8>							
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
			ALTDT	Rx<7:0>						
bit 7							bit 0			
Legend:										
R = Readable bit W = Writable bit				U = Unimplemented bit, read as '0'						
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown			

bit 15-14 Unimplemented: Read as '0'

bit 13-0 ALTDTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 17-3: QEI1STAT: QEI1 STATUS REGISTER (CONTINUED)

bit 2	HOMIEN: Home Input Event Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled
bit 1	IDXIRQ: Status Flag for Index Event Status bit 1 = Index event has occurred 0 = No Index event has occurred
bit 0	IDXIEN: Index Input Event Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled

Note 1: This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

REGISTER 17-17: INT1TMRH: INTERVAL 1 TIMER HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
			INTTM	R<31:24>							
bit 15							bit 8				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
	INTTMR<23:16>										
bit 7							bit 0				
Legend:											
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'								
-n = Value at POR (1' = Bit is set (0' = Bit is cleared x = Bit is unknown					nown						

bit 15-0 INTTMR<31:16>: High Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

REGISTER 17-18: INT1TMRL: INTERVAL 1 TIMER LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
	INTTMR<15:8>										
bit 15							bit 8				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
	INTTMR<7:0>										
bit 7							bit 0				
Legend:											
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'								
-n = Value at POR '1' = Bit is set				'0' = Bit is cleared x = Bit is unknown							

bit 15-0 INTTMR<15:0>: Low Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits





REGISTER 21-2: CxC1	RL2: ECANx CON	TROL REGISTER 2
---------------------	----------------	-----------------

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
	_	_	_	_	_	_	_			
bit 15							bit 8			
							,			
U-0	U-0	U-0	R-0	R-0 R-0		R-0	R-0			
—	—	—	DNCNT4	DNCNT3	DNCNT2	DNCNT1	DNCNT0			
bit 7 bit 0										
Legend:										
R = Readable I	bit	W = Writable	bit	U = Unimplemented bit, read as '0'						
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown				
bit 15-5	Unimplemen	ted: Read as '	0'							
bit 4-0	DNCNT<4:0>	: DeviceNet™	Filter Bit Num	ber bits						
	10010-1111	1 = Invalid sele	ection							
	10001 = Com	pares up to Da	ata Byte 3, bit	6 with EID<17	>					
	•									
	•									
	•									
	00001 = Compares up to Data Byte 1, bit 7 with EID<0> 00000 = Does not compare data bytes									

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0			
DMABS2	DMABS1	DMABS0	—	_	_		—			
bit 15	•	•					bit 8			
U-0	U-0 U-0 U-0 R/W-0 F			R/W-0	R/W-0	R/W-0	R/W-0			
	—	—	FSA4	FSA3	FSA2	FSA1	FSA0			
bit 7 bit										
Legend:										
R = Readable	bit	W = Writable I	bit	U = Unimplei	mented bit, read	l as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown			
bit 15-13 bit 12-5 bit 4-0	DMABS<2:0> 111 = Reserv 110 = 32 buff 101 = 24 buff 100 = 16 buff 011 = 12 buff 010 = 8 buffe 001 = 6 buffe 000 = 4 buffe Unimplemen FSA<4:0>: FI 11111 = Rea 11110 = Rea	>: DMA Buffer S red fers in RAM fers in RAM fers in RAM rs in RAM rs in RAM rs in RAM ted: Read as for IFO Area Starts d Buffer RB31 d Buffer RB30	Size bits)' s with Buffer b	its						

REGISTER 21-4: CxFCTRL: ECANx FIFO CONTROL REGISTER

23.4 ADC Control Registers

REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0				
ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0				
bit 15						-	bit 8				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC, HS	R/C-0, HC, HS				
SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE ⁽³⁾				
bit 7						-	bit 0				
Legend:		HC = Hardwa	re Clearable bit	HS = Hardwa	re Settable bit	C = Clearable bi	t				
R = Readab	le bit	W = Writable I	bit	U = Unimpler	nented bit, read	d as '0'					
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknow	vn				
bit 15	ADON: ADO	C1 Operating N	lode bit								
	1 = ADC module is operating										
	0 = ADC is off										
bit 14	Unimplemented: Read as '0'										
bit 13	ADSIDL: ADC1 Stop in Idle Mode bit										
	1 = Disconti	inues module o	peration when	device enters	Idle mode						
	0 = Continues module operation in Idle mode										
bit 12	ADDMABM	: DMA Buffer E	Build Mode bit								
	1 = DMA b	uffers are writte	en in the order	of conversion	; the module p	provides an addre	ess to the DMA				
	0 = DMA bi	uffers are writte	en in Scatter/Ga	ther mode: the	e module prov	ides a Scatter/Ga	ther address to				
	the DM	A channel, bas	ed on the index	of the analog	input and the	size of the DMA	ouffer.				
bit 11	Unimpleme	ented: Read as	'0'								
bit 10	AD12B: AD	C1 10-Bit or 12	2-Bit Operation	Mode bit							
	1 = 12-bit, 1	-channel ADC	operation								
	0 = 10-bit, 4	-channel ADC	operation								
bit 9-8	FORM<1:0	>: Data Output	Format bits								
	For 10-Bit C	Operation:									
	11 = Signed	d fractional (Do	UT = sddd ddd	ld dd00 000	0, where $s = $.	NOT.d<9>)					
	10 = Fractions	hai (DOUT = ac	iaa aaaa aau = cccc cccd		where $c = N($	(<0>b TC					
	00 = Intege	r (Dout = 0000	00dd dddd	dddd)		51.u (0 ²)					
	For 12-Bit C	Deration:		,							
	11 = Signed	fractional (Do	UT = sddd ddd	ld dddd 000	0, where $s = .$	NOT.d<11>)					
	10 = Fractic	onal (Dout = do	ldd dddd ddd	ld 0000)							
	01 - 5 Signed integer (DOUT = SSSS SAAA AAAA AAAA, WHEre S = .NOT.U<17) 00 = Integer (DOUT = 0000, dddd, dddd, dddd)										
		. (2001 - 0000		adduj							
Note 1: S	See Section 24	1.0 "Peripheral	l Trigger Gene	rator (PTG) M	odule" for info	ormation on this s	election.				

- 2: This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 3: Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

R/W-0	R/W	-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0			
VCFG2	VCFC	G1	VCFG0		_	CSCNA	CHPS1	CHPS0			
bit 15								bit 8			
R-0	R/W	-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
BUFS	SMP	14	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS			
bit 7								bit 0			
Legend:											
R = Readable	e bit		W = Writable	bit	U = Unimpl	emented bit, read	d as '0'				
-n = Value at	POR		'1' = Bit is set		'0' = Bit is c	cleared	x = Bit is unk	nown			
bit 15-13	VCFG<	VCFG<2:0>: Converter Voltage Reference Configuration bits									
	Value		VREFH	VREFL							
	000		Avdd	Avss							
	001	Ext	ernal VREF+	Avss							
	010		Avdd	External VRE	F-						
	011	Ext	ernal VREF+	External VRE	F-						
	lxx		Avdd	Avss							
bit 12-11	Unimple	emen	ted: Read as '	0'							
bit 10	CSCNA	CSCNA: Input Scan Select bit									
	1 = Scans inputs for CH0+ during Sample MUXA 0 = Does not scan inputs										
bit 9-8	CHPS<	CHPS<1:0>: Channel Select bits									
	<u>In 12-bit</u>	In 12-bit mode (AD21B = 1), the CHPS<1:0> bits are Unimplemented and are Read as '0':									
	1x = Co 01 = Co 00 = Co	1x = Converts CH0, CH1, CH2 and CH3 01 = Converts CH0 and CH1 00 = Converts CH0									
bit 7	BUFS:	Buffer	Fill Status bit	onlv valid wher	BUFM = 1)					
	1 = ADC is currently filling the second half of the buffer; the user application should access data in the										
	first 0 = AD sec	 a provide the second half of the buffer a ADC is currently filling the first half of the buffer; the user application should access data in the second half of the buffer 									
bit 6-2	SMPI<4	: 0>:	ncrement Rate	bits							
	When A	DDM/	AEN = 0:								
	x1111 =	= Gen	erates interrup	t after completion	on of every	16th sample/conv	ersion operation	on			
	x1110 =	= Gen	erates interrup	t after completion	on of every	15th sample/conv	ersion operation	on			
	•										
	•										
	x0001 = x0000 =	= Gen = Gen	erates interrup erates interrup	t after completion t after completion	on of every 2 on of every 3	2nd sample/conv sample/conversic	ersion operation	n			
	When A	DDM/	AEN = 1:								
	11111 =	= Incre	ements the DM	IA address after	completion	of every 32nd sa	ample/conversi	ion operation			
	11110 = Increments the DMA address after completion of every 31st sample/conversion operation										
	•										
	•										
	00001 = 00000 =	= Incre = Incre	ements the DM ements the DM	IA address aftei IA address aftei	^r completion ^r completion	of every 2nd sar	nple/conversio /conversion op	n operation eration			

. . ACOND. ADCA CONTROL DECISTED 2

					-						
R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0				
CON	COE ⁽²⁾	CPOL	_		OPMODE	CEVT	COUT				
bit 15						•	bit 8				
R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0				
EVPOL1	EVPOL0		CREF ⁽¹⁾	—	_	CCH1 ⁽¹⁾	CCH0 ⁽¹⁾				
Lbit 7 bit C											
Legend:											
R = Readable	bit	W = Writable	bit		mented bit, read	as '0'					
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	IOWN				
bit 1E		n/Comporator	Enabla bit								
DIL 15		ip/Comparator is e									
	$\perp = Op amp/comparator is enabled 0 = Op amp/comparator is disabled$										
bit 14	COE: Comparator Output Enable bit ⁽²⁾										
	1 = Compara	itor output is pr	esent on the C	xOUT pin							
	0 = Comparator output is internal only										
bit 13	CPOL: Comp	parator Output	Polarity Select	bit							
	1 = Compara	tor output is inv	verted								
h: 40 44	0 = Compara	itor output is no	o, inverted								
		ited: Read as	0 	- Maria Oalart							
DIT 10		p Amp/Compa	rator Operation	n Mode Select	DIT						
	1 = Circuit op 0 = Circuit op	perates as an o	p amp mparator								
bit 9	CEVT: Comp	arator Event bi	t								
	1 = Compara	ator event acco	ording to the E	VPOL<1:0> se	ettings occurred	; disables futur	e triggers and				
	interrupt	s until the bit is	cleared								
	0 = Compara	ator event did n	ot occur								
bit 8	COUT: Comp	parator Output I	oit								
	<u>When CPOL</u> 1 = Vin + > Vi		ed polarity):								
	0 = VIN + < VI	IN-									
	When CPOL = 1 (inverted polarity):										
	1 = VIN+ < VI	N-									
0 = VIN + > VIN -											
Note 1. Inn	uts that are sel	ected and not a	vailable will be	tied to Vss. S	See the " Pin Dia	arams" section	n for available				

REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3)

- Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.
 - 2: This output is not available when OPMODE (CMxCON<10>) = 1.

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
1	ADD	ADD	Acc ⁽¹⁾	Add Accumulators	1	1	OA,OB,SA,SB
		ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD	f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD	Wso,#Slit4,Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (4)	None
		BRA	GE, Expr	Branch if greater than or equal	1	1 (4)	None
		BRA	GEU, Expr	Branch if unsigned greater than or equal	1	1 (4)	None
		BRA	GT, Expr	Branch if greater than	1	1 (4)	None
		BRA	GTU, Expr	Branch if unsigned greater than	1	1 (4)	None
		BRA	LE, Expr	Branch if less than or equal	1	1 (4)	None
		BRA	LEU, Expr	Branch if unsigned less than or equal	1	1 (4)	None
		BRA	LT,Expr	Branch if less than	1	1 (4)	None
		BRA	LTU, Expr	Branch if unsigned less than	1	1 (4)	None
		BRA	N,Expr	Branch if Negative	1	1 (4)	None
		BRA	NC, Expr	Branch if Not Carry	1	1 (4)	None
		BRA	NN, Expr	Branch if Not Negative	1	1 (4)	None
		BRA	NOV, Expr	Branch if Not Overflow	1	1 (4)	None
		BRA	NZ,Expr	Branch if Not Zero	1	1 (4)	None
		BRA	OA, Expr(1)	Branch if Accumulator A overflow	1	1 (4)	None
		BRA	OB, Expr(1)	Branch if Accumulator B overflow	1	1 (4)	None
		BRA	OV, Expr(1)	Branch if Overflow	1	1 (4)	None
		BRA	SA, Expr(1)	Branch if Accumulator A saturated	1	1 (4)	None
		BRA	SB, Expr(1)	Branch if Accumulator B saturated	1	1 (4)	None
		BRA	Expr	Branch Unconditionally	1	4	None
		BRA	Z,Expr	Branch if Zero	1	1 (4)	None
L		BRA	Wn	Computed Branch	1	4	None
7	BSET	BSET	f,#bit4	Bit Set f	1	1	None
		BSET	Ws,#bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C	Ws,Wb	Write C bit to Ws <wb></wb>	1	1	None
		BSW.Z	Ws,Wb	Write Z bit to Ws <wb></wb>	1	1	None

TABLE 28-2: INSTRUCTION SET OVERVIEW

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions (see Note 1): 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$						
Param No.	Symbol	Characteristic	Min. Typ. Max. Units Conditions						
Operating Voltage									
DC10	Vdd	Supply Voltage	3.0	_	3.6	V			
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	_	_	Vss	V			
DC17	Svdd	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.03	—	—	V/ms	0V-1V in 100 ms		

TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

Standard Operating	Standard Operating Conditions (unless otherwise stated): Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended								
Param No. Symbol Characteristics Min. Typ. Max. Units Comments							Comments		
	Cefc	External Filter Capacitor Value ⁽¹⁾	4.7	10		μF	Capacitor must have a low series resistance (< 1 Ohm)		

Note 1: Typical VCAP voltage = 1.8 volts when VDD \ge VDDMIN.

TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic	Min.	Min. Typ. ⁽¹⁾ Max. Units			Conditions		
OS50	Fplli	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8.0	MHz	ECPLL, XTPLL modes		
OS51	Fvco	On-Chip VCO System Frequency	120	—	340	MHz			
OS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	ms			
OS53	DCLK	CLKO Stability (Jitter) ⁽²⁾	-3	0.5	3	%			

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases, or communication clocks used by the application, use the following formula:

$$Effective Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Time Base or Communication Clock}}}$$

For example, if Fosc = 120 MHz and the SPIx bit rate = 10 MHz, the effective jitter is as follows:

Effective Jitter =
$$\frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

TABLE 30-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		$\begin{array}{ l l l l l l l l l l l l l l l l l l l$							
Param No. Characteristic		Min.	Тур.	Max.	Units	Conditions			
Internal FRC Accuracy @ FRC Frequency = 7.37 MHz ⁽¹⁾									
F20a	FRC	-1.5	0.5	+1.5	%	$-40^{\circ}C \le TA \le -10^{\circ}C$	VDD = 3.0-3.6V		
		-1	0.5	+1	%	$-10^{\circ}C \leq TA \leq +85^{\circ}C$	VDD = 3.0-3.6V		
F20b	FRC	-2	1	+2	%	$+85^{\circ}C \le TA \le +125^{\circ}C$	VDD = 3.0-3.6V		

Note 1: Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

TABLE 30-20: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		$\begin{array}{llllllllllllllllllllllllllllllllllll$								
Param No. Characteristic		Min.	Тур.	Max.	Units	Conditions				
LPRC @ 32.768 kHz ⁽¹⁾										
F21a	LPRC	-30		+30	%	$-40^\circ C \le T A \le -10^\circ C$	VDD = 3.0-3.6V			
		-20		+20	%	$-10^{\circ}C \le TA \le +85^{\circ}C$	VDD = 3.0-3.6V			
F21b	LPRC	-30		+30	%	$+85^{\circ}C \leq TA \leq +125^{\circ}C$	VDD = 3.0-3.6V			

Note 1: The change of LPRC frequency as VDD changes.



FIGURE 30-12: QEA/QEB INPUT CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

TABLE 30-31: QUADRATURE DECODER TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			Standard Ope (unless other Operating tem	erating Co wise state perature	nditions: 3.0V to 3.6V ed) $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended		
Param No.	Symbol	Characteristic ⁽¹⁾	Тур. ⁽²⁾	Max.	Units	Conditions	
TQ30	TQUL	Quadrature Input Low Time	6 Tcy		ns		
TQ31	ΤουΗ	Quadrature Input High Time	6 Tcy	—	ns		
TQ35	ΤουΙΝ	Quadrature Input Period	12 Tcy	—	ns		
TQ36	ΤουΡ	Quadrature Phase Period	3 Tcy	—	ns		
TQ40	TQUFL	Filter Time to Recognize Low, with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)	
TQ41	TQUFH	Filter Time to Recognize High, with Digital Filter	3 * N * Tcy		ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: N = Index Channel Digital Filter Clock Divide Select bits. Refer to "Quadrature Encoder Interface (QEI)" (DS70601) in the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip web site for the latest family reference manual sections.

33.1 Package Marking Information (Continued)



28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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