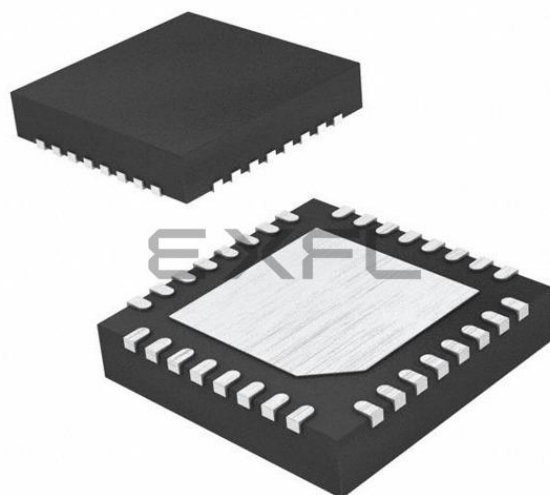




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mc502-h-mm

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X AND PIC24EP64GP/MC20X DEVICES

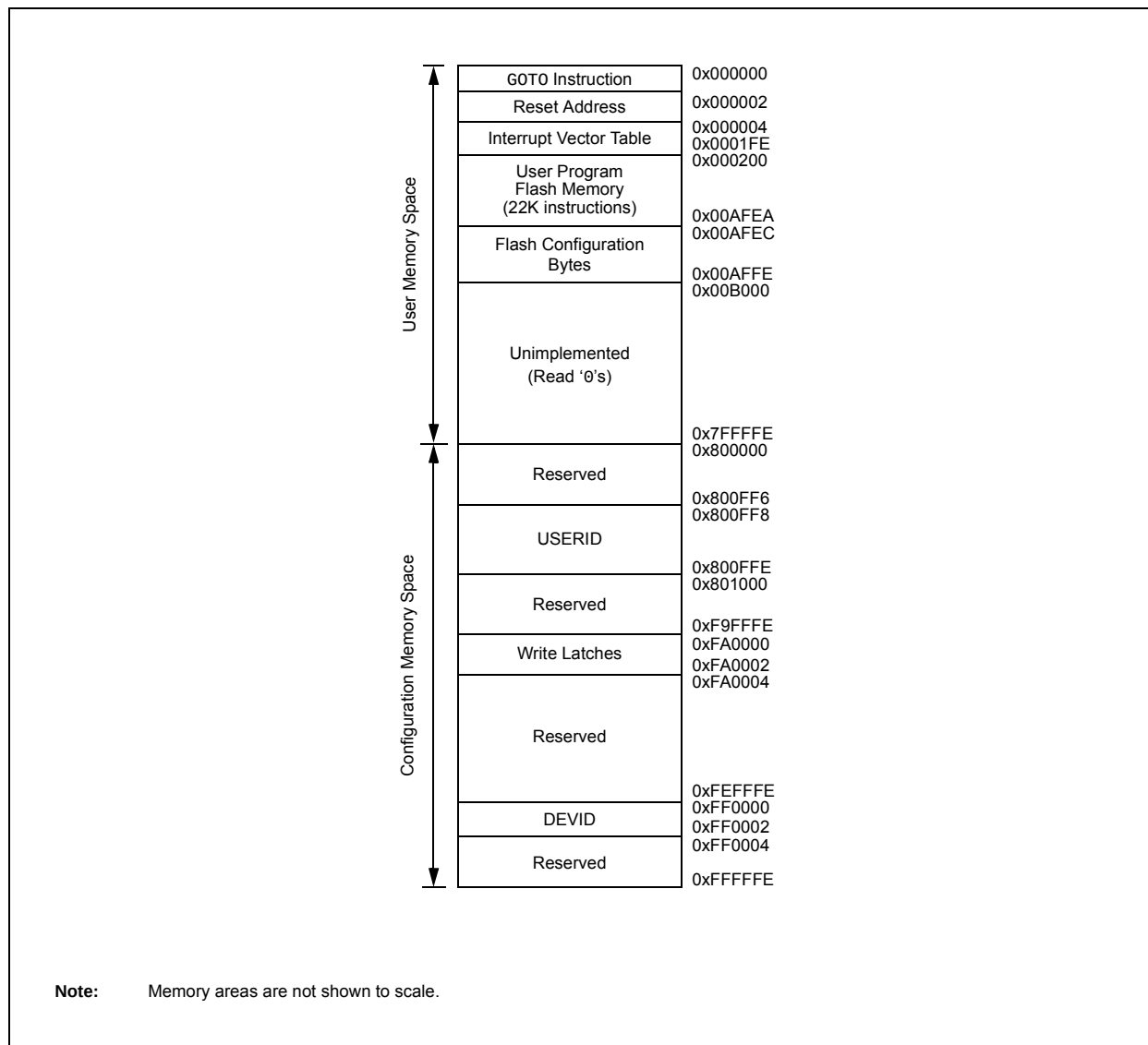


FIGURE 4-16: DATA MEMORY MAP FOR PIC24EP512GP/MC20X/50X DEVICES

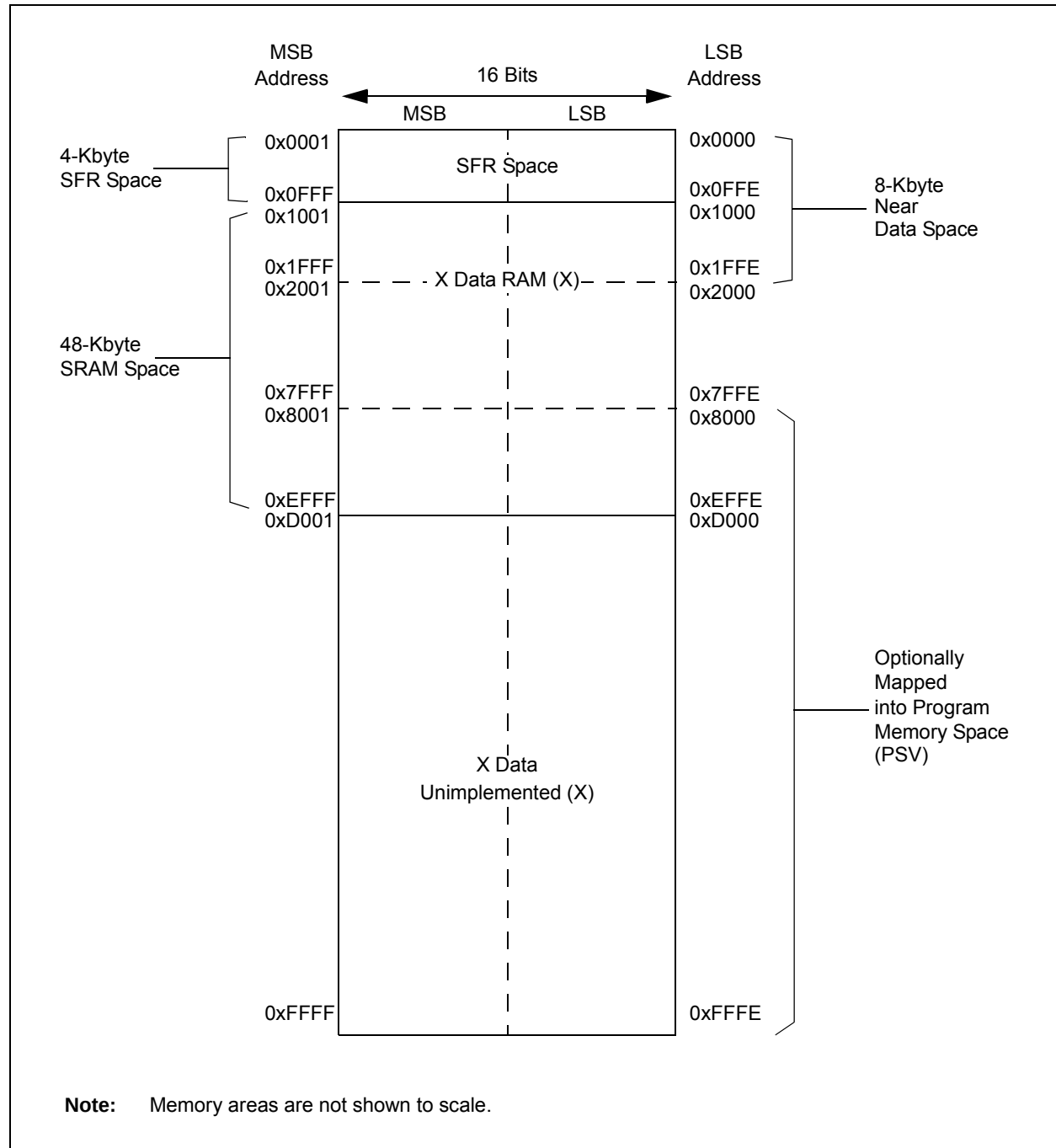


TABLE 4-9: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 4 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1CON1	0140	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC1CON2	0142	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC1BUF	0144	Input Capture 1 Buffer Register																xxxx
IC1TMR	0146	Input Capture 1 Timer																0000
IC2CON1	0148	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC2CON2	014A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC2BUF	014C	Input Capture 2 Buffer Register																xxxx
IC2TMR	014E	Input Capture 2 Timer																0000
IC3CON1	0150	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC3CON2	0152	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC3BUF	0154	Input Capture 3 Buffer Register																xxxx
IC3TMR	0156	Input Capture 3 Timer																0000
IC4CON1	0158	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC4CON2	015A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC4BUF	015C	Input Capture 4 Buffer Register																xxxx
IC4TMR	015E	Input Capture 4 Timer																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-49: PORTD REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E30	—	—	—	—	—	—	—	TRISD8	—	TRISD6	TRISD5	—	—	—	—	—	0160
PORTD	0E32	—	—	—	—	—	—	—	RD8	—	RD6	RD5	—	—	—	—	—	xxxx
LATD	0E34	—	—	—	—	—	—	—	LATD8	—	LATD6	LATD5	—	—	—	—	—	xxxx
ODCD	0E36	—	—	—	—	—	—	—	ODCD8	—	ODCD6	ODCD5	—	—	—	—	—	0000
CNEND	0E38	—	—	—	—	—	—	—	CNIED8	—	CNIED6	CNIED5	—	—	—	—	—	0000
CNPUD	0E3A	—	—	—	—	—	—	—	CNPUD8	—	CNPUD6	CNPUD5	—	—	—	—	—	0000
CNPDD	0E3C	—	—	—	—	—	—	—	CNPDD8	—	CNPDD6	CNPDD5	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-50: PORTE REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	0E40	TRISE15	TRISE14	TRISE13	TRISE12	—	—	—	—	—	—	—	—	—	—	—	—	F000
PORTE	0E42	RE15	RE14	RE13	RE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
LATE	0E44	LATE15	LATE14	LATE13	LATE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
ODCE	0E46	ODCE15	ODCE14	ODCE13	ODCE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNENE	0E48	CNIEE15	CNIEE14	CNIEE13	CNIEE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPUE	0E4A	CNPUE15	CNPUE14	CNPUE13	CNPUE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPDE	0E4C	CNPDE15	CNPDE14	CNPDE13	CNPDE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
ANSELE	0E4E	ANSE15	ANSE14	ANSE13	ANSE12	—	—	—	—	—	—	—	—	—	—	—	—	F000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-51: PORTF REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISF1	TRISF0	0003
PORTF	0E52	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RF1	RF0	xxxx
LATF	0E54	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATF1	LATF0	xxxx
ODCF	0E56	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCF1	ODCF0	0000
CNENF	0E58	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNIEF1	CNIEF0	0000
CNPUF	0E5A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUF1	CNPUF0	0000
CNPDF	0E5C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPDF1	CNPDF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

- Four DMA channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode

- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU interrupt after half or full block transfer complete
- Byte or word transfers
- Fixed priority channel arbitration
- Manual (software) or automatic (peripheral DMA requests) transfer initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer is complete)
- DMA request for each channel can be selected from any supported interrupt source
- Debug support features

The peripherals that can utilize DMA are listed in Table 8-1.

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
INT0 – External Interrupt 0	00000000	—	—
IC1 – Input Capture 1	00000001	0x0144 (IC1BUF)	—
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	—
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	—
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	—
OC1 – Output Compare 1	00000010	—	0x0906 (OC1R) 0x0904 (OC1RS)
OC2 – Output Compare 2	00000110	—	0x0910 (OC2R) 0x090E (OC2RS)
OC3 – Output Compare 3	00011001	—	0x091A (OC3R) 0x0918 (OC3RS)
OC4 – Output Compare 4	00011010	—	0x0924 (OC4R) 0x0922 (OC4RS)
TMR2 – Timer2	00000111	—	—
TMR3 – Timer3	00001000	—	—
TMR4 – Timer4	00011011	—	—
TMR5 – Timer5	00011100	—	—
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	—
UART1TX – UART1 Transmitter	00001100	—	0x0224 (U1TXREG)
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	—
UART2TX – UART2 Transmitter	00011111	—	0x0234 (U2TXREG)
ECAN1 – RX Data Ready	00100010	0x0440 (C1RXD)	—
ECAN1 – TX Data Request	01000110	—	0x0442 (C1TXD)
ADC1 – ADC1 Convert Done	00001101	0x0300 (ADC1BUF0)	—

REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/S-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE ⁽¹⁾	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0
bit 7							bit 0

Legend:	S = Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

- bit 15 **FORCE:** Force DMA Transfer bit⁽¹⁾
 1 = Forces a single DMA transfer (Manual mode)
 0 = Automatic DMA transfer initiation by DMA request
- bit 14-8 **Unimplemented:** Read as '0'
- bit 7-0 **IRQSEL<7:0>:** DMA Peripheral IRQ Number Select bits
 01000110 = ECAN1 – TX Data Request⁽²⁾
 00100110 = IC4 – Input Capture 4
 00100101 = IC3 – Input Capture 3
 00100010 = ECAN1 – RX Data Ready⁽²⁾
 00100001 = SPI2 Transfer Done
 00011111 = UART2TX – UART2 Transmitter
 00011110 = UART2RX – UART2 Receiver
 00011100 = TMR5 – Timer5
 00011011 = TMR4 – Timer4
 00011010 = OC4 – Output Compare 4
 00011001 = OC3 – Output Compare 3
 00001101 = ADC1 – ADC1 Convert done
 00001100 = UART1TX – UART1 Transmitter
 00001011 = UART1RX – UART1 Receiver
 00001010 = SPI1 – Transfer Done
 00001000 = TMR3 – Timer3
 00000111 = TMR2 – Timer2
 00000110 = OC2 – Output Compare 2
 00000101 = IC2 – Input Capture 2
 00000010 = OC1 – Output Compare 1
 00000001 = IC1 – Input Capture 1
 00000000 = INT0 – External Interrupt 0

- Note 1:** The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).
- 2:** This selection is available in dsPIC33EPXXXGP/MC50X devices only.

REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'bit 7-0 **DSADR<23:16>:** Most Recent DMA Address Accessed by DMA bits**REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER**

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<15:8>							
bit 15				bit 8			

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **DSADR<15:0>:** Most Recent DMA Address Accessed by DMA bits

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES (CONTINUED)

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
010 1000	I/O	RP40	101 0101	—	—
010 1001	I/O	RP41	101 0110	—	—
010 1010	I/O	RP42	101 0111	—	—
010 1011	I/O	RP43	101 1000	—	—
010 1100	I	RPI44	101 1001	—	—
101 1010	—	—	110 1101	—	—
101 1011	—	—	110 1110	—	—
101 1100	—	—	110 1111	—	—
101 1101	—	—	111 0000	—	—
101 1110	I	RPI94	111 0001	—	—
101 1111	I	RPI95	111 0010	—	—
110 0000	I	RPI96	111 0011	—	—
110 0001	I/O	RP97	111 0100	—	—
110 0010	—	—	111 0101	—	—
110 0011	—	—	111 0110	I/O	RP118
110 0100	—	—	111 0111	I	RPI119
110 0101	—	—	111 1000	I/O	RP120
110 0110	—	—	111 1001	I	RPI121
110 0111	—	—	111 1010	—	—
110 1000	—	—	111 1011	—	—
110 1001	—	—	111 1100	—	—
110 1010	—	—	111 1101	—	—
110 1011	—	—	111 1110	—	—
110 1100	—	—	111 1111	—	—

Legend: Shaded rows indicate PPS Input register values that are unimplemented.

Note 1: See Section 11.4.4.1 “Virtual Connections” for more information on selecting this pin assignment.

2: These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

REGISTER 11-9: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	HOME1R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INDX1R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **HOME1R<6:0>:** Assign QE11 HOME1 (HOME1) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **INDX1R<6:0>:** Assign QE11 INDEX1 (INDX1) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 17-2: QE1IOC: QE1 I/O CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QCAPEN	FLTREN	QFDIV2	QFDIV1	QFDIV0	OUTFNC1	OUTFNC0	SWPAB
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x
HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **QCAPEN:** QE1 Position Counter Input Capture Enable bit
1 = Index match event triggers a position capture event
0 = Index match event does not trigger a position capture event
- bit 14 **FLTREN:** QEAx/QEBx/INDXx/HOMEx Digital Filter Enable bit
1 = Input pin digital filter is enabled
0 = Input pin digital filter is disabled (bypassed)
- bit 13-11 **QFDIV<2:0>:** QEAx/QEBx/INDXx/HOMEx Digital Input Filter Clock Divide Select bits
111 = 1:128 clock divide
110 = 1:64 clock divide
101 = 1:32 clock divide
100 = 1:16 clock divide
011 = 1:8 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide
- bit 10-9 **OUTFNC<1:0>:** QE1 Module Output Function Mode Select bits
11 = The CTNCMPx pin goes high when $QE1LEC \geq POS1CNT \geq QE1GEC$
10 = The CTNCMPx pin goes high when $POS1CNT \leq QE1LEC$
01 = The CTNCMPx pin goes high when $POS1CNT \geq QE1GEC$
00 = Output is disabled
- bit 8 **SWPAB:** Swap QEA and QEB Inputs bit
1 = QEAx and QEBx are swapped prior to quadrature decoder logic
0 = QEAx and QEBx are not swapped
- bit 7 **HOMPOL:** HOMEx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted
- bit 6 **IDXPOL:** INDXx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted
- bit 5 **QEBPOL:** QEBx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted
- bit 4 **QEAPOL:** QEAx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted
- bit 3 **HOME:** Status of HOMEx Input Pin After Polarity Control
1 = Pin is at logic '1'
0 = Pin is at logic '0'

REGISTER 17-7: VEL1CNT: VELOCITY COUNTER 1 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VELCNT<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VELCNT<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **VELCNT<15:0>**: Velocity Counter bits**REGISTER 17-8: INDX1CNTH: INDEX COUNTER 1 HIGH WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXCNT<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXCNT<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **INDXCNT<31:16>**: High Word Used to Form 32-Bit Index Counter Register (INDX1CNT) bits**REGISTER 17-9: INDX1CNTL: INDEX COUNTER 1 LOW WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXCNT<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXCNT<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **INDXCNT<15:0>**: Low Word Used to Form 32-Bit Index Counter Register (INDX1CNT) bits

REGISTER 17-13: QE11LECH: QE11 LESS THAN OR EQUAL COMPARE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **QEILEC<31:16>**: High Word Used to Form 32-Bit Less Than or Equal Compare Register (QE11LEC) bits**REGISTER 17-14: QE11LECL: QE11 LESS THAN OR EQUAL COMPARE LOW WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **QEILEC<15:0>**: Low Word Used to Form 32-Bit Less Than or Equal Compare Register (QE11LEC) bits

18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
 - a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on $\overline{SSx}$.
 - b) If FRMPOL = 0, use a pull-up resistor on $\overline{SSx}$.

Note: This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode, (i.e., not using $\overline{SSx}$ from a master):
 - a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on $\overline{SSx}$.
 - b) If CKP = 0, always place a pull-down resistor on $\overline{SSx}$.

Note: This will insure that during power-up and initialization the master/slave will not lose Sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the $\overline{SSx}$ pin, which indicates the start of a data frame.

Note: Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in **Section 30.0 "Electrical Characteristics"** for details.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPIx data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

18.2.1 KEY RESOURCES

- **"Serial Peripheral Interface (SPI)"** (DS70569) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

18.3 SPIx Control Registers

REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
SPIEN	—	SPISIDL	—	—	SPIBEC<2:0>		
bit 15							bit 8

R/W-0	R/C-0, HS	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC	R-0, HS, HC
SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	HC = Hardware Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **SPIEN:** SPIx Enable bit
1 = Enables the module and configures SCKx, SDOx, SDIx and $\overline{SSx}$ as serial port pins
0 = Disables the module
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SPISIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues the module operation when device enters Idle mode
0 = Continues the module operation in Idle mode
- bit 12-11 **Unimplemented:** Read as '0'
- bit 10-8 **SPIBEC<2:0>:** SPIx Buffer Element Count bits (valid in Enhanced Buffer mode)
Master mode:
Number of SPIx transfers that are pending.
Slave mode:
Number of SPIx transfers that are unread.
- bit 7 **SRMPT:** SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode)
1 = SPIx Shift register is empty and Ready-To-Send or receive the data
0 = SPIx Shift register is not empty
- bit 6 **SPIROV:** SPIx Receive Overflow Flag bit
1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register
0 = No overflow has occurred
- bit 5 **SRXMPT:** SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode)
1 = RX FIFO is empty
0 = RX FIFO is not empty
- bit 4-2 **SISEL<2:0>:** SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)
111 = Interrupt when the SPIx transmit buffer is full (SPITBF bit is set)
110 = Interrupt when last bit is shifted into SPIxSR and as a result, the TX FIFO is empty
101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete
100 = Interrupt when one data is shifted into the SPIxSR and as a result, the TX FIFO has one open memory location
011 = Interrupt when the SPIx receive buffer is full (SPIRBF bit is set)
010 = Interrupt when the SPIx receive buffer is 3/4 or more full
001 = Interrupt when data is available in the receive buffer (SRMPT bit is set)
000 = Interrupt when the last data in the receive buffer is read and as a result, the buffer is empty (SRXMPT bit is set)

REGISTER 24-2: PTGCON: PTG CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **PTGCLK<2:0>:** Select PTG Module Clock Source bits

111 = Reserved
110 = Reserved
101 = PTG module clock source will be T3CLK
100 = PTG module clock source will be T2CLK
011 = PTG module clock source will be T1CLK
010 = PTG module clock source will be TAD
001 = PTG module clock source will be Fosc
000 = PTG module clock source will be FP

bit 12-8 **PTGDIV<4:0>:** PTG Module Clock Prescaler (divider) bits

11111 = Divide-by-32
11110 = Divide-by-31
•
•
•
00001 = Divide-by-2
00000 = Divide-by-1

bit 7-4 **PTGPWD<3:0>:** PTG Trigger Output Pulse-Width bits

1111 = All trigger outputs are 16 PTG clock cycles wide
1110 = All trigger outputs are 15 PTG clock cycles wide
•
•
•
0001 = All trigger outputs are 2 PTG clock cycles wide
0000 = All trigger outputs are 1 PTG clock cycle wide

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **PTGWDT<2:0>:** Select PTG Watchdog Timer Time-out Count Value bits

111 = Watchdog Timer will time-out after 512 PTG clocks
110 = Watchdog Timer will time-out after 256 PTG clocks
101 = Watchdog Timer will time-out after 128 PTG clocks
100 = Watchdog Timer will time-out after 64 PTG clocks
011 = Watchdog Timer will time-out after 32 PTG clocks
010 = Watchdog Timer will time-out after 16 PTG clocks
001 = Watchdog Timer will time-out after 8 PTG clocks
000 = Watchdog Timer is disabled

REGISTER 24-4: PTGT0LIM: PTG TIMER0 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PTGT0LIM<15:0>**: PTG Timer0 Limit Register bits
General Purpose Timer0 Limit register (effective only with a PTGT0 Step command).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-5: PTGT1LIM: PTG TIMER1 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PTGT1LIM<15:0>**: PTG Timer1 Limit Register bits
General Purpose Timer1 Limit register (effective only with a PTGT1 Step command).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

29.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

29.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 30-24: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Typ.	Max.	Units	Conditions
TB10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	—	—	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	—	—	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	—	—	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Typ.	Max.	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous, with prescaler	2 Tcy + 40	—	—	ns	N = prescale value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

ECAN Module	
Control Registers	290
Modes of Operation	289
Overview	287
Resources	289
Electrical Characteristics	401
AC	413, 471
Enhanced CAN (ECAN) Module	287
Equations	
Device Operating Frequency	154
FPLLO Calculation	154
FVCO Calculation	154
Errata	23
F	
Filter Capacitor (CEFC) Specifications	403
Flash Program Memory	119
Control Registers	120
Programming Operations	120
Resources	120
RTSP Operation	120
Table Instructions	119
Flexible Configuration	379
G	
Guidelines for Getting Started	29
Application Examples	32
Basic Connection Requirements	29
CPU Logic Filter Capacitor Connection (VCAP)	30
Decoupling Capacitors	29
External Oscillator Pins	31
ICSP Pins	31
Master Clear (MCLR) Pin	30
Oscillator Value Conditions on Start-up	32
Unused I/Os	32
H	
High-Speed PWM	225
Control Registers	230
Faults	225
Resources	229
High-Temperature Electrical Characteristics	467
Absolute Maximum Ratings	467
I	
I/O Ports	173
Helpful Tips	181
Parallel I/O (PIO)	173
Resources	182
Write/Read Timing	174
In-Circuit Debugger	386
In-Circuit Emulation	379
In-Circuit Serial Programming (ICSP)	379, 386
Input Capture	213
Control Registers	215
Resources	214
Input Change Notification (ICN)	174
Instruction Addressing Modes	112
File Register Instructions	112
Fundamental Modes Supported	112
MAC Instructions	113
MCU Instructions	112
Move and Accumulator Instructions	113
Other Instructions	113

Instruction Set	
Overview	390
Summary	387
Symbols Used in Opcode Descriptions	388
Inter-Integrated Circuit (I ² C)	273
Control Registers	276
Resources	275
Internal RC Oscillator	
Use with WDT	385
Internet Address	524
Interrupt Controller	
Control and Status Registers	131
INTCON1	131
INTCON2	131
INTCON3	131
INTCON4	131
INTTREG	131
Interrupt Vector Details	129
Interrupt Vector Table (IVT)	127
Reset Sequence	127
Resources	131
J	
JTAG Boundary Scan Interface	379
JTAG Interface	386
M	
Memory Maps	
Extended Data Space	109
Memory Organization	45
Resources	62
Microchip Internet Web Site	524
Modulo Addressing	114
Applicability	115
Operation Example	114
Start and End Address	114
W Address Register Selection	114
MPLAB Assembler, Linker, Librarian	398
MPLAB ICD 3 In-Circuit Debugger	399
MPLAB PM3 Device Programmer	399
MPLAB REAL ICE In-Circuit Emulator System	399
MPLAB X Integrated Development	
Environment Software	397
MPLAB X SIM Software Simulator	399
MPLIB Object Librarian	398
MPLINK Object Linker	398
O	
Op Amp	
Application Considerations	358
Configuration A	358
Configuration B	359
Op Amp/Comparator	355
Control Registers	360
Resources	359
Open-Drain Configuration	174
Oscillator	
Control Registers	156
Resources	155
Output Compare	219
Control Registers	221
Resources	220

