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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	·
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mc502t-e-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 3 MHz < F_{IN} < 5.5 MHz to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between Vss and unused pins, and drive the output to logic low.

2.9 Application Examples

- · Induction heating
- Uninterruptable Power Supplies (UPS)
- DC/AC inverters
- · Compressor motor control
- · Washing machine 3-phase motor control
- BLDC motor control
- · Automotive HVAC, cooling fans, fuel pumps
- Stepper motor control
- · Audio and fluid sensor monitoring
- · Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- Consumer audio
- Industrial and building control (security systems and access control)
- · Barcode reading
- Networking: LAN switches, gateways
- Data storage device management
- · Smart cards and smart card readers

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION



4.5.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions. which apply to dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and the DSP accumulator class of instructions, which apply to the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.5.4 MAC INSTRUCTIONS (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X DEVICES ONLY)

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY. N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The Two-Source Operand Prefetch registers must be members of the set: {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the ${\tt MAC}$ class of instructions:

- · Register Indirect
- Register Indirect Post-Modified by 2
- · Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.5.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

				(,			
R/SO-0 ⁽¹	⁾ R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	NVMSIDL ⁽²⁾			—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
	—	—		NVMOP3 ^(3,4)	NVMOP2 ^(3,4)	NVMOP1 ^(3,4)	NVMOP0 ^(3,4)
bit 7							bit 0
						_	
Legend:		SO = Settab	le Only bit				
R = Reada	ble bit	W = Writable	e bit	U = Unimplem	ented bit, read	as '0'	
-n = Value	at POR	'1' = Bit is se	t	'0' = Bit is clea	ired	x = Bit is unkn	iown
bit 15	WR: Write Co 1 = Initiates a cleared by 0 = Program	ntrol bit ⁽¹⁾ a Flash memo y hardware o or erase oper	ory program or nce the operati ation is comple	erase operation on is complete ate and inactive	on; the operatio	n is self-timed	and the bit is
bit 14	WREN: Write 1 = Enables F 0 = Inhibits Fl	Enable bit ⁽¹⁾ ⁻ lash program ash program/	n/erase operati ⁄erase operatio	ons			
bit 13	WRERR: Writ 1 = An improp on any se 0 = The progr	e Sequence E per program of t attempt of th ram or erase	Error Flag bit ⁽¹⁾ rerase sequence e WR bit) operation comp	ce attempt or ter	mination has oc	curred (bit is se	t automatically
bit 12	NVMSIDL: N\ 1 = Flash volt 0 = Flash volt	/M Stop in Idl age regulator age regulator	e Control bit ⁽²⁾ goes into Star is active durin	ndby mode duri g Idle mode	ng Idle mode		
bit 11-4	Unimplement	ted: Read as	'0'	-			
bit 11-4 Unimplemented: Read as '0' bit 3-0 NVMOP<3:0>: NVM Operation Select bits ^(1,3,4) 1111 = Reserved 1100 = Reserved 1000 = Reserved 1011 = Reserved 1010 = Reserved 1010 = Reserved 0011 = Memory page erase operation 0010 = Reserved 0011 = Memory double-word program operation ⁽⁵⁾ 0000 = Reserved							
Note 1: 2: 3: 4: 5:	These bits can only If this bit is set, the (TVREG) before Fla All other combination Execution of the PV Two adjacent word	/ be reset on a re will be mini sh memory be ons of NVMO wrsav instruc s on a 4-word	a POR. mal power sav ecomes operat P<3:0> are uni tion is ignored I boundary are	rings (IIDLE) and ional. implemented. while any of the programmed d	d upon exiting lo e NVM operatio uring execution	the mode, there ns are in progra	is a delay ess. on.

REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

9.1 CPU Clocking System

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X family of devices provides six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase Locked Loop (PLL)
- · FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- · Low-Power RC (LPRC) Oscillator

Instruction execution speed or device operating frequency, FCY, is given by Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

FCY = Fosc/2

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (FIN) and output frequency (FPLLO). In clock modes S1 and S3, when the PLL output is selected, FOSC = FPLLO.

Equation 9-3 provides the relationship between input frequency (FIN) and VCO frequency (FVCO).



EQUATION 9-2: FPLLO CALCULATION

$$FPLLO = FIN \times \left(\frac{M}{N1 \times N2}\right) = FIN \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)}\right)$$

Where:

N1 = PLLPRE + 2 $N2 = 2 \times (PLLPOST + 1)$

M = PLLDIV + 2

EQUATION 9-3: Fvco CALCULATION

$$Fvco = FIN \times \left(\frac{M}{N1}\right) = FIN \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)}\right)$$

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FIGURE 9-2: PLL BLOCK DIAGRAM

11.0 I/O PORTS

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "I/O Ports" (DS70598) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

Many of the device pins are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

Generally, a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through," in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have eight registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Latch register (LATx) read the latch. Writes to the Latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device is disabled. This means the corresponding LATx and TRISx registers and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.





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U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP39F	२<5:0>		
bit 15	•						bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP38F	२<5:0>		
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplem	ented bit, read	d as '0'	
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown				
bit 15-14	Unimpleme	nted: Read as '	0'				
bit 13-8	RP39R<5:0>	: Peripheral Ou	Itput Function	n is Assigned to I	RP39 Output I	⊃in bits	

REGISTER 11-20: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

	(see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP38R<5:0>: Peripheral Output Function is Assigned to RP38 Output Pin bits
	(see Table 11-3 for peripheral function numbers)

REGISTER 11-21: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
—	_		RP41R<5:0>							
bit 15							bit 8			

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
_			RP40R<5:0>						
bit 7							bit 0		

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-14 Unimplemented: Read as '0'

- bit 13-8 **RP41R<5:0>:** Peripheral Output Function is Assigned to RP41 Output Pin bits (see Table 11-3 for peripheral function numbers)
- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 **RP40R<5:0>:** Peripheral Output Function is Assigned to RP40 Output Pin bits (see Table 11-3 for peripheral function numbers)

14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend: HC = Hardware Clearable bit		HS = Hardware Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture Stop in Idle Control bit
	1 = Input capture will Halt in CPU Idle mode
	0 = Input capture will continue to operate in CPU Idle mode
bit 12-10	ICTSEL<2:0>: Input Capture Timer Select bits
	111 = Peripheral clock (FP) is the clock source of the ICx
	110 = Reserved
	101 = Reserved
	100 - 11 CLR is the clock source of the ICx (only the synchronous clock is supported) 011 = T5CLK is the clock source of the ICx
	010 = T4CLK is the clock source of the ICx
	001 = T2CLK is the clock source of the ICx
	000 = T3CLK is the clock source of the ICx
bit 9-7	Unimplemented: Read as '0'
bit 6-5	ICI<1:0>: Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	01 = Interrupt on every second capture event
hit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
Dit 4	1 = Input capture buffer overflow occurred
	0 = No input capture buffer overflow occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	1 = Input capture buffer is not empty, at least one more capture value can be read
	0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture Mode Select bits
	111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
	110 = Unused (module is disabled)
	101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
	100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
	011 = Capture mode, every falling edge (Simple Capture mode)
	001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
	000 = Input capture module is turned off

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U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimplem	ented bit, read	as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is clea	ired	x = Bit is unkr	nown
			- ¹				
DIT 15-12	Unimpleme	nted: Read as 1).				
DIT 11-8	BLANKSEL	<3:0>: PVVMX S	tate Blank Sol	LICE Select bits	and/on Fault in	aut airmala /if a	
	BCH and BC	I state blank sig	RCONx regist	ne current-iimit er)	and/or Fault inp	but signals (il e	nabled via the
	1001 = Res e	erved	Sective				
	•						
	•						
	•						
	0100 = Res e	erved					
	0011 = PWN	A3H selected as	state blank s	ource			
	0010 = PWN	M2H selected as	state blank s	ource			
	0000 = No s	tate blanking					
bit 7-6	Unimpleme	nted: Read as '	D'				
bit 5-2	CHOPSEL<	3:0>: PWMx Ch	op Clock Sou	rce Select bits			
	The selected	l signal will enat erved	ble and disable	e (CHOP) the se	elected PWMx of	outputs.	
	•						
	•						
	•						
	0100 = Res e	erved					
	0011 = PWN	A3H selected as	CHOP clock	source			
	0010 = PWN	M2H selected as		source			
	0000 = Cho	p clock generato	or selected as	CHOP clock so	urce		
bit 1	CHOPHEN:	PWMxH Output	Chopping En	able bit			
	1 = PWMxH	chopping function	on is enabled				
	0 = PWMxH	chopping function	on is disabled				
bit 0	CHOPLEN:	PWMxL Output	Chopping Ena	able bit			
	1 = PWMxL	chopping function	on is enabled				
	0 = PWMxL	chopping function	on is disabled				

REGISTER 16-18: AUXCONx: PWMx AUXILIARY CONTROL REGISTER

NOTES:

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-19: CxFMSKSEL2: ECANx FILTER 15-8 MASK SELECTION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F15M	SK<1:0>	F14MS	K<1:0>	F13MS	SK<1:0>	F12MS	K<1:0>	
bit 15		·					bit 8	
	D 444 0	D 444 0	DAALO	DAMA	D 4 4 4	D 444 0	DAVO	
R/W-0	R/W-0	R/W-U	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F11M	F11MSK<1:0>		F10MSK<1:0>		K<1:0>	F8MS	<<1:0>	
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'		
-n = Value at POR '1' = Bit is set				'0' = Bit is cleared x = Bit is unknown				
bit 15-14	F15MSK<1: 11 = Reserv 10 = Accept 01 = Accept 00 = Accept	0>: Mask Sourc ed ance Mask 2 reg ance Mask 1 reg ance Mask 0 reg	e for Filter 15 gisters contain gisters contain gisters contain	mask mask mask mask				
bit 13-12	F14MSK<1:	0>: Mask Sourc	e for Filter 14	bits (same valu	ies as bits<15:	14>)		
bit 11-10	F13MSK<1:	0>: Mask Sourc	e for Filter 13	bits (same valu	ies as bits<15:	14>)		
bit 9-8	F12MSK<1:	0>: Mask Sourc	e for Filter 12	bits (same valu	ies as bits<15:	14>)		
bit 7-6	F11MSK<1:	0>: Mask Sourc	e for Filter 11 I	oits (same valu	es as bits<15:	14>)		
bit 5-4	F10MSK<1:	0>: Mask Sourc	e for Filter 10	bits (same valu	ies as bits<15:	14>)		
bit 3-2	F9MSK<1:0	>: Mask Source	for Filter 9 bit	s (same values	as bits<15:14	>)		

21.5 ECAN Message Buffers

ECAN Message Buffers are part of RAM memory. They are not ECAN Special Function Registers. The user application must directly write into the RAM area that is configured for ECAN Message Buffers. The location and size of the buffer area is defined by the user application.

BUFFER 21-1: ECAN™ MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
		_	SID10	SID9	SID8	SID7	SID6	
bit 15							bit 8	
r								
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
SID5	SID4	SID3	SID2	SID1	SID0	SRR	IDE	
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'					
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unki	nown	
bit 15-13	Unimplemen	ted: Read as '	0'					
bit 12-2	SID<10:0>: S	Standard Identif	ier bits					
bit 1	SRR: Substitu	ute Remote Re	quest bit					
	When IDE = 0	<u>):</u>						
	1 = Message	will request rer	mote transmis	ssion				
	0 = Normal m	lessage						
	When IDE = 1	<u>1:</u>						
	The SRR bit r	must be set to '	1'.					
bit 0	IDE: Extende	d Identifier bit						
	1 = Message	will transmit Ex	ktended Ident	ifier				
	0 = Message	will transmit St	andard Identi	fier				

BUFFER 21-2: ECAN™ MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	
—	—	—		EID17	EID16	EID15	EID14	
bit 15 bit								
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
EID13	EID12	EID11	EID10	EID9	EID8	EID7	EID6	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable I	bit	U = Unimplemented bit, read as '0'				
-n = Value at P	OR	'1' = Bit is set	et '0' = Bit is cleared x = Bit is unknown			iown		

bit 15-12 Unimplemented: Read as '0'

bit 11-0 EID<17:6>: Extended Identifier bits

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	_	—	—		ADDMAEN
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	DMABL2	DMABL1	DMABL0
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimpler					mented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	'0' = Bit is cleared		nown
L							
bit 15-9	Unimplemen	ted: Read as 'o)'				
bit 8	ADDMAEN: /	ADC1 DMA Ena	able bit				
	1 = Conversio	on results are st	ored in the Al	DC1BUF0 regi	ster for transfer	to RAM using	DMA
	0 = Conversio	on results are st	ored in ADC1	BUF0 through	ADC1BUFF reg	gisters; DMA w	vill not be used
bit 7-3	Unimplemen	ted: Read as '0)'				
bit 2-0	DMABL<2:0>	Selects Number Selects Number	per of DMA Bu	uffer Locations	per Analog Inp	ut bits	
	111 = Allocat	es 128 words o	f buffer to eac	h analog input	t		
	110 = Allocat	es 64 words of	buffer to each	analog input			
	101 = Allocat	es 32 words of	buffer to each	analog input			
	100 = Allocat	es 16 words of	buffer to each	analog input			
		es 8 words of b	uffer to each a	analog input			
		es 2 words of h	uffer to each :	analog input			
	000 = Allocat	es 1 word of bu	ffer to each a	nalog input			

REGISTER 23-4: AD1CON4: ADC1 CONTROL REGISTER 4

REGISTER 23-5: AD1CHS123: ADC1 INPUT CHANNEL 1, 2, 3 SELECT REGISTER (CONTINUED)

bit 0

CH123SA: Channel 1, 2, 3 Positive Input Select for Sample MUXA bit In 12-bit mode (AD21B = 1), CH123SA is Unimplemented and is Read as '0':

Value	ADC Channel						
value	CH1	CH2	CH3				
1 (2)	OA1/AN3	OA2/AN0	OA3/AN6				
0 (1,2)	OA2/AN0	AN1	AN2				

Note 1: AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)

- PTGITM<1:0>: PTG Input Trigger Command Operating Mode bits⁽¹⁾
 - 11 = Single level detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
 - 10 = Single level detect with Step delay executed on exit of command
 - 01 = Continuous edge detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
 - 00 = Continuous edge detect with Step delay executed on exit of command
- Note 1: These bits apply to the PTGWHI and PTGWLO commands only.

bit 1-0

- **2:** This bit is only used with the PTGCTRL step command software trigger option.
- **3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			PTGA	DJ<15:8>				
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			PTGA	DJ<7:0>				
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	eared x = Bit is unknown			

bit 15-0 **PTGADJ<15:0>:** PTG Adjust Register bits This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGADD command.

REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	PTGL0<15:8>									
bit 15							bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	PTGL0<7:0>									
bit 7							bit 0			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 PTGL0<15:0>: PTG Literal 0 Register bits

This register holds the 16-bit value to be written to the AD1CHS0 register with the ${\tt PTGCTRL}$ Step command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

AC CHARACTERISTICS			Standard Oper (unless otherw Operating temp	ating Co vise stat perature	onditions: 3.0V ed) -40°C ≤ TA ≤ + -40°C ≤ TA ≤ +	to 3.6V -85°C foi -125°C fo	r Industrial pr Extended	
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Тур.	Max.	Units	Conditions
ТВ10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or (TcY + 20)/N		_	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N		_	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from Clock Edge Increment	External TxCK to Timer	0.75 Tcy + 40		1.75 Tcy + 40	ns	

TABLE 30-24:	TIMER2 AND TI	MER4 (TYPE B TIM	ER) EXTERNAL CLOC	K TIMING REQUIREMENTS
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Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				$\begin{array}{ll} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Тур.	Max.	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous, with prescaler	2 Tcy + 40	—	_	ns	N = prescale value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.



FIGURE 30-28: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

NOTES:

31.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40° C to $+150^{\circ}$ C are identical to those shown in **Section 30.0** "**Electrical Characteristics**" for operation between -40° C to $+125^{\circ}$ C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in **Section 30.0 "Electrical Characteristics"** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias ⁽²⁾	40°C to +150°C
Storage temperature	65°C to +160°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to Vss ⁽³⁾	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD < 3.0V ⁽³⁾	-0.3V to 3.6V
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 3.0V^{(3)}$	-0.3V to 5.5V
Maximum current out of Vss pin	60 mA
Maximum current into VDD pin ⁽⁴⁾	60 mA
Maximum junction temperature	+155°C
Maximum current sourced/sunk by any 4x I/O pin	
Maximum current sourced/sunk by any 8x I/O pin	15 mA
Maximum current sunk by all ports combined	
Maximum current sourced by all ports combined ⁽⁴⁾	70 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
 - 2: AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time from +125°C to +150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.
 - 3: Refer to the "Pin Diagrams" section for 5V tolerant pins.
 - 4: Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

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