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#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
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Pin Name <sup>(4)</sup>	Pin Type	Buffer Type	PPS	Description
C1IN1-	Ι	Analog	No	Op Amp/Comparator 1 Negative Input 1.
C1IN2-	I	Analog	No	Comparator 1 Negative Input 2.
C1IN1+	I	Analog	No	Op Amp/Comparator 1 Positive Input 1.
OA1OUT	0	Analog	No	Op Amp 1 output.
C10UT	0		Yes	Comparator 1 output.
C2IN1-	Ι	Analog	No	Op Amp/Comparator 2 Negative Input 1.
C2IN2-	I.	Analog	No	Comparator 2 Negative Input 2.
C2IN1+	I.	Analog	No	Op Amp/Comparator 2 Positive Input 1.
OA2OUT	0	Analog	No	Op Amp 2 output.
C2OUT	0	—	Yes	Comparator 2 output.
C3IN1-	I	Analog	No	Op Amp/Comparator 3 Negative Input 1.
C3IN2-	I	Analog	No	Comparator 3 Negative Input 2.
C3IN1+	I	Analog	No	Op Amp/Comparator 3 Positive Input 1.
OA3OUT	0	Analog	No	Op Amp 3 output.
C3OUT	0		Yes	Comparator 3 output.
C4IN1-	I	Analog	No	Comparator 4 Negative Input 1.
C4IN1+	I	Analog	No	Comparator 4 Positive Input 1.
C4OUT	0	—	Yes	Comparator 4 output.
CVREF10	0	Analog	No	Op amp/comparator voltage reference output.
CVREF20	0	Analog	No	Op amp/comparator voltage reference divided by 2 output.
PGED1	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 1.
PGEC1	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 1.
PGED2	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 2.
PGEC2		SI	No	Clock input pin for Programming/Debugging Communication Channel 2.
PGED3	1/0	SI	NO	Data I/O pin for Programming/Debugging Communication Channel 3.
PGEC3	1	51	NO	Clock input pin for Programming/Debugging Communication Channel 3.
MCLR	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	Р	Р	No	Positive supply for analog modules. This pin must be connected at all times.
AVss	Р	Р	No	Ground reference for analog modules. This pin must be connected at all times.
Vdd	Р		No	Positive supply for peripheral logic and I/O pins.
VCAP	Р		No	CPU logic filter capacitor connection.
Vss	Р		No	Ground reference for logic and I/O pins.
VREF+	Ι	Analog	No	Analog voltage reference (high) input.
VREF-	Ι	Analog	No	Analog voltage reference (low) input.
Legend: CMOS = C	MOS co	ompatible	e input	or output Analog = Analog input P = Power
ST = Schmi	tt Trigg	jer input v	with Cl	MOS levels O = Output I = Input

TABLE 1-1:	PINOUT I/O DESCRIPTIONS	(CONTINUED)
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Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.

PPS = Peripheral Pin Select

3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)" for more information.

TTL = TTL input buffer

4: Not all pins are available in all packages variants. See the "Pin Diagrams" section for pin availability.

**5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

# 3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

# 3.1 Registers

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls.

# 3.2 Instruction Set

The instruction set for dsPIC33EPXXXGP50X and dsPIC33EPXXXMC20X/50X devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The instruction set for PIC24EPXXXGP/MC20X devices has the MCU class of instructions only and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

## 3.3 Data Space Addressing

The base Data Space can be addressed as 64 Kbytes (32K words).

The Data Space includes two ranges of memory, referred to as X and Y data memory. Each memory range is accessible through its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Spaces have memory locations that are device-specific, and are described further in the data memory maps in **Section 4.2 "Data Address Space"**.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 32-Kbyte aligned program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to the "**Data Memory**" (DS70595) and "**Program Memory**" (DS70613) sections in the "*dsPIC33/PIC24 Family Reference Manual*" for more details on EDS, PSV and table accesses.

On the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms. PIC24EPXXXGP/MC20X devices do not support Modulo and Bit-Reversed Addressing.

# 3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- · Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

### 3.7 CPU Control Registers

R/W-0	) R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
0A <sup>(1)</sup>	OB <sup>(1)</sup>	SA <sup>(1,4)</sup>	SB <sup>(1,4)</sup>	OAB <sup>(1)</sup>	SAB <sup>(1)</sup>	DA <sup>(1)</sup>	DC
bit 15							bit 8
R/W-0 <sup>(2</sup>	R/W-0 <sup>(2,3)</sup>	R/W-0 <sup>(2,3)</sup>	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2	IPL1	IPL0	RA	N	OV	Z	С
bit 7							bit 0
Legend:		C = Clearable	bit				
R = Reada	able bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value	e at POR	'1'= Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	OA: Accumu	lator A Overflow	v Status bit <sup>(1)</sup>				
	1 = Accumula	ator A has over	flowed				
	0 = Accumula	ator A has not c	verflowed				
bit 14	OB: Accumu	lator B Overflov	v Status bit <sup>(1)</sup>				
	1 = Accumula	ator B has over	flowed				
hit 13		lator A Saturatio	n 'Sticky' Sta	tue hit(1,4)			
DIL 15	$1 = \Delta c cumula$	ator A is saturat	ed or has her	n saturated at	some time		
	0 = Accumula	ator A is not sat	urated		Some time		
bit 12	SB: Accumu	lator B Saturatio	on 'Sticky' Sta	tus bit <sup>(1,4)</sup>			
	1 = Accumula	ator B is satura	ed or has bee	en saturated at	some time		
	0 = Accumula	ator B is not sat	urated				
bit 11	<b>OAB:</b> OA    (	OB Combined A	ccumulator O	verflow Status	bit <sup>(1)</sup>		
	1 = Accumula	ators A or B have	ve overflowed				
	0 = Neither A	Accumulators A	or B have ove	erflowed	(1)		
bit 10	SAB: SA    S	B Combined A	cumulator 'Si	icky Status bit		<b>1</b>	
	1 = Accumula  0 = Neither A	ators A or B are	or B are satur	nave been sat	urated at some	time	
hit 9		Active hit(1)		alou			
bit 0	1 = DO loop is	s in progress					
	0 = DO loop is	s not in progres	S				
bit 8	DC: MCU AL	U Half Carry/Bo	orrow bit				
	1 = A carry-o	out from the 4th	low-order bit (	for byte-sized o	data) or 8th low-	order bit (for wo	ord-sized data)
	of the re	sult occurred					
	0 = No carry	-out from the 4	th low-order t	bit (for byte-siz	ed data) or 8th	low-order bit (1	for word-sized
	uala) U						
Note 1:	This bit is availabl	e on dsPIC33E	PXXXMC20X	/50X and dsPl	C33EPXXXGP	50X devices on	ly.
2:	The IPL<2:0> bits	are concatenat	ed with the IF	PL<3> bit (COR	RCON<3>) to fo	rm the CPU Inte	errupt Priority
	Level. The value I IPL< $3 > = 1$ .	n parentheses i	naicates the I	PL, IT IPL<3> =	= ⊥. User interru	ipts are disable	a wnen

#### REGISTER 3-1: SR: CPU STATUS REGISTER

- 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- **4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.





#### TABLE 4-46: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	TRISA12	TRISA11	TRISA10	TRISA9	TRISA8	TRISA7	—	—	TRISA4	-	—	TRISA1	TRISA0	1F93
PORTA	0E02	_	_	_	RA12	RA11	RA10	RA9	RA8	RA7	_	_	RA4	_	_	RA1	RA0	0000
LATA	0E04	_	_	_	LATA12	LATA11	LATA10	LATA9	LATA8	LATA7	_	_	LATA4	_	_	LA1TA1	LA0TA0	0000
ODCA	0E06	_	_	_	ODCA12	ODCA11	ODCA10	ODCA9	ODCA8	ODCA7	_	_	ODCA4	_	_	ODCA1	ODCA0	0000
CNENA	0E08	_	_	_	CNIEA12	CNIEA11	CNIEA10	CNIEA9	CNIEA8	CNIEA7	_	_	CNIEA4	_	_	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	CNPUA12	CNPUA11	CNPUA10	CNPUA9	CNPUA8	CNPUA7	_	_	CNPUA4	_	_	CNPUA1	CNPUA0	0000
CNPDA	0E0C	_	_	_	CNPDA12	CNPDA11	CNPDA10	CNPDA9	CNPDA8	CNPDA7	_	_	CNPDA4	_	_	CNPDA1	CNPDA0	0000
ANSELA	0E0E	_	_	—	ANSA12	ANSA11	—	_	_	—		—	ANSA4	-	_	ANSA1	ANSA0	1813

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### TABLE 4-47: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	_	_	_	_		—	_	ANSB8		—	-		ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### TABLE 4-48: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	TRISC15	_	TRISC13	TRISC12	TRISC11	TRISC10	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	BFFF
PORTC	0E22	RC15	-	RC13	RC12	RC11	RC10	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	LATC15	-	LATC13	LATC12	LATC11	LATC10	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	ODCC15	_	ODCC13	ODCC12	ODCC11	ODCC10	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	CNIEC15	_	CNIEC13	CNIEC12	CNIEC11	CNIEC10	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	CNPUC15	_	CNPUC13	CNPUC12	CNPUC11	CNPUC10	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	CNPDC15	_	CNPDC13	CNPDC12	CNPDC11	CNPDC10	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E		-	-	—	ANSC11	_		_	—	—	_		—	ANSC2	ANSC1	ANSC0	0807

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0
I a manuali							

### REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 Unimplemented: Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits 011111 = Maximum frequency deviation of 1.453% (7.477 MHz) 011110 = Center frequency + 1.406% (7.474 MHz) •••• 000001 = Center frequency + 0.047% (7.373 MHz) 000000 = Center frequency (7.37 MHz nominal) 111111 = Center frequency - 0.047% (7.367 MHz) ••• 100001 = Center frequency - 1.453% (7.263 MHz) 100000 = Minimum frequency deviation of -1.5% (7.259 MHz)

### 10.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- · Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into Standby when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

### 10.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- · The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see Section 10.4 "Peripheral Module Disable").
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- · Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction or the first instruction in the Interrupt Service Routine (ISR).

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the TSIDL bit in the Timer1 Control register (T1CON<13>).

### 10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode. NOTES:

### 15.1 Output Compare Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

#### 15.1.1 KEY RESOURCES

- "Output Compare" (DS70358) in the "dsPIC33/ PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-26:	CxTRmnCON: ECANx TX/RX BUFFER mn CONTROL REGISTER	
	(m = 0,2,4,6; n = 1,3,5,7)	

R/W-0	) R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXEN	n TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15							bit 8
R/W-0	) R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENr	m TXABTm <sup>(1)</sup>	TXLARBm <sup>(1)</sup>	TXERRm <sup>(1)</sup>	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7							bit 0
r							
Legend:							
R = Read	able bit	W = Writable	bit	U = Unimplei	mented bit, read	d as '0'	
-n = Value	e at POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15-8	See Definition	n for bits<7:0>,	Controls Buffe	er n			
bit 7	TXENm: TX/	RX Buffer Sele	ction bit				
	1 = Buffer TR	Bn is a transm	it buffer				
		Bn is a receive					
bit 6	TXABTm: Me	essage Abortec	bit				
	1 = Message	was aborted	nemission succ	ressfully			
hit 5			whitration hit(1)	)			
bit o	1 = Message	lost arbitration	while being se	nt			
	0 = Message	did not lose ar	bitration while	being sent			
bit 4	TXERRm: Er	ror Detected D	uring Transmis	ssion bit <sup>(1)</sup>			
	1 = A bus err	or occurred wh	ile the messag	je was being s	sent		
	0 = A bus error	or did not occu	r while the me	ssage was be	ing sent		
bit 3	TXREQm: Me	essage Send R	equest bit				
	1 = Requests	s that a messag	ge be sent; the	bit automatic	ally clears wher	n the message i	s successfully
	o = Clearing	the hit to '0' wh	nile set reques	ts a messarie	abort		
hit 2		ito-Remote Tra	ine set reques	hit	abort		
511 2	1 = When a result of the second sec	emote transmit	is received T	XRFQ will be	set		
	0 = When a r	emote transmit	is received, T	XREQ will be	unaffected		
bit 1-0	TXmPRI<1:0	>: Message Tra	ansmission Pri	iority bits			
	11 = Highest	message priori	ity				
	10 = High inte	ermediate mes	sage priority				
	01 = Low interview	ermediate mess	age priority				
		messaye priori	Ly				
Note 1:	This bit is cleared	when TXREQ i	s set.				

Note: The buffers, SID, EID, DLC, Data Field, and Receive Status registers are located in DMA RAM.

# 27.5 Watchdog Timer (WDT)

For dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

#### 27.5.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT Timeout period (TWDT), as shown in Parameter SY12 in Table 30-22.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- · On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution
- Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.



### FIGURE 27-2: WDT BLOCK DIAGRAM

# 27.5.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3,2>) needs to be cleared in software after the device wakes up.

# 27.5.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

### 27.5.4 WDT WINDOW

The Watchdog Timer has an optional Windowed mode, enabled by programming the WINDIS bit in the WDT Configuration register (FWDT<6>). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window select bits (WDTWIN<1:0>).

Field	Description
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 working registers ∈ {W0W15}
Wnd	One of 16 destination working registers ∈ {W0W15}
Wns	One of 16 source working registers ∈ {W0W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}

TABLE 28-1:	SYMBOLS USED IN OPCODE DESCRIPTIONS (	(CONTINUED)

#### TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic	Min. Typ. <sup>(1)</sup> Max. Units Conditions						
OS50	Fplli	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	_	8.0	MHz	ECPLL, XTPLL modes		
OS51	Fvco	On-Chip VCO System Frequency	120	_	340	MHz			
OS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	ms			
OS53	DCLK	CLKO Stability (Jitter) <sup>(2)</sup>	-3	0.5	3	%			

**Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases, or communication clocks used by the application, use the following formula:

$$Effective Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Time Base or Communication Clock}}}$$

For example, if Fosc = 120 MHz and the SPIx bit rate = 10 MHz, the effective jitter is as follows:

Effective Jitter = 
$$\frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

#### TABLE 30-19: INTERNAL FRC ACCURACY

АС СНА	RACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended							
Param No.	Characteristic	Min.	Тур.	Max.	Units	Conditions			
Internal	FRC Accuracy @ FRC Fre	equency =	7.37 MHz	<u>(</u> 1)					
F20a	FRC	-1.5	0.5	+1.5	%	$-40^{\circ}C \le TA \le -10^{\circ}C$	VDD = 3.0-3.6V		
		-1	0.5	+1	%	$-10^{\circ}C \leq TA \leq +85^{\circ}C$	VDD = 3.0-3.6V		
F20b	FRC	-2	1	+2	%	$+85^{\circ}C \le TA \le +125^{\circ}C$	VDD = 3.0-3.6V		

Note 1: Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

#### TABLE 30-20: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param No. Characteristic		Min.	Тур.	Max.	Units	Conditions			
LPRC (	@ 32.768 kHz <sup>(1)</sup>								
F21a	LPRC	-30		+30	%	$-40^\circ C \le T A \le -10^\circ C$	VDD = 3.0-3.6V		
		-20		+20	%	$-10^{\circ}C \le TA \le +85^{\circ}C$	VDD = 3.0-3.6V		
F21b	LPRC	-30		+30	%	$+85^{\circ}C \leq TA \leq +125^{\circ}C$	VDD = 3.0-3.6V		

**Note 1:** The change of LPRC frequency as VDD changes.

AC CHARACTERISTICS			Standar (unless Operatir	d Opera otherwi ng tempe	ting Cor se stated rature	ditions: 1) <sup>(1)</sup> -40°C ≤ <sup>°</sup> -40°C ≤ <sup>°</sup>	: <b>3.0V to 3.6V</b> TA $\leq$ +85°C for Industrial TA $\leq$ +125°C for Extended
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
		ADC /	Accuracy	/ (12-Bit	Mode)		
AD20a	Nr	Resolution	12	2 Data Bi	its	bits	
AD21a	INL	Integral Nonlinearity	-2.5		2.5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-5.5	_	5.5	LSb	+85°C < TA $\leq$ +125°C (Note 2)
AD22a	DNL	Differential Nonlinearity	-1		1	LSb	-40°C $\leq$ TA $\leq$ +85°C (Note 2)
			-1		1	LSb	+85°C < TA $\leq$ +125°C (Note 2)
AD23a	Gerr	Gain Error <sup>(3)</sup>	-10		10	LSb	-40°C $\leq$ TA $\leq$ +85°C (Note 2)
			-10		10	LSb	+85°C < TA $\leq$ +125°C (Note 2)
AD24a	EOFF	Offset Error	-5		5	LSb	$-40^{\circ}C \le TA \le +85^{\circ}C$ (Note 2)
			-5		5	LSb	+85°C < TA $\leq$ +125°C (Note 2)
AD25a	—	Monotonicity	_			—	Guaranteed
		Dynamic	Performa	ance (12	-Bit Mod	e)	
AD30a	THD	Total Harmonic Distortion <sup>(3)</sup>	_	75		dB	
AD31a	SINAD	Signal to Noise and Distortion <sup>(3)</sup>	_	68	-	dB	
AD32a	SFDR	Spurious Free Dynamic Range <sup>(3)</sup>		80	_	dB	
AD33a	Fnyq	Input Signal Bandwidth <sup>(3)</sup>	_	250		kHz	
AD34a	ENOB	Effective Number of Bits <sup>(3)</sup>	11.09	11.3	_	bits	

## TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) <sup>(1)</sup> Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
		ADC A	ccuracy (	10-Bit N	lode)		
AD20b	Nr	Resolution	10	) Data B	its	bits	
AD21b	INL	Integral Nonlinearity	-0.625		0.625	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-1.5		1.5	LSb	+85°C < TA ≤ +125°C (Note 2)
AD22b	DNL	Differential Nonlinearity	-0.25	_	0.25	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-0.25	_	0.25	LSb	$+85^{\circ}C < TA \le +125^{\circ}C$ (Note 2)
AD23b	Gerr	Gain Error	-2.5		2.5	LSb	-40°C $\leq$ TA $\leq$ +85°C (Note 2)
			-2.5		2.5	LSb	+85°C < TA $\leq$ +125°C (Note 2)
AD24b	EOFF	Offset Error	-1.25		1.25	LSb	-40°C $\leq$ TA $\leq$ +85°C (Note 2)
			-1.25		1.25	LSb	+85°C < TA $\leq$ +125°C (Note 2)
AD25b	—	Monotonicity	_	_	_		Guaranteed
		Dynamic P	erforman	ce (10-E	Bit Mode)		
AD30b	THD	Total Harmonic Distortion <sup>(3)</sup>	—	64	—	dB	
AD31b	SINAD	Signal to Noise and Distortion <sup>(3)</sup>	-	57	_	dB	
AD32b	SFDR	Spurious Free Dynamic Range <sup>(3)</sup>	—	72	—	dB	
AD33b	Fnyq	Input Signal Bandwidth <sup>(3)</sup>	—	550	—	kHz	
AD34b	ENOB	Effective Number of Bits <sup>(3)</sup>	—	9.4	—	bits	

### TABLE 30-59: ADC MODULE SPECIFICATIONS (10-BIT MODE)

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

**3:** Parameters are characterized but not tested in manufacturing.

NOTES:

# 31.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between  $-40^{\circ}$ C to  $+150^{\circ}$ C are identical to those shown in **Section 30.0** "**Electrical Characteristics**" for operation between  $-40^{\circ}$ C to  $+125^{\circ}$ C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in **Section 30.0 "Electrical Characteristics"** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

# Absolute Maximum Ratings<sup>(1)</sup>

Ambient temperature under bias <sup>(2)</sup>	40°C to +150°C
Storage temperature	-65°C to +160°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to Vss <sup>(3)</sup>	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD < 3.0V <sup>(3)</sup>	-0.3V to 3.6V
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 3.0V^{(3)}$	-0.3V to 5.5V
Maximum current out of Vss pin	60 mA
Maximum current into VDD pin <sup>(4)</sup>	60 mA
Maximum junction temperature	+155°C
Maximum current sourced/sunk by any 4x I/O pin	10 mA
Maximum current sourced/sunk by any 8x I/O pin	
Maximum current sunk by all ports combined	70 mA
Maximum current sourced by all ports combined <sup>(4)</sup>	70 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
  - 2: AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time from +125°C to +150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.
  - 3: Refer to the "Pin Diagrams" section for 5V tolerant pins.
  - 4: Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$						
Param No.	Symbol	Characteristic	Min Typ Max		Units	Conditions			
ADC Accuracy (12-Bit Mode) <sup>(1)</sup>									
HAD20a	Nr	Resolution <sup>(3)</sup>	1:	2 Data B	its	bits			
HAD21a	INL	Integral Nonlinearity	-5.5	_	5.5	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V		
HAD22a	DNL	Differential Nonlinearity	-1	—	1	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V		
HAD23a	Gerr	Gain Error	-10	_	10	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V		
HAD24a	EOFF	Offset Error	-5	—	5	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V		
		Dynamic	Performa	nce (12·	Bit Mode	e) <sup>(2)</sup>			
HAD33a	FNYQ	Input Signal Bandwidth	_	_	200	kHz			

# TABLE 31-12: ADC MODULE SPECIFICATIONS (12-BIT MODE)

**Note 1:** These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

## TABLE 31-13: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$								
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions				
	ADC Accuracy (10-Bit Mode) <sup>(1)</sup>										
HAD20b	Nr	Resolution <sup>(3)</sup>	10	) Data B	its	bits					
HAD21b	INL	Integral Nonlinearity	-1.5	_	1.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V				
HAD22b	DNL	Differential Nonlinearity	-0.25	—	0.25	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V				
HAD23b	Gerr	Gain Error	-2.5	_	2.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V				
HAD24b	EOFF	Offset Error	-1.25	_	1.25	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V				
	Dynamic Performance (10-Bit Mode) <sup>(2)</sup>										
HAD33b	HAD33b FNYQ Input Signal Bandwidth — 400 kHz										

Note 1: These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

## 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	0.65 BSC			
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44) Y				0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B