What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
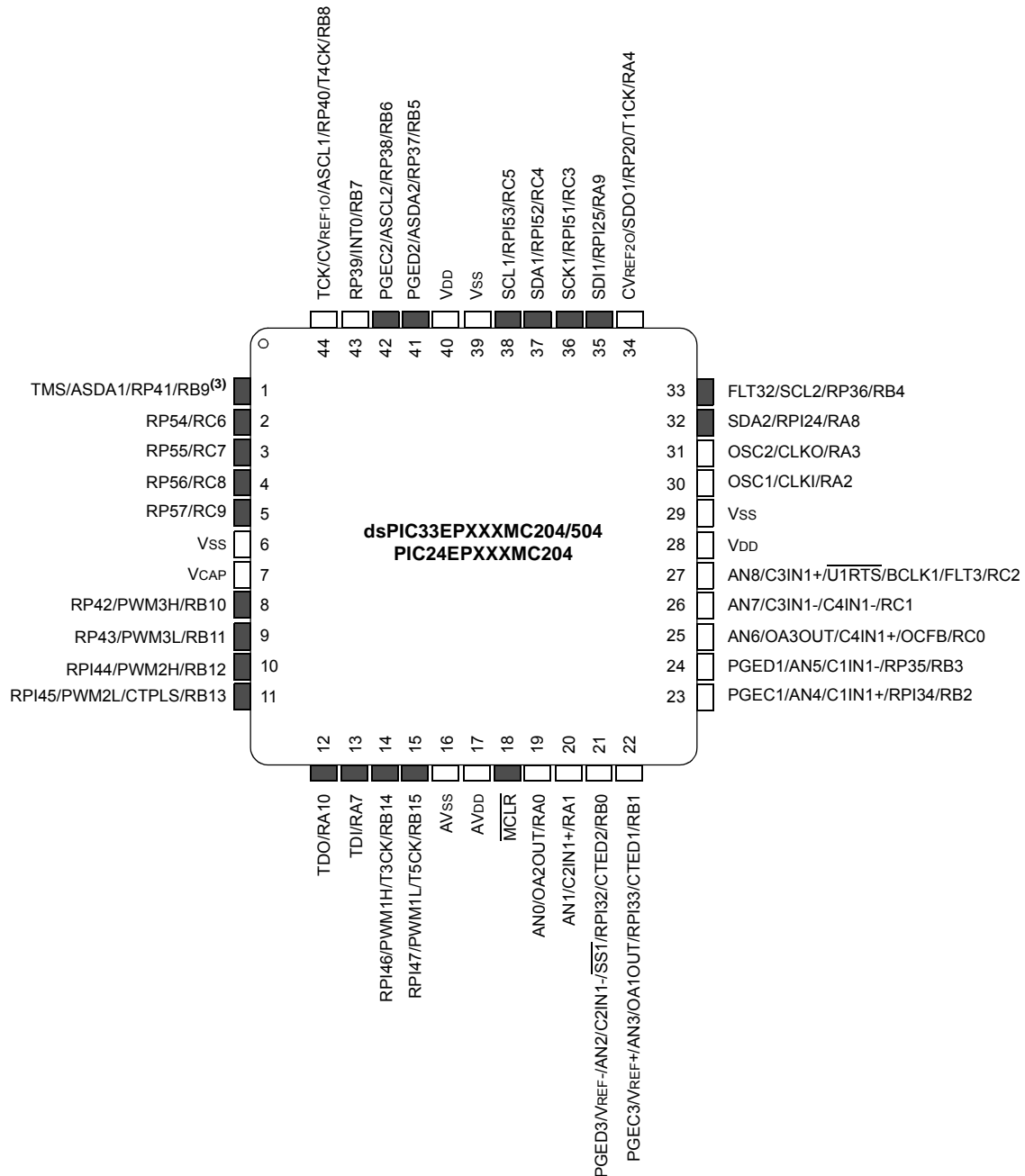
Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mc504-i-pt

Pin Diagrams (Continued)

44-Pin TQFP[1,2]

■ = Pins are up to 5V tolerant

Top pins (44–34):
- 44 TCK/CV$_{REF1O}$/ASCL1/RP40/T4CK/RB8
- 43 RP39/INT0/RB7
- 42 PGEC2/ASCL2/RP38/RB6
- 41 PGED2/ASDA2/RP37/RB5
- 40 V$_{DD}$
- 39 V$_{SS}$
- 38 SCL1/RPI53/RC5
- 37 SDA1/RPI52/RC4
- 36 SCK1/RPI51/RC3
- 35 SDI1/RPI25/RA9
- 34 CV$_{REF2O}$/SDO1/RP20/T1CK/RA4

Left pins (1–11):
- 1 TMS/ASDA1/RP41/RB9[3]
- 2 RP54/RC6
- 3 RP55/RC7
- 4 RP56/RC8
- 5 RP57/RC9
- 6 V$_{SS}$
- 7 V$_{CAP}$
- 8 RP42/PWM3H/RB10
- 9 RP43/PWM3L/RB11
- 10 RPI44/PWM2H/RB12
- 11 RPI45/PWM2L/CTPLS/RB13

Device:
dsPIC33EPXXXMC204/504
PIC24EPXXXMC204

Right pins (33–23):
- 33 FLT32/SCL2/RP36/RB4
- 32 SDA2/RPI24/RA8
- 31 OSC2/CLKO/RA3
- 30 OSC1/CLKI/RA2
- 29 V$_{SS}$
- 28 V$_{DD}$
- 27 AN8/C3IN1+/$\overline{U1RTS}$/BCLK1/FLT3/RC2
- 26 AN7/C3IN1-/C4IN1-/RC1
- 25 AN6/OA3OUT/C4IN1+/OCFB/RC0
- 24 PGED1/AN5/C1IN1-/RP35/RB3
- 23 PGEC1/AN4/C1IN1+/RPI34/RB2

Bottom pins (12–22):
- 12 TDO/RA10
- 13 TDI/RA7
- 14 RPI46/PWM1H/T3CK/RB14
- 15 RPI47/PWM1L/T5CK/RB15
- 16 AV$_{SS}$
- 17 AV$_{DD}$
- 18 $\overline{MCLR}$
- 19 AN0/OA2OUT/RA0
- 20 AN1/C2IN1+/RA1
- 21 PGED3/V$_{REF}$-/AN2/C2IN1-/$\overline{SS1}$/RPI32/CTED2/RB0
- 22 PGEC3/V$_{REF}$+/AN3/OA1OUT/RPI33/CTED1/RB1

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Table of Contents

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name[4]	Pin Type	Buffer Type	PPS	Description
U2CTS	I	ST	No	UART2 Clear-To-Send.
U2RTS	O	—	No	UART2 Ready-To-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
BCLK2	O	ST	No	UART2 IrDA® baud clock output.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	O	—	No	SPI1 data out.
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS[5]	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
C1RX[2]	I	ST	Yes	ECAN1 bus receive pin.
C1TX[2]	O	—	Yes	ECAN1 bus transmit pin.
FLT1[1], FLT2[1]	I	ST	Yes	PWM Fault Inputs 1 and 2.
FLT3[1], FLT4[1]	I	ST	No	PWM Fault Inputs 3 and 4.
FLT32[1,3]	I	ST	No	PWM Fault Input 32 (Class B Fault).
DTCMP1-DTCMP3[1]	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 through 3.
PWM1L-PWM3L[1]	O	—	No	PWM Low Outputs 1 through 3.
PWM1H-PWM3H[1]	O	—	No	PWM High Outputs 1 through 3.
SYNCI1[1]	I	ST	Yes	PWM Synchronization Input 1.
SYNCO1[1]	O	—	Yes	PWM Synchronization Output 1.
INDX1[1]	I	ST	Yes	Quadrature Encoder Index1 pulse input.
HOME1[1]	I	ST	Yes	Quadrature Encoder Home1 pulse input.
QEA1[1]	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer external clock/gate input in Timer mode.
QEB1[1]	I	ST	Yes	Quadrature Encoder Phase B input in QEI1 mode. Auxiliary timer external clock/gate input in Timer mode.
CNTCMP1[1]	O	—	Yes	Quadrature Encoder Compare Output 1.

Legend: CMOS = CMOS compatible input or output   Analog = Analog input   P = Power
ST = Schmitt Trigger input with CMOS levels   O = Output   I = Input
PPS = Peripheral Pin Select   TTL = TTL input buffer

Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

  2: This pin is available on dsPIC33EPXXXGP/MC50X devices only.

  3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"** for more information.

  4: Not all pins are available in all packages variants. See the **"Pin Diagrams"** section for pin availability.

  5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 4-7: **DATA MEMORY MAP FOR dsPIC33EP32MC20X/50X AND dsPIC33EP32GP50X DEVICES**

Note: Memory areas are not shown to scale.
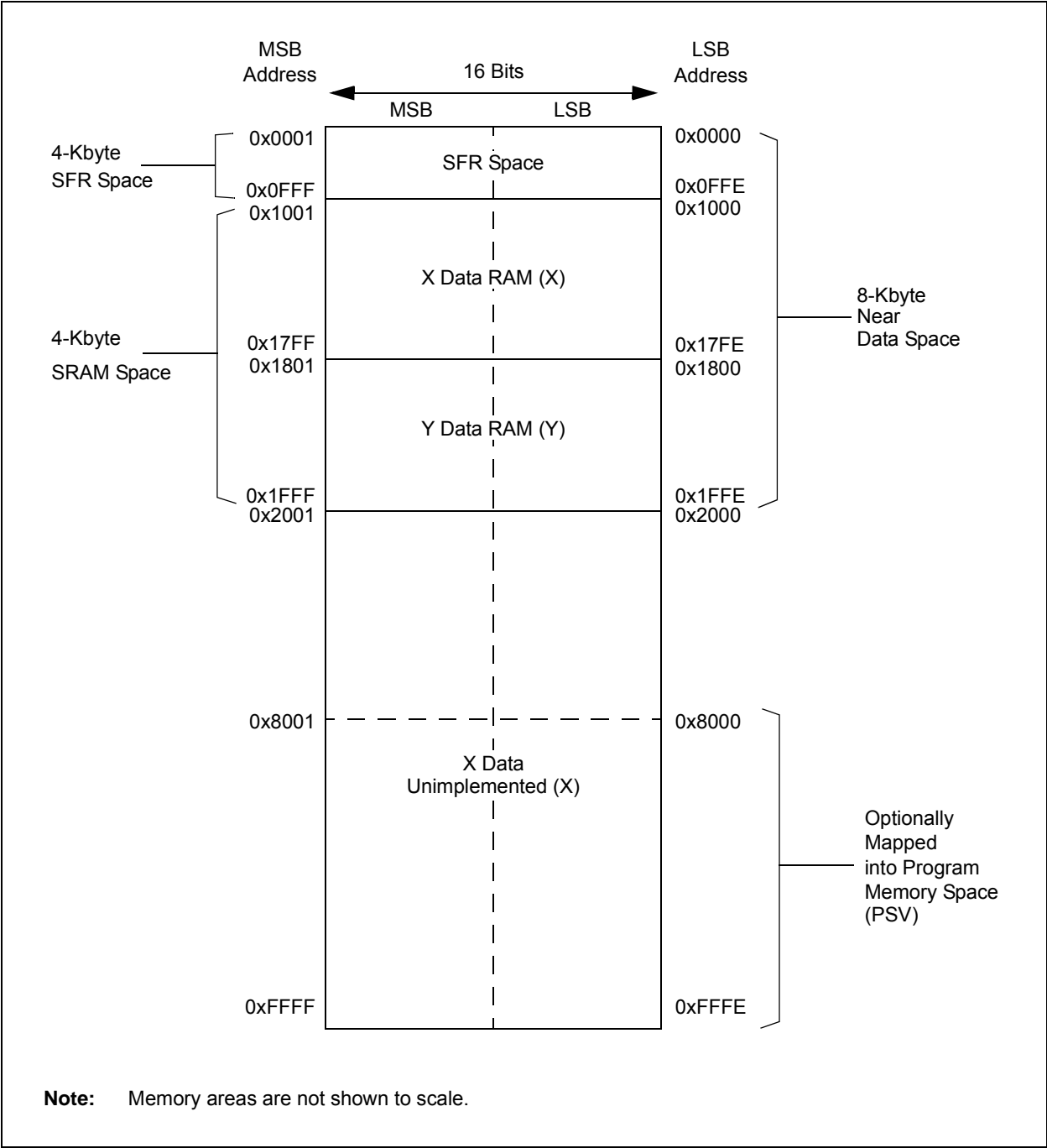
TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC23	086E	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC24	0870	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IP<2:0>			0004
IPC35	0886	—	JTAGIP<2:0>			—	ICDIP<2:0>			—	—	—	—	—	—	—	—	4400
IPC36	0888	—	PTG0IP<2:0>			—	PTGWDTIP<2:0>			—	PTGSTEPIP<2:0>			—	—	—	—	4440
IPC37	088A	—	—	—	—	—	PTG3IP<2:0>			—	PTG2IP<2:0>			—	PTG1IP<2:0>			0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR<3:0>				VECNUM<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
  - In Word mode, this instruction maps the lower word of the Program Space location (P<15:0>) to a data address (D<15:0>)

- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

- TBLRDH (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. The 'phantom' byte (D<15:8>) is always '0'.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to D<7:0> of the data address in the TBLRDL instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

FIGURE 4-23:   ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS
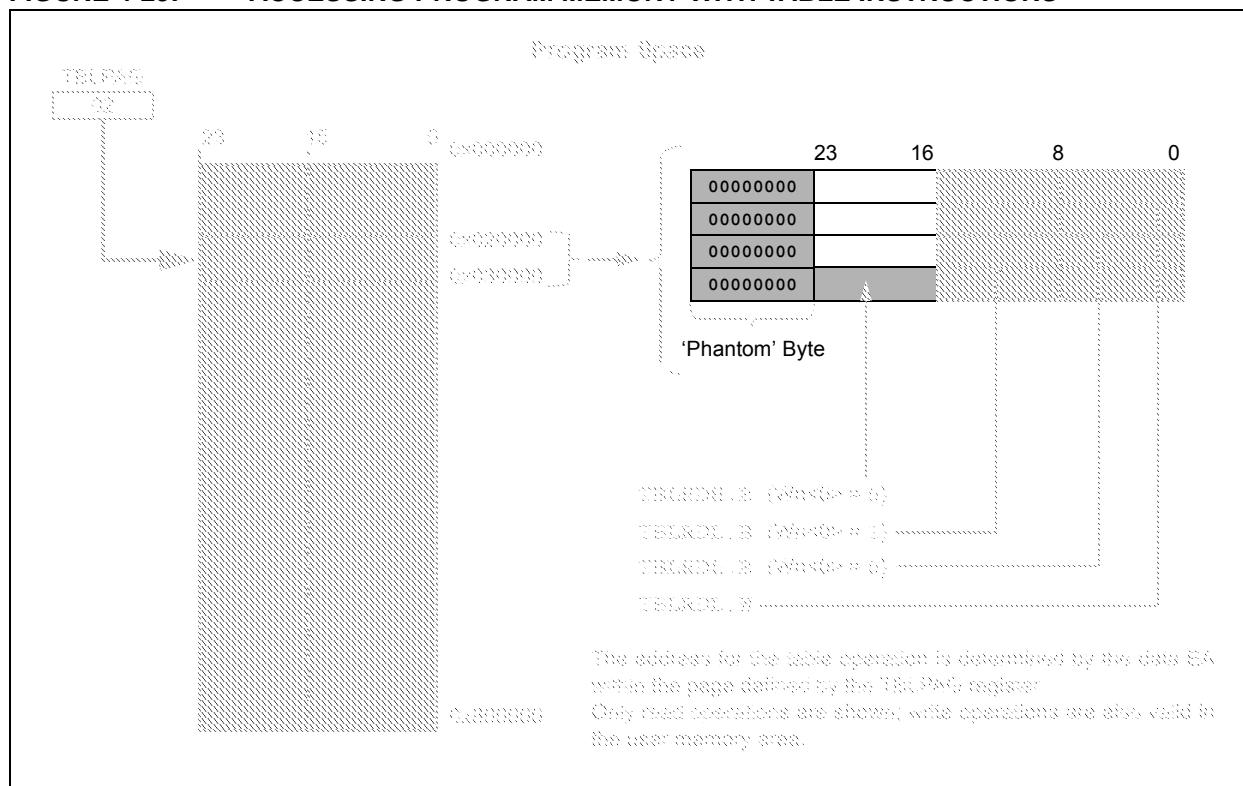
9.3   Oscillator Control Registers

REGISTER 9-1:   OSCCON: OSCILLATOR CONTROL REGISTER[1]

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC2	COSC1	COSC0	—	NOSC2[2]	NOSC1[2]	NOSC0[2]
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF[3]	—	—	OSWEN
bit 7							bit 0

Legend:		y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-12   **COSC<2:0>:** Current Oscillator Selection bits (read-only)
                111 = Fast RC Oscillator (FRC) with Divide-by-n
                110 = Fast RC Oscillator (FRC) with Divide-by-16
                101 = Low-Power RC Oscillator (LPRC)
                100 = Reserved
                011 = Primary Oscillator (XT, HS, EC) with PLL
                010 = Primary Oscillator (XT, HS, EC)
                001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
                000 = Fast RC Oscillator (FRC)

bit 11   **Unimplemented:** Read as '0'

bit 10-8   **NOSC<2:0>:** New Oscillator Selection bits[2]
                111 = Fast RC Oscillator (FRC) with Divide-by-n
                110 = Fast RC Oscillator (FRC) with Divide-by-16
                101 = Low-Power RC Oscillator (LPRC)
                100 = Reserved
                011 = Primary Oscillator (XT, HS, EC) with PLL
                010 = Primary Oscillator (XT, HS, EC)
                001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
                000 = Fast RC Oscillator (FRC)

bit 7   **CLKLOCK:** Clock Lock Enable bit
                1 = If (FCKSM0 = 1), then clock and PLL configurations are locked; if (FCKSM0 = 0), then clock and
                    PLL configurations may be modified
                0 = Clock and PLL selections are not locked, configurations may be modified

bit 6   **IOLOCK:** I/O Lock Enable bit
                1 = I/O lock is active
                0 = I/O lock is not active

bit 5   **LOCK:** PLL Lock Status bit (read-only)
                1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
                0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

Note 1:   Writes to this register require an unlock sequence. Refer to **"Oscillator"** (DS70580) in the *"dsPIC33/
            PIC24 Family Reference Manual"* (available from the Microchip web site) for details.

2:   Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted.
            This applies to clock switches in either direction. In these instances, the application must switch to FRC
            mode as a transitional clock source between the two PLL modes.

3:   This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an
            actual oscillator failure and trigger an oscillator failure trap.

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than V_{DD} by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum V_{IH} specification for that particular pin.

See the **"Pin Diagrams"** section for the available 5V tolerant pins and Table 30-11 for the maximum V_{IH} specification for each pin.

11.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (V_{OH} or V_{OL}) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP, as shown in Example 11-1.

11.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the Change Notification (CN) functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pull-downs act as a current source or sink source connected to the pin and eliminate the need for external resistors when push button, or keypad devices are connected. The pull-ups and pull-downs are enabled separately, using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note:	Pull-ups and pull-downs on Change Notification pins should always be disabled when the port pin is configured as a digital output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

```
MOV     0xFF00, W0   ; Configure PORTB<15:8>
                     ; as inputs
MOV     W0, TRISB    ; and PORTB<7:0>
                     ; as outputs
NOP                  ; Delay 1 cycle
BTSS    PORTB, #13   ; Next Instruction
```

REGISTER 11-5:   RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC4R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC3R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15　　　　**Unimplemented:** Read as '0'

bit 14-8　　　**IC4R<6:0>:** Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits
　　　　　　　(see Table 11-2 for input pin selection numbers)
　　　　　　　1111001 = Input tied to RPI121
　　　　　　　.
　　　　　　　.
　　　　　　　.
　　　　　　　0000001 = Input tied to CMP1
　　　　　　　0000000 = Input tied to Vss

bit 7　　　　 **Unimplemented:** Read as '0'

bit 6-0　　　 **IC3R<6:0>:** Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits
　　　　　　　(see Table 11-2 for input pin selection numbers)
　　　　　　　1111001 = Input tied to RPI121
　　　　　　　.
　　　　　　　.
　　　　　　　.
　　　　　　　0000001 = Input tied to CMP1
　　　　　　　0000000 = Input tied to Vss

REGISTER 11-10: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	U1RXR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **U1RXR<6:0>:** Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-11: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	U2RXR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **U2RXR<6:0>:** Assign UART2 Receive (U2RX) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

16.3 PWMx Control Registers

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU[1]	SYNCPOL[1]	SYNCOEN[1]
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN[1]	SYNCSRC2[1]	SYNCSRC1[1]	SYNCSRC0[1]	SEVTPS3[1]	SEVTPS2[1]	SEVTPS1[1]	SEVTPS0[1]
bit 7							bit 0

Legend:		
	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15   **PTEN:** PWMx Module Enable bit
1 = PWMx module is enabled
0 = PWMx module is disabled

bit 14   **Unimplemented:** Read as '0'

bit 13   **PTSIDL:** PWMx Time Base Stop in Idle Mode bit
1 = PWMx time base halts in CPU Idle mode
0 = PWMx time base runs in CPU Idle mode

bit 12   **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending

bit 11   **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled

bit 10   **EIPU:** Enable Immediate Period Updates bit[1]
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWMx cycle boundaries

bit 9   **SYNCPOL:** Synchronize Input and Output Polarity bit[1]
1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
0 = SYNCI1/SYNCO1 is active-high

bit 8   **SYNCOEN:** Primary Time Base Sync Enable bit[1]
1 = SYNCO1 output is enabled
0 = SYNCO1 output is disabled

bit 7   **SYNCEN:** External Time Base Synchronization Enable bit[1]
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

Note 1:   These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user
application must program the period register with a value that is slightly larger than the expected period of
the external synchronization input signal.

2:   See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for information on this selection.

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7							bit 0

Legend:		C = Clearable bit	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I²C™ master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware is set or clear at the end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No bus collision detected
Hardware is set at detection of a bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware is set when address matches general call address. Hardware is clear at Stop detection.

bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.

bit 7 **IWCOL:** I2Cx Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I²C module is busy
0 = No collision
Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register was still holding the previous byte
0 = No overflow
Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as I²C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	AMSK9	AMSK8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10   **Unimplemented:** Read as '0'

bit 9-0   **AMSK<9:0>:** Address Mask Select bits

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax + 1; bit match is required in this position

20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"UART"** (DS70582) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices contains two UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins, and also includes an IrDA® encoder and decoder.

Note: Hardware flow control using UxRTS and UxCTS is not available on all pin count devices. See the **"Pin Diagrams"** section for availability.

The primary features of the UARTx module are:

• Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
• Even, Odd or No Parity Options (for 8-bit data)
• One or Two Stop bits
• Hardware Flow Control Option with UxCTS and UxRTS Pins
• Fully Integrated Baud Rate Generator with 16-Bit Prescaler
• Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
• Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
• 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
• 4-Deep FIFO Receive Data Buffer
• Parity, Framing and Buffer Overrun Error Detection
• Support for 9-bit mode with Address Detect (9th bit = 1)
• Transmit and Receive Interrupts
• A Separate Interrupt for all UARTx Error Conditions
• Loopback mode for Diagnostic Support
• Support for Sync and Break Characters
• Support for Automatic Baud Rate Detection
• IrDA® Encoder and Decoder Logic
• 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 20-1. The UARTx module consists of these key hardware elements:

• Baud Rate Generator
• Asynchronous Transmitter
• Asynchronous Receiver

FIGURE 20-1: UARTx SIMPLIFIED BLOCK DIAGRAM
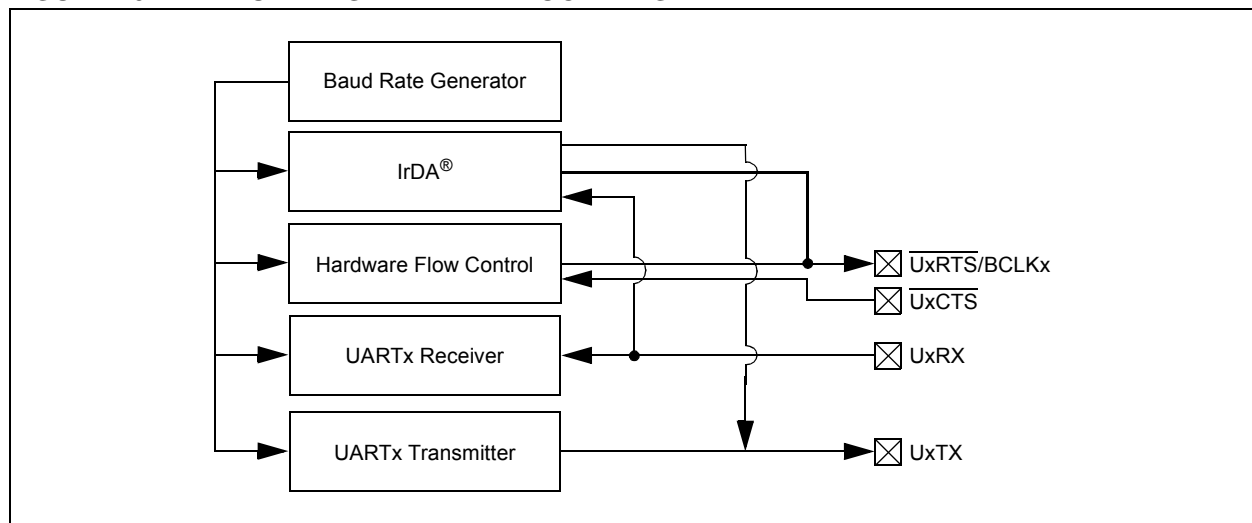
REGISTER 21-5: CxFIFO: ECANx FIFO STATUS REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0
bit 15							bit 8

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-14   **Unimplemented:** Read as '0'

bit 13-8   **FBP<5:0>:** FIFO Buffer Pointer bits
011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **FNRB<5:0>:** FIFO Next Read Buffer Pointer bits
011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

REGISTER 21-6:   CxINTF: ECANx INTERRUPT FLAG REGISTER (CONTINUED)

bit 1   **RBIF:** RX Buffer Interrupt Flag bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0   **TBIF:** TX Buffer Interrupt Flag bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP<3:0>				F6BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP<3:0>				F4BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F7BP<3:0>:** RX Buffer Mask for Filter 7 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>:** RX Buffer Mask for Filter 6 bits (same values as bits<15:12>)

bit 7-4 **F5BP<3:0>:** RX Buffer Mask for Filter 5 bits (same values as bits<15:12>)

bit 3-0 **F4BP<3:0>:** RX Buffer Mask for Filter 4 bits (same values as bits<15:12>)

REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11BP<3:0>				F10BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F9BP<3:0>				F8BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F11BP<3:0>:** RX Buffer Mask for Filter 11 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F10BP<3:0>:** RX Buffer Mask for Filter 10 bits (same values as bits<15:12>)

bit 7-4 **F9BP<3:0>:** RX Buffer Mask for Filter 9 bits (same values as bits<15:12>)

bit 3-0 **F8BP<3:0>:** RX Buffer Mask for Filter 8 bits (same values as bits<15:12>)

NOTES:

TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.[(1)]	Max.	Units	Conditions
OS50	F_{PLLI}	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8.0	MHz	ECPLL, XTPLL modes
OS51	F_{VCO}	On-Chip VCO System Frequency	120	—	340	MHz	
OS52	T_{LOCK}	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	ms	
OS53	D_{CLK}	CLKO Stability (Jitter)[(2)]	-3	0.5	3	%	

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases, or communication clocks used by the application, use the following formula:

$$Effective\ Jitter = \frac{D_{CLK}}{\sqrt{\dfrac{F_{OSC}}{Time\ Base\ or\ Communication\ Clock}}}$$

For example, if F_{OSC} = 120 MHz and the SPIx bit rate = 10 MHz, the effective jitter is as follows:

$$Effective\ Jitter = \frac{D_{CLK}}{\sqrt{\dfrac{120}{10}}} = \frac{D_{CLK}}{\sqrt{12}} = \frac{D_{CLK}}{3.464}$$

TABLE 30-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min.	Typ.	Max.	Units	Conditions	
Internal FRC Accuracy @ FRC Frequency = 7.37 MHz[(1)]							
F20a	FRC	-1.5	0.5	+1.5	%	-40°C ≤ TA ≤ -10°C	VDD = 3.0-3.6V
		-1	0.5	+1	%	-10°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F20b	FRC	-2	1	+2	%	+85°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

TABLE 30-20: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min.	Typ.	Max.	Units	Conditions	
LPRC @ 32.768 kHz[(1)]							
F21a	LPRC	-30	—	+30	%	-40°C ≤ TA ≤ -10°C	VDD = 3.0-3.6V
		-20	—	+20	%	-10°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F21b	LPRC	-30	—	+30	%	+85°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: The change of LPRC frequency as VDD changes.

FIGURE 30-28: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS