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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mc504t-i-tl">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mc504t-i-tl</a>

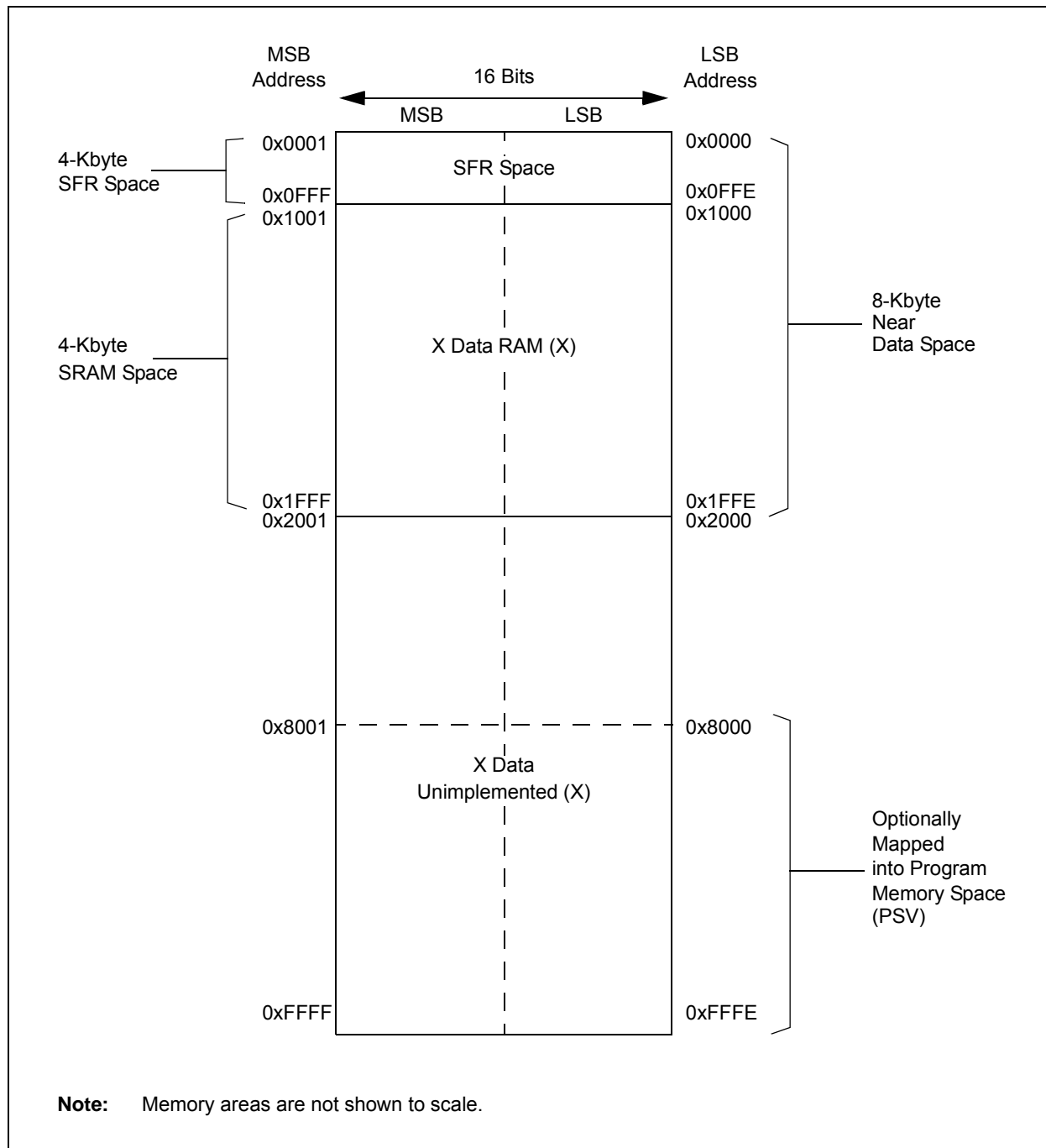
**TABLE 1-1: PINOUT I/O DESCRIPTIONS**

Pin Name <sup>(4)</sup>	Pin Type	Buffer Type	PPS	Description
AN0-AN15	I	Analog	No	Analog input channels.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKO	O	—	Yes	Reference clock output.
IC1-IC4	I	ST	Yes	Capture Inputs 1 through 4.
OCFA	I	ST	Yes	Compare Fault A input (for Compare channels).
OCFB	I	ST	No	Compare Fault B input (for Compare channels).
OC1-OC4	O	—	Yes	Compare Outputs 1 through 4.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
RA0-RA4, RA7-RA12	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
RC0-RC13, RC15	I/O	ST	No	PORTC is a bidirectional I/O port.
RD5, RD6, RD8	I/O	ST	No	PORTD is a bidirectional I/O port.
RE12-RE15	I/O	ST	No	PORTE is a bidirectional I/O port.
RF0, RF1	I/O	ST	No	PORTF is a bidirectional I/O port.
RG6-RG9	I/O	ST	No	PORTG is a bidirectional I/O port.
T1CK	I	ST	No	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK	I	ST	No	Timer3 external clock input.
T4CK	I	ST	No	Timer4 external clock input.
T5CK	I	ST	No	Timer5 external clock input.
CTPLS	O	ST	No	CTMU pulse output.
CTED1	I	ST	No	CTMU External Edge Input 1.
CTED2	I	ST	No	CTMU External Edge Input 2.
U1CTS	I	ST	No	UART1 Clear-To-Send.
U1RTS	O	—	No	UART1 Ready-To-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
BCLK1	O	ST	No	UART1 IrDA <sup>®</sup> baud clock output.

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input      P = Power  
ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
PPS = Peripheral Pin Select      TTL = TTL input buffer

- Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.
- 3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 “High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”** for more information.
- 4:** Not all pins are available in all packages variants. See the **“Pin Diagrams”** section for pin availability.
- 5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 4-12: DATA MEMORY MAP FOR PIC24EP32GP/MC20X/50X DEVICES



**TABLE 4-19: SPI1 AND SPI2 REGISTER MAP**

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	SPIBEC<2:0>			SRMPT	SPIROV	SRXMPT	SISEL<2:0>			SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE<2:0>			PPRE<1:0>		0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	SPIBEC<2:0>			SRMPT	SPIROV	SRXMPT	SISEL<2:0>			SPITBF	SPIRBF	0000
SPI2CON1	0262	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE<2:0>			PPRE<1:0>		0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI2BUF	0268	SPI2 Transmit and Receive Buffer Register																0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## 9.1 CPU Clocking System

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices provides six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

Instruction execution speed or device operating frequency,  $FCY$ , is given by Equation 9-1.

### EQUATION 9-1: DEVICE OPERATING FREQUENCY

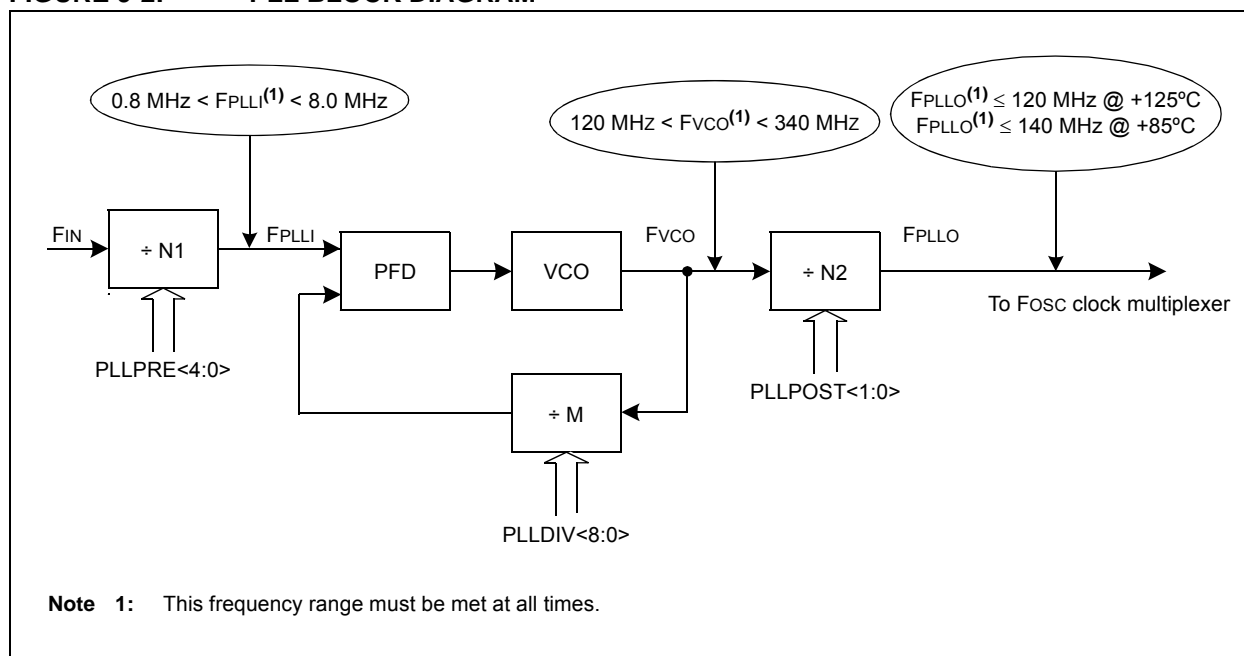
$$FCY = Fosc/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency ( $F_{IN}$ ) and output frequency ( $F_{PLLO}$ ). In clock modes S1 and S3, when the PLL output is selected,  $FOSC = F_{PLLO}$ .

Equation 9-3 provides the relationship between input frequency ( $F_{IN}$ ) and VCO frequency ( $F_{VCO}$ ).

**FIGURE 9-2: PLL BLOCK DIAGRAM**



### EQUATION 9-2: $F_{PLLO}$ CALCULATION

$$F_{PLLO} = F_{IN} \times \left( \frac{M}{N1 \times N2} \right) = F_{IN} \times \left( \frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)} \right)$$

Where:

$$N1 = PLLPRE + 2$$

$$N2 = 2 \times (PLLPOST + 1)$$

$$M = PLLDIV + 2$$

### EQUATION 9-3: $F_{VCO}$ CALCULATION

$$F_{VCO} = F_{IN} \times \left( \frac{M}{N1} \right) = F_{IN} \times \left( \frac{(PLLDIV + 2)}{(PLLPRE + 2)} \right)$$

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	xx	101	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	1
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

**Note 1:** OSC2 pin function is determined by the OSCIOFNC Configuration bit.

**2:** This is the default oscillator mode for an unprogrammed (erased) device.

## 9.2 Oscillator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 9.2.1 KEY RESOURCES

- “**Oscillator**” (DS70580) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

### 9.3 Oscillator Control Registers

**REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER<sup>(1)</sup>**

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC2	COSC1	COSC0	—	NOSC2 <sup>(2)</sup>	NOSC1 <sup>(2)</sup>	NOSC0 <sup>(2)</sup>
bit 15				bit 8			

R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF <sup>(3)</sup>	—	—	OSWEN
bit 7				bit 0			

**Legend:** y = Value set from Configuration bits on POR  
R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15      **Unimplemented:** Read as '0'

bit 14-12      **COSC<2:0>:** Current Oscillator Selection bits (read-only)

111 = Fast RC Oscillator (FRC) with Divide-by-n  
110 = Fast RC Oscillator (FRC) with Divide-by-16  
101 = Low-Power RC Oscillator (LPRC)  
100 = Reserved  
011 = Primary Oscillator (XT, HS, EC) with PLL  
010 = Primary Oscillator (XT, HS, EC)  
001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)  
000 = Fast RC Oscillator (FRC)

bit 11      **Unimplemented:** Read as '0'

bit 10-8      **NOSC<2:0>:** New Oscillator Selection bits<sup>(2)</sup>

111 = Fast RC Oscillator (FRC) with Divide-by-n  
110 = Fast RC Oscillator (FRC) with Divide-by-16  
101 = Low-Power RC Oscillator (LPRC)  
100 = Reserved  
011 = Primary Oscillator (XT, HS, EC) with PLL  
010 = Primary Oscillator (XT, HS, EC)  
001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)  
000 = Fast RC Oscillator (FRC)

bit 7      **CLKLOCK:** Clock Lock Enable bit

1 = If (FCKSM0 = 1), then clock and PLL configurations are locked; if (FCKSM0 = 0), then clock and PLL configurations may be modified  
0 = Clock and PLL selections are not locked, configurations may be modified

bit 6      **IOLOCK:** I/O Lock Enable bit

1 = I/O lock is active  
0 = I/O lock is not active

bit 5      **LOCK:** PLL Lock Status bit (read-only)

1 = Indicates that PLL is in lock or PLL start-up timer is satisfied  
0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

**Note 1:** Writes to this register require an unlock sequence. Refer to “**Oscillator**” (DS70580) in the “dsPIC33/PIC24 Family Reference Manual” (available from the Microchip web site) for details.

**2:** Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

**3:** This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

**NOTES:**



**REGISTER 16-3: PTPER: PWMx PRIMARY MASTER TIME BASE PERIOD REGISTER**

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PTPER<15:8>							
bit 15				bit 8			

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
PTPER<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-0                      **PTPER<15:0>**: Primary Master Time Base (PMTMR) Period Value bits

**REGISTER 16-4: SEVTCMP: PWMx PRIMARY SPECIAL EVENT COMPARE REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-0                      **SEVTCMP<15:0>**: Special Event Compare Count Value bits

**REGISTER 17-4: POS1CNTH: POSITION COUNTER 1 HIGH WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<23:16>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **POSCNT<31:16>**: High Word Used to Form 32-Bit Position Counter Register (POS1CNT) bits

**REGISTER 17-5: POS1CNTL: POSITION COUNTER 1 LOW WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **POSCNT<15:0>**: Low Word Used to Form 32-Bit Position Counter Register (POS1CNT) bits

**REGISTER 17-6: POS1HLD: POSITION COUNTER 1 HOLD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **POSHLD<15:0>**: Hold Register for Reading and Writing POS1CNTH bits

**REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER**

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15						bit 8	

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7						bit 0	

<b>Legend:</b>	C = Clearable bit	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15     **ACKSTAT:** Acknowledge Status bit (when operating as I<sup>2</sup>C™ master, applicable to master transmit operation)  
1 = NACK received from slave  
0 = ACK received from slave  
Hardware is set or clear at the end of slave Acknowledge.
- bit 14     **TRSTAT:** Transmit Status bit (when operating as I<sup>2</sup>C master, applicable to master transmit operation)  
1 = Master transmit is in progress (8 bits + ACK)  
0 = Master transmit is not in progress  
Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
- bit 13-11     **Unimplemented:** Read as '0'
- bit 10     **BCL:** Master Bus Collision Detect bit  
1 = A bus collision has been detected during a master operation  
0 = No bus collision detected  
Hardware is set at detection of a bus collision.
- bit 9     **GCSTAT:** General Call Status bit  
1 = General call address was received  
0 = General call address was not received  
Hardware is set when address matches general call address. Hardware is clear at Stop detection.
- bit 8     **ADD10:** 10-Bit Address Status bit  
1 = 10-bit address was matched  
0 = 10-bit address was not matched  
Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
- bit 7     **IWCOL:** I2Cx Write Collision Detect bit  
1 = An attempt to write to the I2CxTRN register failed because the I<sup>2</sup>C module is busy  
0 = No collision  
Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
- bit 6     **I2COV:** I2Cx Receive Overflow Flag bit  
1 = A byte was received while the I2CxRCV register was still holding the previous byte  
0 = No overflow  
Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
- bit 5     **D\_A:** Data/Address bit (when operating as I<sup>2</sup>C slave)  
1 = Indicates that the last byte received was data  
0 = Indicates that the last byte received was a device address  
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
- bit 4     **P:** Stop bit  
1 = Indicates that a Stop bit has been detected last  
0 = Stop bit was not detected last  
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

**REGISTER 21-3: CxVEC: ECANx INTERRUPT CODE REGISTER**

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0
bit 15							bit 8

U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
—	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bits

10000-11111 = Reserved

01111 = Filter 15

•  
•  
•

00001 = Filter 1

00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits

1000101-1111111 = Reserved

1000100 = FIFO almost full interrupt

1000011 = Receiver overflow interrupt

1000010 = Wake-up interrupt

1000001 = Error interrupt

1000000 = No interrupt

•  
•  
•

0010000-0111111 = Reserved

0001111 = RB15 buffer interrupt

•  
•  
•

0001001 = RB9 buffer interrupt

0001000 = RB8 buffer interrupt

0000111 = TRB7 buffer interrupt

0000110 = TRB6 buffer interrupt

0000101 = TRB5 buffer interrupt

0000100 = TRB4 buffer interrupt

0000011 = TRB3 buffer interrupt

0000010 = TRB2 buffer interrupt

0000001 = TRB1 buffer interrupt

0000000 = TRB0 buffer interrupt

## 22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Charge Time Measurement Unit (CTMU)**” (DS70661) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available on the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Charge Time Measurement Unit is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Four Edge Input Trigger Sources
- Polarity Control for Each Edge Source
- Control of Edge Sequence
- Control of Response to Edges
- Precise Time Measurement Resolution of 1 ns
- Accurate Current Source Suitable for Capacitive Measurement
- On-Chip Temperature Measurement using a Built-in Diode

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

**REGISTER 23-4: AD1CON4: ADC1 CONTROL REGISTER 4**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	ADDMAEN
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	DMABL2	DMABL1	DMABL0
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-9

**Unimplemented:** Read as '0'

bit 8

**ADDMAEN:** ADC1 DMA Enable bit

1 = Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA

0 = Conversion results are stored in ADC1BUF0 through ADC1BUFF registers; DMA will not be used

bit 7-3

**Unimplemented:** Read as '0'

bit 2-0

**DMABL<2:0>:** Selects Number of DMA Buffer Locations per Analog Input bits

111 = Allocates 128 words of buffer to each analog input

110 = Allocates 64 words of buffer to each analog input

101 = Allocates 32 words of buffer to each analog input

100 = Allocates 16 words of buffer to each analog input

011 = Allocates 8 words of buffer to each analog input

010 = Allocates 4 words of buffer to each analog input

001 = Allocates 2 words of buffer to each analog input

000 = Allocates 1 word of buffer to each analog input

**REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)**

- bit 1-0      **PTGITM<1:0>**: PTG Input Trigger Command Operating Mode bits<sup>(1)</sup>
- 11 = Single level detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
  - 10 = Single level detect with Step delay executed on exit of command
  - 01 = Continuous edge detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
  - 00 = Continuous edge detect with Step delay executed on exit of command

- Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.
- 2:** This bit is only used with the PTGCTRL step command software trigger option.
- 3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

## 27.5 Watchdog Timer (WDT)

For dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

### 27.5.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT Time-out period (TWDT), as shown in Parameter SY12 in Table 30-22.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

**Note:** The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

### 27.5.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3,2>) needs to be cleared in software after the device wakes up.

### 27.5.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

### 27.5.4 WDT WINDOW

The Watchdog Timer has an optional Windowed mode, enabled by programming the WINDIS bit in the WDT Configuration register (FWDT<6>). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window select bits (WDTWIN<1:0>).

**FIGURE 27-2: WDT BLOCK DIAGRAM**

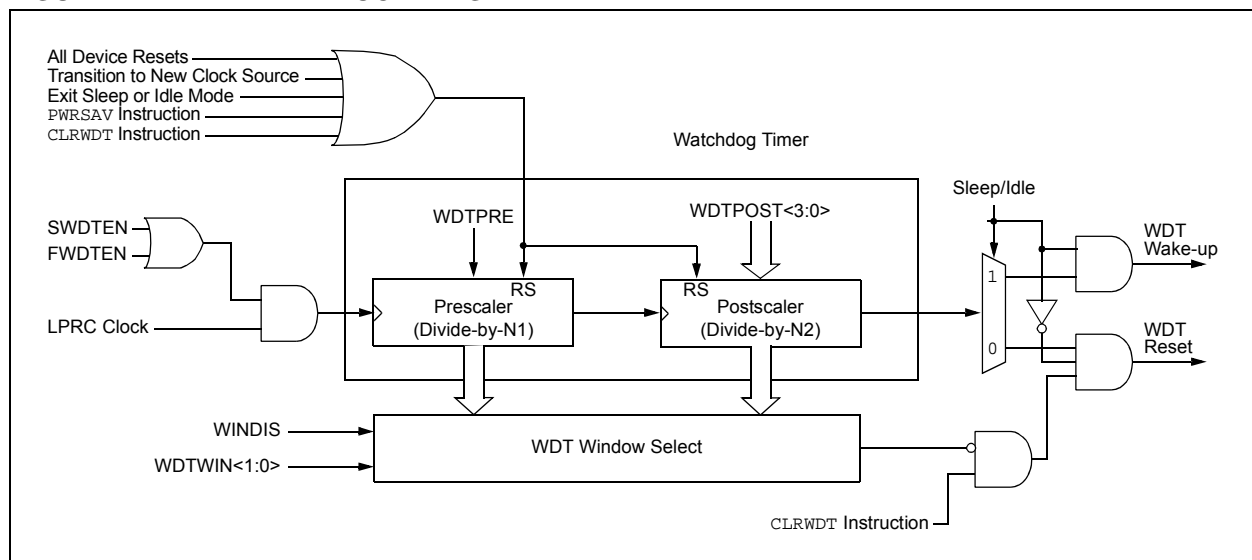




FIGURE 30-34: ECANx MODULE I/O TIMING CHARACTERISTICS

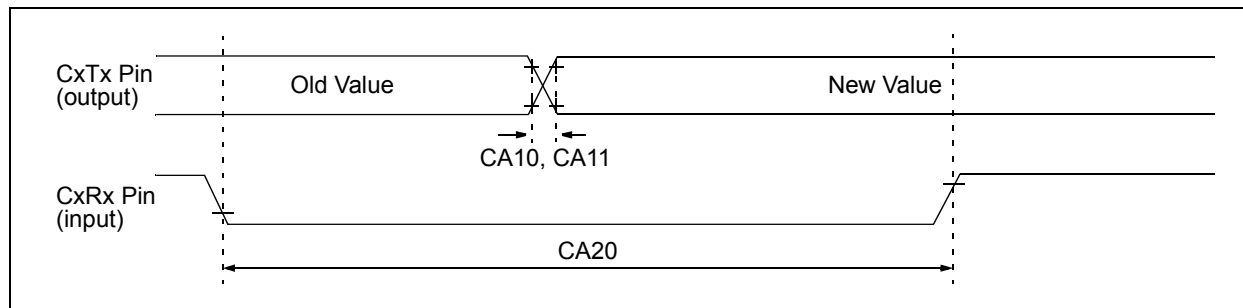


TABLE 30-51: ECANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
CA10	TioF	Port Output Fall Time	—	—	—	ns	See Parameter DO32
CA11	TioR	Port Output Rise Time	—	—	—	ns	See Parameter DO31
CA20	TcWF	Pulse Width to Trigger CAN Wake-up Filter	120	—	—	ns	

**Note 1:** These parameters are characterized but not tested in manufacturing.

**Note 2:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 30-35: UARTx MODULE I/O TIMING CHARACTERISTICS

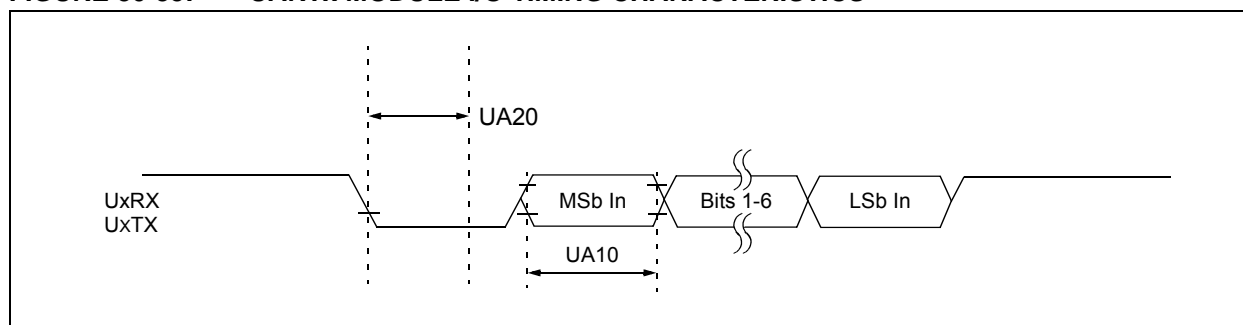


TABLE 30-52: UARTx MODULE I/O TIMING REQUIREMENTS

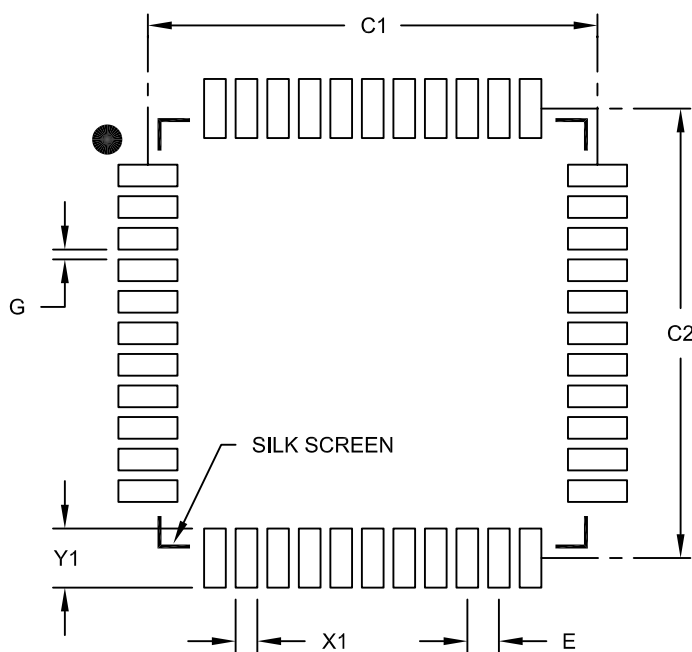
AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
UA10	TUABAUd	UARTx Baud Time	66.67	—	—	ns	
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps	
UA20	TcWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	—	—	ns	

**Note 1:** These parameters are characterized but not tested in manufacturing.

**Note 2:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

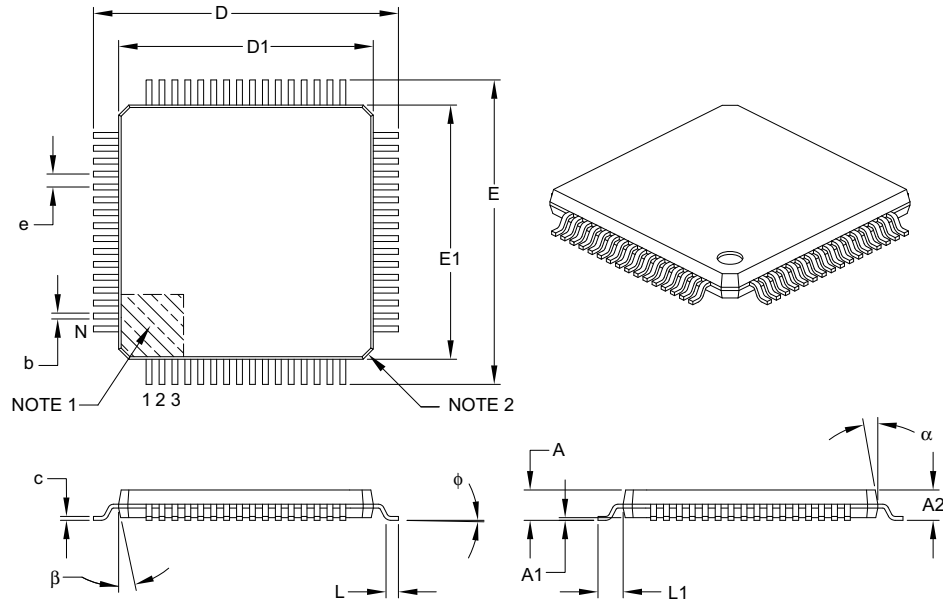
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

**64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm Footprint [TQFP]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Leads	N		64		
Lead Pitch	e		0.50 BSC		
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.95	1.00	1.05
Standoff	A1		0.05	–	0.15
Foot Length	L		0.45	0.60	0.75
Footprint	L1		1.00 REF		
Foot Angle	φ		0°	3.5°	7°
Overall Width	E		12.00 BSC		
Overall Length	D		12.00 BSC		
Molded Package Width	E1		10.00 BSC		
Molded Package Length	D1		10.00 BSC		
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.17	0.22	0.27
Mold Draft Angle Top	α		11°	12°	13°
Mold Draft Angle Bottom	β		11°	12°	13°

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B

## Revision F (November 2012)

Removed “Preliminary” from data sheet footer.

## Revision G (March 2013)

This revision includes the following global changes:

- changes “ $\overline{\text{FLT}}\text{x}$ ” pin function to “FLT<sub>x</sub>” on all occurrences
- adds **Section 31.0 “High-Temperature Electrical Characteristics”** for high-temperature (+150°C) data

This revision also includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-5.

**TABLE A-5: MAJOR SECTION UPDATES**

Section Name	Update Description
<b>Cover Section</b>	<ul style="list-style-type: none"> <li>• Changes internal oscillator specification to 1.0%</li> <li>• Changes I/O sink/source values to 12 mA or 6 mA</li> <li>• Corrects 44-pin VTLA pin diagram (pin 32 now shows as 5V tolerant)</li> </ul>
<b>Section 4.0 “Memory Organization”</b>	<ul style="list-style-type: none"> <li>• Deletes references to Configuration Shadow registers</li> <li>• Corrects the spelling of the JTAGIP and PTGWDTIP bits throughout</li> <li>• Corrects the Reset value of all IOCON registers as C000h</li> <li>• Adds footnote to Table 4-42 to indicate the absence of Comparator 3 in 28-pin devices</li> </ul>
<b>Section 6.0 “Resets”</b>	<ul style="list-style-type: none"> <li>• Removes references to cold and warm Resets, and clarifies the initial configuration of the device clock source on all Resets</li> </ul>
<b>Section 7.0 “Interrupt Controller”</b>	<ul style="list-style-type: none"> <li>• Corrects the definition of GIE as “Global Interrupt Enable” (not “General”)</li> </ul>
<b>Section 9.0 “Oscillator Configuration”</b>	<ul style="list-style-type: none"> <li>• Clarifies the behavior of the CF bit when cleared in software</li> <li>• Removes POR behavior footnotes from all control registers</li> <li>• Corrects the tuning range of the TUN&lt;5:0&gt; bits in Register 9-4 to an overall range <math>\pm 1.5\%</math></li> </ul>
<b>Section 13.0 “Timer2/3 and Timer4/5”</b>	<ul style="list-style-type: none"> <li>• Clarifies the presence of the ADC Trigger in 16-bit Timer3 and Timer5, as well as the 32-bit timers</li> </ul>
<b>Section 15.0 “Output Compare”</b>	<ul style="list-style-type: none"> <li>• Corrects the first trigger source for SYNCSEL&lt;4:0&gt; (OCxCON2&lt;4:0&gt;) as OCxRS match</li> </ul>
<b>Section 16.0 “High-Speed PWM Module”</b>	<ul style="list-style-type: none"> <li>• Clarifies the source of the PWM interrupts in Figure 16-1</li> <li>• Corrects the Reset states of IOCONx&lt;15:14&gt; in Register 16-13 as ‘11’</li> </ul>
<b>Section 17.0 “Quadrature Encoder Interface (QEI) Module”</b>	<ul style="list-style-type: none"> <li>• Clarifies the operation of the IMV&lt;1:0&gt; bits (QEICON&lt;9:8&gt;) with updated text and additional notes</li> <li>• Corrects the first prescaler value for QFVDIV&lt;2:0&gt; (QE1IOC&lt;13:11&gt;), now 1:128</li> </ul>
<b>Section 23.0 “10-Bit/12-Bit Analog-to-Digital Converter (ADC)”</b>	<ul style="list-style-type: none"> <li>• Adds note to Figure 23-1 that Op Amp 3 is not available in 28-pin devices</li> <li>• Changes “sample clock” to “sample trigger” in AD1CON1 (Register 23-1)</li> <li>• Clarifies footnotes on op amp usage in Registers 23-5 and 23-6</li> </ul>
<b>Section 25.0 “Op Amp/Comparator Module”</b>	<ul style="list-style-type: none"> <li>• Adds Note text to indicate that Comparator 3 is unavailable in 28-pin devices</li> <li>• Splits Figure 25-1 into two figures for clearer presentation (Figure 25-1 for Op amp/Comparators 1 through 3, Figure 25-2 for Comparator 4). Subsequent figures are renumbered accordingly.</li> <li>• Corrects reference description in xxxxx (now (AVDD+AVSS)/2)</li> <li>• Changes CMSTAT&lt;15&gt; in Register 25-1 to “PSIDL”</li> </ul>
<b>Section 27.0 “Special Features”</b>	<ul style="list-style-type: none"> <li>• Corrects the addresses of all Configuration bytes for 512 Kbyte devices</li> </ul>

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