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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

-·XE

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mc506-i-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1 (General Purpose Families) and Table 2 (Motor Control Families). Their pinout diagrams appear on the following pages.

	s)	es)			Rei	mappa	ble Pe	eriphe	rals				~																					
Device	Page Erase Size (Instruction:	Program Flash Memory (Kbyt	RAM (Kbyte)	16-Bit/32-Bit Timers	Input Capture	Output Compare	UART	SPI ⁽²⁾	ECAN™ Technology	External Interrupts ⁽³⁾	I²C™	CRC Generator	10-Bit/12-Bit ADC (Channels	Op Amps/Comparators	CTMU	РТС	I/O Pins	Pins	Packages															
PIC24EP32GP202	512	32	4																															
PIC24EP64GP202	1024	64	8																SPDIP,															
PIC24EP128GP202	1024	128	16	5	4	4	2	2		3	2	1	6	2/3(1)	Yes	Yes	21	28	SOIC,															
PIC24EP256GP202	1024	256	32																OFN-S															
PIC24EP512GP202	1024	512	48																Q. 11 0															
PIC24EP32GP203	512	32	4																															
PIC24EP64GP203	1024	64	8	5	4	4	2	2	—	3	2	1	8	3/4	Yes	Yes	25	36	VTLA															
PIC24EP32GP204	512	32	4																															
PIC24EP64GP204	1024	64	8										9	3/4	Yes				VTLA ⁽⁴⁾ ,															
PIC24EP128GP204	1024	128	16	5	4	4	2	2	_	3	2	1				Yes	35	44/	TQFP,															
PIC24EP256GP204	1024	256	32										-					48	QEN, UOEN															
PIC24EP512GP204	1024	512	48	_															OQIN															
PIC24EP64GP206	1024	64	8																															
PIC24EP128GP206	1024	128	16		4												53	64	TQFP, QFN															
PIC24EP256GP206	1024	256	32	5		4	2	2	—	3	2	1	16	3/4	Yes	Yes																		
PIC24EP512GP206	1024	512	48																															
dsPIC33EP32GP502	512	32	4																															
dsPIC33EP64GP502	1024	64	8				2												SPDIP,															
dsPIC33EP128GP502	1024	128	16	5	4	4		2	1	3	2	1	6	2/3 (1)	Yes	Yes	21	28	SOIC,															
dsPIC33EP256GP502	1024	256	32										Ŭ						OFN-S															
dsPIC33EP512GP502	1024	512	48																Q. 11 0															
dsPIC33EP32GP503	512	32	4				_	_			_		_																					
dsPIC33EP64GP503	1024	64	8	5	4	4	2	2	1	3	2	1	8	3/4	Yes	Yes	25	36	VTLA															
dsPIC33EP32GP504	512	32	4																															
dsPIC33EP64GP504	1024	64	8																VTLA ⁽⁴⁾ ,															
dsPIC33EP128GP504	1024	128	16	5	4	4	2	2	1	3	2	1	9	3/4	Yes	Yes	35	44/	TQFP,															
dsPIC33EP256GP504	1024	256	32	1														48	UQFN,															
dsPIC33EP512GP504	1024	512	48	1																														
dsPIC33EP64GP506	1024	64	8			Ì						Ì		1				Ì																
dsPIC33EP128GP506	1024	128	16			4		2	2	2	2	2	2	2	2	2	2	2	2	2											TQFP.			
dsPIC33EP256GP506	1024	256	32	5	4		2														2	2	2	2	2	2	2	2	2	2	2	2	2	2
dsPIC33EP512GP506	1024	512	48	1																														

TABLE 1: dsPIC33EPXXXGP50X and PIC24EPXXXGP20X GENERAL PURPOSE FAMILIES

Note 1: On 28-pin devices, Comparator 4 does not have external connections. Refer to Section 25.0 "Op Amp/Comparator Module" for details.

Only SPI2 is remappable.
 INT0 is not remappable.

4: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

Pin Diagrams (Continued)





2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μ F to 47 μ F.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohm) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor greater than 4.7 μ F (10 μ F is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 30.0** "**Electrical Characteristics**" for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 27.3 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

- Device Reset
- Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.







FIGURE 4-9: DATA MEMORY MAP FOR dsPIC33EP128MC20X/50X AND dsPIC33EP128GP50X DEVICES

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL		0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	_		_	_	_	_	_	_	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	_	_	_	_	_		_	_	_	_	DAE	DOOVR	_	_	_	_	0000
INTCON4	08C6					_	_			_				_	—		SGHT	0000
INTTREG	08C8						ILR<	3:0>					VECNU	M<7:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0	
OA	OB	SA	SB	OAB	SAB	DA	DC	
bit 15							bit 8	
R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0	
	IPL<2:0> ⁽²⁾		RA	Ν	OV	Z	С	
bit 7						-	bit 0	
								1

REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

Legend:	C = Clearable bit		-
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits ^(2,3)
	111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
	110 = CPU Interrupt Priority Level is 6 (14)
	101 = CPU Interrupt Priority Level is 5 (13)
	100 = CPU Interrupt Priority Level is 4 (12)
	011 = CPU Interrupt Priority Level is 3 (11)
	010 = CPU Interrupt Priority Level is 2 (10)
	001 = CPU Interrupt Priority Level is 1 (9)
	000 = CPU Interrupt Priority Level is 0 (8)

- **Note 1:** For complete register details, see Register 3-1.
 - 2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 - **3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

NOTES:

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				IC4R<6:0>			
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				IC3R<6:0>			
bit 7							bit 0
Legend:							
R = Readable bit		W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown
bit 15	Unimpleme	ented: Read as '	0'				
bit 14-8	IC4R<6:0>: (see Table 2	Assign Input Ca	pture 4 (IC4) selection nu) to the Correspo mbers)	onding RPn P	in bits	
	1111001 =	Input tied to RPI	121				
	•						
	•						
	0000001 =	Input tied to CM	P1				
bit 7		nput tied to vss	, 0,				
bit 6-0		Assign Input Ca	o unture 3 (IC3)) to the Correspo	ondina RPn P	in hits	
bit 0 0	(see Table 1	11-2 for input pin	selection nu	mbers)		in bits	
	1111001 =	Input tied to RPI	121	,			
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss	5				

REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture Stop in Idle Control bit
	1 = Input capture will Halt in CPU Idle mode
	0 = Input capture will continue to operate in CPU Idle mode
bit 12-10	ICTSEL<2:0>: Input Capture Timer Select bits
	111 = Peripheral clock (FP) is the clock source of the ICx
	110 = Reserved
	101 = Reserved
	100 - 11 CLR is the clock source of the ICx (only the synchronous clock is supported) 011 = T5CLK is the clock source of the ICx
	010 = T4CLK is the clock source of the ICx
	001 = T2CLK is the clock source of the ICx
	000 = T3CLK is the clock source of the ICx
bit 9-7	Unimplemented: Read as '0'
bit 6-5	ICI<1:0>: Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	01 = Interrupt on every second capture event
hit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
Dit 4	1 = Input capture buffer overflow occurred
	0 = No input capture buffer overflow occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	1 = Input capture buffer is not empty, at least one more capture value can be read
	0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture Mode Select bits
	111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
	110 = Unused (module is disabled)
	101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
	100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
	011 = Capture mode, every falling edge (Simple Capture mode)
	001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
	000 = Input capture module is turned off



FIGURE 16-2: HIGH-SPEED PWMx MODULE REGISTER INTERCONNECTION DIAGRAM

16.2 PWM Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

16.2.1 KEY RESOURCES

- "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0		
—	—	—	_		LEB<11:8>				
bit 15							bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
			LEE	3<7:0>					
bit 7							bit 0		
Legend:									
R = Readable bit W = Writa			bit	U = Unimplemented bit, read as '0'					
-n = Value at POR		'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown			

REGISTER 16-17: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER

bit 15-12 Unimplemented: Read as '0'

bit 11-0 LEB<11:0>: Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits

REGISTER 18-1: SPIx STAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 1 SPITBF: SPIx Transmit Buffer Full Status bit
 - 1 = Transmit not yet started, SPIxTXB is full
 - 0 = Transmit started, SPIxTXB is empty

Standard Buffer mode:

Automatically set in hardware when core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer mode:

Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 SPIRBF: SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full

0 = Receive is incomplete, SPIxRXB is empty

Standard Buffer mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0		
DMABS2	DMABS1	DMABS0	—	_	_	_	—		
bit 15 bit 8									
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—	—	—	FSA4	FSA3	FSA2	FSA1	FSA0		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable I	bit	U = Unimple	mented bit, read	d as '0'			
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unknown			
bit 15-13 DMABS<2:0>: DMA Buffer Size bits 111 = Reserved 110 = 32 buffers in RAM 101 = 24 buffers in RAM 100 = 16 buffers in RAM 011 = 12 buffers in RAM 010 = 8 buffers in RAM 001 = 6 buffers in RAM 000 = 4 buffers in RAM 000 = 4 buffers in RAM bit 12-5 Unimplemented: Read as '0' FSA<4:0>: FIFO Area Starts with Buffer bits 11111 = Read Buffer RB31 11110 = Read Buffer RB30 00001 = TX/RX Buffer TRB1 00000 = TX/RX Buffer TRB1				its					

REGISTER 21-4: CxFCTRL: ECANx FIFO CONTROL REGISTER

REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER^(1,2) (CONTINUED)

bit 4	OC1CS: Clock Source for OC1 bit
	 1 = Generates clock pulse when the broadcast command is executed 0 = Does not generate clock pulse when the broadcast command is executed
bit 3	OC4TSS: Trigger/Synchronization Source for OC4 bit
	 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
bit 2	OC3TSS: Trigger/Synchronization Source for OC3 bit
	 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
bit 1	OC2TSS: Trigger/Synchronization Source for OC2 bit
	 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
bit 0	OC1TSS: Trigger/Synchronization Source for OC1 bit
	 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed

- **Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).
 - 2: This register is only used with the PTGCTRL OPTION = 1111 Step command.





FIGURE 30-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)



TABLE 30-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			Standa (unless Operati	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions		
MP10	TFPWM	PWMx Output Fall Time	—			ns	See Parameter DO32		
MP11	TRPWM	PWMx Output Rise Time	_	_		ns	See Parameter DO31		
MP20	TFD	Fault Input ↓ to PWMx I/O Change	_	_	15	ns			
MP30	Tfh	Fault Input Pulse Width	15	_		ns			

Note 1: These parameters are characterized but not tested in manufacturing.



FIGURE 30-13: QEI MODULE INDEX PULSE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

TABLE 30-32: QEI INDEX PULSE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	am o. Symbol Characteristic ⁽¹⁾		Min.	Min. Max.		Conditions	
TQ50	TqiL	Filter Time to Recognize Low, with Digital Filter	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)	
TQ51	TqiH	Filter Time to Recognize High, with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)	
TQ55	Tqidxr	Index Pulse Recognized to Position Counter Reset (ungated index)	3 TCY	—	ns		

Note 1: These parameters are characterized but not tested in manufacturing.

2: Alignment of index pulses to QEA and QEB is shown for position counter Reset timing only. Shown for forward direction only (QEA leads QEB). Same timing applies for reverse direction (QEA lags QEB) but index pulse recognition occurs on the falling edge.

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)}^{(1)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$								
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions				
	Clock Parameters										
AD50	TAD	ADC Clock Period	117.6	_	_	ns					
AD51	tRC	ADC Internal RC Oscillator Period ⁽²⁾	—	250		ns					
	Conversion Rate										
AD55	tCONV	Conversion Time	_	14 Tad		ns					
AD56	FCNV	Throughput Rate			500	ksps					
AD57a	TSAMP	Sample Time when Sampling any ANx Input	3 Tad	_	—	_					
AD57b	TSAMP	Sample Time when Sampling the Op Amp Outputs (Configuration A and Configuration B) ^(4,5)	3 Tad	—	_						
		Timin	g Parame	ters							
AD60	tPCS	Conversion Start from Sample Trigger ^(2,3)	2 Tad		3 Tad	_	Auto-convert trigger is not selected				
AD61	tpss	Sample Start from Setting Sample (SAMP) bit ^(2,3)	2 Tad	—	3 Tad	_					
AD62	tcss	Conversion Completion to Sample Start (ASAM = 1) ^(2,3)	_	0.5 TAD	1	_					
AD63	tdpu	Time to Stabilize Analog Stage from ADC Off to ADC On ^(2,3)	_		20	μs	(Note 6)				

TABLE 30-60: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: Parameters are characterized but not tested in manufacturing.
- **3:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.
- 4: See Figure 25-6 for configuration information.
- 5: See Figure 25-7 for configuration information.
- **6:** The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1<15>) = 1). During this time, the ADC result is indeterminate.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- · Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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