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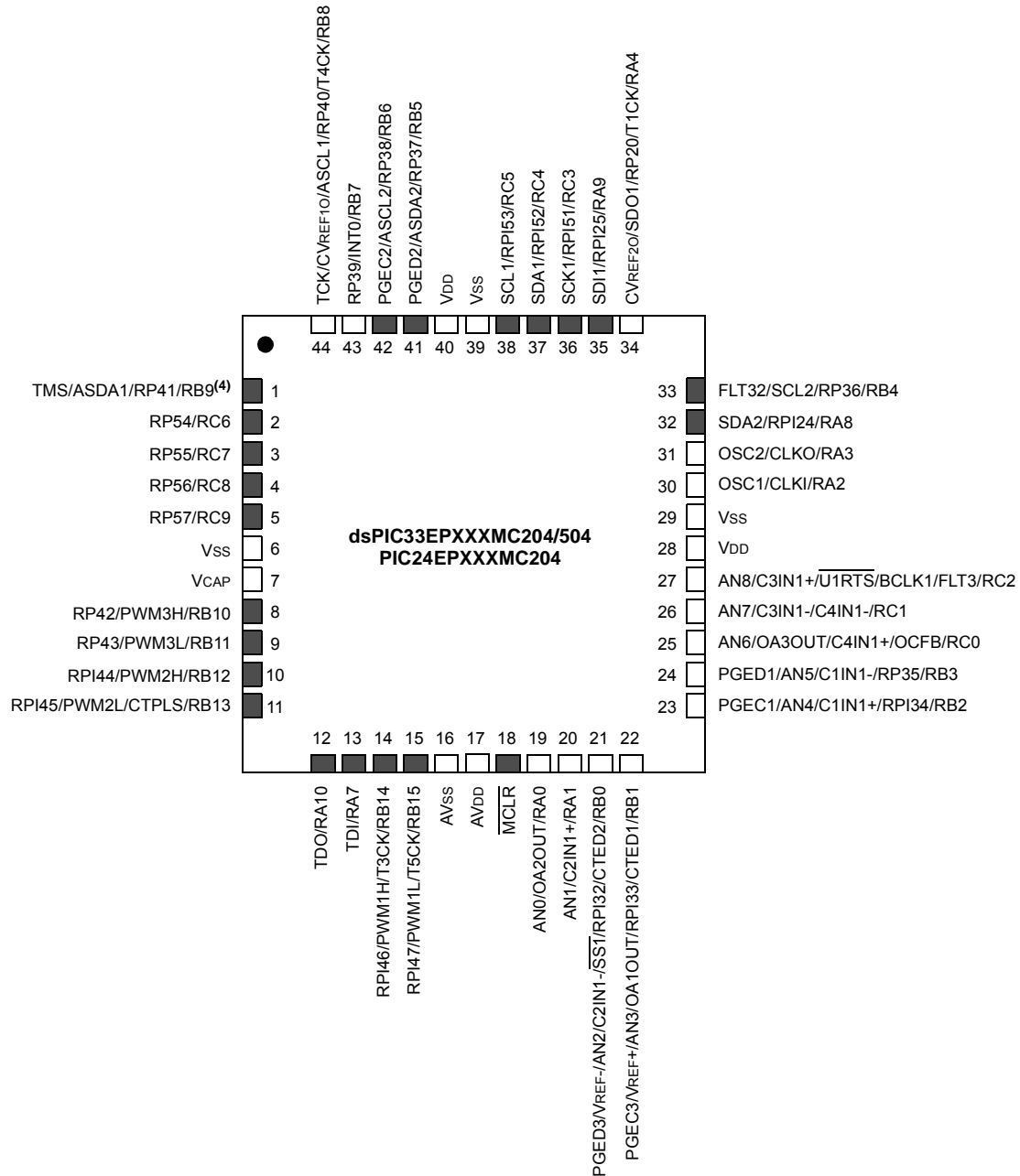
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mc506-i-pt

Pin Diagrams (Continued)

44-Pin QFN[1,2,3]

■ = Pins are up to 5V tolerant

Top pins (44–34):
- 44: TCK/CV$_{REF1O}$/ASCL1/RP40/T4CK/RB8
- 43: RP39/INT0/RB7
- 42: PGEC2/ASCL2/RP38/RB6
- 41: PGED2/ASDA2/RP37/RB5
- 40: V$_{DD}$
- 39: V$_{SS}$
- 38: SCL1/RPI53/RC5
- 37: SDA1/RPI52/RC4
- 36: SCK1/RPI51/RC3
- 35: SDI1/RPI25/RA9
- 34: CV$_{REF2O}$/SDO1/RP20/T1CK/RA4

Left pins (1–11):
- 1: TMS/ASDA1/RP41/RB9[4]
- 2: RP54/RC6
- 3: RP55/RC7
- 4: RP56/RC8
- 5: RP57/RC9
- 6: V$_{SS}$
- 7: V$_{CAP}$
- 8: RP42/PWM3H/RB10
- 9: RP43/PWM3L/RB11
- 10: RPI44/PWM2H/RB12
- 11: RPI45/PWM2L/CTPLS/RB13

Center label:
**dsPIC33EPXXXMC204/504
PIC24EPXXXMC204**

Right pins (33–23):
- 33: FLT32/SCL2/RP36/RB4
- 32: SDA2/RPI24/RA8
- 31: OSC2/CLKO/RA3
- 30: OSC1/CLKI/RA2
- 29: V$_{SS}$
- 28: V$_{DD}$
- 27: AN8/C3IN1+/U1RTS/BCLK1/FLT3/RC2
- 26: AN7/C3IN1-/C4IN1-/RC1
- 25: AN6/OA3OUT/C4IN1+/OCFB/RC0
- 24: PGED1/AN5/C1IN1-/RP35/RB3
- 23: PGEC1/AN4/C1IN1+/RPI34/RB2

Bottom pins (12–22):
- 12: TDO/RA10
- 13: TDI/RA7
- 14: RPI46/PWM1H/T3CK/RB14
- 15: RPI47/PWM1L/T5CK/RB15
- 16: AV$_{SS}$
- 17: AV$_{DD}$
- 18: $\overline{MCLR}$
- 19: AN0/OA2OUT/RA0
- 20: AN1/C2IN1+/RA1
- 21: PGED3/V$_{REF}$-/AN2/C2IN1-/$\overline{SS1}$/RPI32/CTED2/RB0
- 22: PGEC3/V$_{REF}$+/AN3/OA1OUT/RPI33/CTED1/RB1

**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to V$_{SS}$ externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

REGISTER 3-2:   CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2   **SFA:** Stack Frame Active Status bit

      1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values

      0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1   **RND:** Rounding Mode Select bit[1]

      1 = Biased (conventional) rounding is enabled

      0 = Unbiased (convergent) rounding is enabled

bit 0   **IF:** Integer or Fractional Multiplier Mode Select bit[1]

      1 = Integer mode is enabled for DSP multiply

      0 = Fractional mode is enabled for DSP multiply

Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

    2: This bit is always read as '0'.

    3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

FIGURE 4-5: **PROGRAM MEMORY MAP FOR dsPIC33EP512GP50X, dsPIC33EP512MC20X/50X AND PIC24EP512GP/MC20X DEVICES**

Note: Memory areas are not shown to scale.
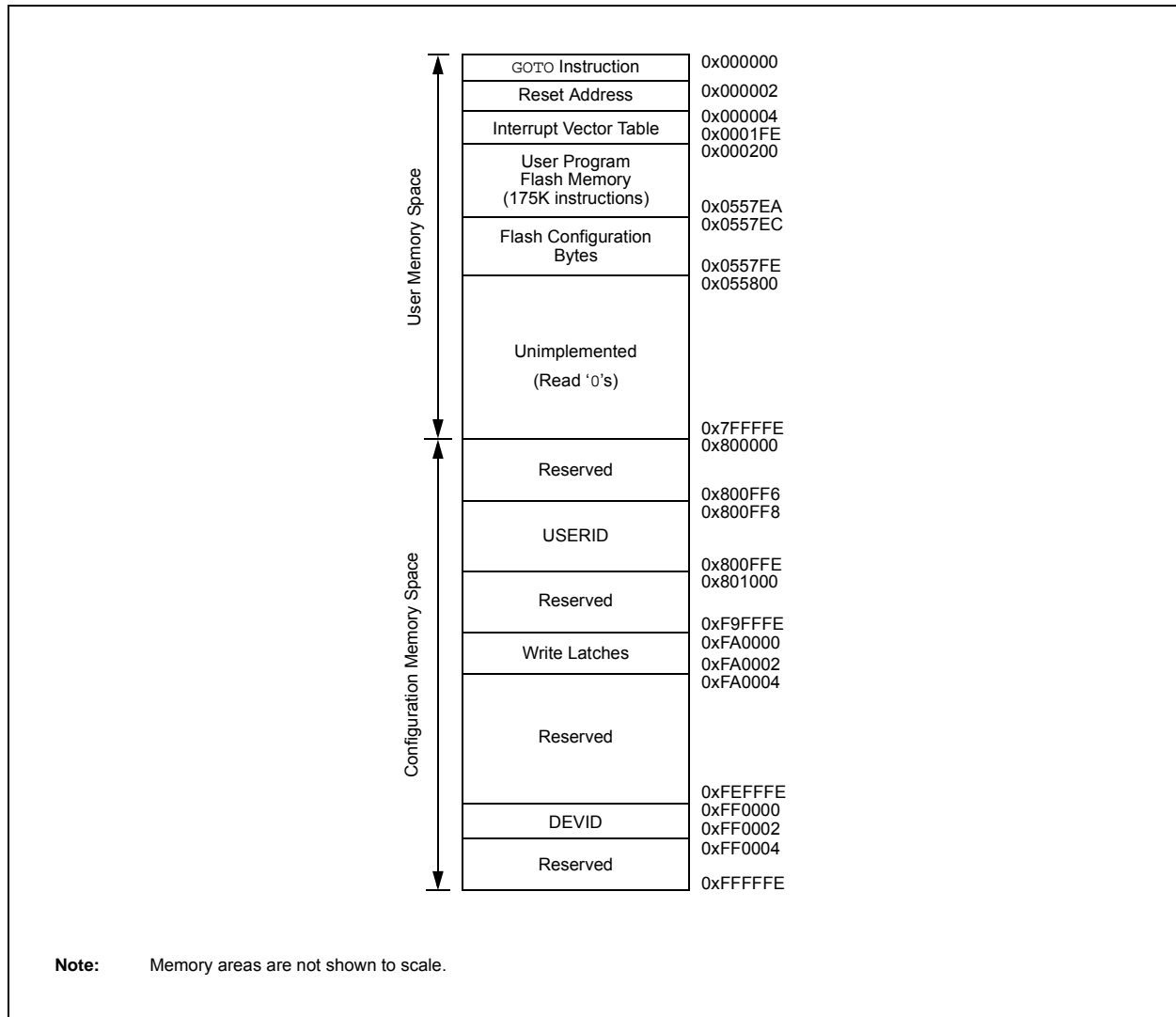
4.4 Special Function Register Maps

TABLE 4-1:   CPU CORE REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000	W0 (WREG)																xxxx
W1	0002	W1																xxxx
W2	0004	W2																xxxx
W3	0006	W3																xxxx
W4	0008	W4																xxxx
W5	000A	W5																xxxx
W6	000C	W6																xxxx
W7	000E	W7																xxxx
W8	0010	W8																xxxx
W9	0012	W9																xxxx
W10	0014	W10																xxxx
W11	0016	W11																xxxx
W12	0018	W12																xxxx
W13	001A	W13																xxxx
W14	001C	W14																xxxx
W15	001E	W15																xxxx
SPLIM	0020	SPLIM																0000
ACCAL	0022	ACCAL																0000
ACCAH	0024	ACCAH																0000
ACCAU	0026	Sign Extension of ACCA<39>								ACCAU								0000
ACCBL	0028	ACCBL																0000
ACCBH	002A	ACCBH																0000
ACCBU	002C	Sign Extension of ACCB<39>								ACCBU								0000
PCL	002E	PCL<15:0>															—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH<6:0>							0000
DSRPAG	0032	—	—	—	—	—	—	DSRPAG<9:0>										0001
DSWPAG	0034	—	—	—	—	—	—	—	DSWPAG<8:0>									0001
RCOUNT	0036	RCOUNT<15:0>																0000
DCOUNT	0038	DCOUNT<15:0>																0000
DOSTARTL	003A	DOSTARTL<15:1>															—	0000
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>						0000
DOENDL	003E	DOENDL<15:1>															—	0000
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	DOENDH<5:0>						0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

TABLE 4-27: **PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC204/504 AND PIC24EPXXXGP/MC204 DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—			RP35R<5:0>				—	—			RP20R<5:0>				0000
RPOR1	0682	—	—			RP37R<5:0>				—	—			RP36R<5:0>				0000
RPOR2	0684	—	—			RP39R<5:0>				—	—			RP38R<5:0>				0000
RPOR3	0686	—	—			RP41R<5:0>				—	—			RP40R<5:0>				0000
RPOR4	0688	—	—			RP43R<5:0>				—	—			RP42R<5:0>				0000
RPOR5	068A	—	—			RP55R<5:0>				—	—			RP54R<5:0>				0000
RPOR6	068C	—	—			RP57R<5:0>				—	—			RP56R<5:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-28: **PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC206/506 AND PIC24EPXXXGP/MC206 DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—			RP35R<5:0>				—	—			RP20R<5:0>				0000
RPOR1	0682	—	—			RP37R<5:0>				—	—			RP36R<5:0>				0000
RPOR2	0684	—	—			RP39R<5:0>				—	—			RP38R<5:0>				0000
RPOR3	0686	—	—			RP41R<5:0>				—	—			RP40R<5:0>				0000
RPOR4	0688	—	—			RP43R<5:0>				—	—			RP42R<5:0>				0000
RPOR5	068A	—	—			RP55R<5:0>				—	—			RP54R<5:0>				0000
RPOR6	068C	—	—			RP57R<5:0>				—	—			RP56R<5:0>				0000
RPOR7	068E	—	—			RP97R<5:0>				—	—	—	—	—	—	—	—	0000
RPOR8	0690	—	—			RP118R<5:0>				—	—	—	—	—	—	—	—	0000
RPOR9	0692	—	—	—	—	—	—	—	—	—	—			RP120R<5:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-49: PORTD REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E30	—	—	—	—	—	—	—	TRISD8	—	TRISD6	TRISD5	—	—	—	—	—	0160
PORTD	0E32	—	—	—	—	—	—	—	RD8	—	RD6	RD5	—	—	—	—	—	xxxx
LATD	0E34	—	—	—	—	—	—	—	LATD8	—	LATD6	LATD5	—	—	—	—	—	xxxx
ODCD	0E36	—	—	—	—	—	—	—	ODCD8	—	ODCD6	ODCD5	—	—	—	—	—	0000
CNEND	0E38	—	—	—	—	—	—	—	CNIED8	—	CNIED6	CNIED5	—	—	—	—	—	0000
CNPUD	0E3A	—	—	—	—	—	—	—	CNPUD8	—	CNPUD6	CNPUD5	—	—	—	—	—	0000
CNPDD	0E3C	—	—	—	—	—	—	—	CNPDD8	—	CNPDD6	CNPDD5	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-50: PORTE REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	0E40	TRISE15	TRISE14	TRISE13	TRISE12	—	—	—	—	—	—	—	—	—	—	—	—	F000
PORTE	0E42	RE15	RE14	RE13	RE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
LATE	0E44	LATE15	LATE14	LATE13	LATE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
ODCE	0E46	ODCE15	ODCE14	ODCE13	ODCE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNENE	0E48	CNIEE15	CNIEE14	CNIEE13	CNIEE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPUE	0E4A	CNPUE15	CNPUE14	CNPUE13	CNPUE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPDE	0E4C	CNPDE15	CNPDE14	CNPDE13	CNPDE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
ANSELE	0E4E	ANSE15	ANSE14	ANSE13	ANSE12	—	—	—	—	—	—	—	—	—	—	—	—	F000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-51: PORTF REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISF1	TRISF0	0003
PORTF	0E52	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RF1	RF0	xxxx
LATF	0E54	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATF1	LATF0	xxxx
ODCF	0E56	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCF1	ODCF0	0000
CNENF	0E58	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNIEF1	CNIEF0	0000
CNPUF	0E5A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUF1	CNPUF0	0000
CNPDF	0E5C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPDF1	CNPDF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the `MAC` class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the `MUL` instruction), which writes the result to a register or register pair. The `MOV` instruction allows additional flexibility and can access the entire Data Space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

`Operand 3 = Operand 1 <function> Operand 2`

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note:	Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

10.0 POWER-SAVING FEATURES

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Watchdog Timer and Power-Saving Modes"** (DS70615) in the "*dsPIC33/ PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

> **Note:** SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV  #SLEEP_MODE     ; Put the device into Sleep mode
PWRSAV  #IDLE_MODE      ; Put the device into Idle mode
```

11.5   I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 30-11, under "Injection Current", have internal protection diodes to V_{DD} and V_{SS}. The term, "Injection Current", is also referred to as "Clamp Current". On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the V_{SS} and V_{DD} supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device, that is clamped internally by the V_{DD} and V_{SS} power rails, may affect the ADC accuracy by four to six counts.

2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.

> **Note:** Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.

4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(V_{DD} – 0.8), not V_{DD}. This value is still above the minimum V_{IH} of CMOS and TTL devices.

5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the V_{OH}/I_{OH} and V_{OL}/I_{OL} DC characteristic specification. The respective I_{OH} and I_{OL} current rating only applies to maintaining the corresponding output at or above the V_{OH}, and at or below the V_{OL} levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum V_{IH}/V_{IL} levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:

    V_{OH} = 2.4V @ I_{OH} = -8 mA and V_{DD} = 3.3V

    The maximum output current sourced by any 8 mA I/O pin = 12 mA.

    LED source current < 12 mA is technically permitted. Refer to the V_{OH}/I_{OH} graphs in **Section 30.0 "Electrical Characteristics"** for additional information.

6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:

    a) Only one "output" function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).

    b) It is possible to assign a "remappable output" function to multiple pins and externally short or tie them together for increased current drive.

    c) If any "dedicated output" function is enabled on a pin, it will take precedence over any remappable "output" function.

    d) If any "dedicated digital" (input or output) function is enabled on a pin, any number of "input" remappable functions can be mapped to the same pin.

    e) If any "dedicated analog" function(s) are enabled on a given pin, "digital input(s)" of any kind will all be disabled, although a single "digital output", at the user's cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input provided there is no external analog input, such as for a built-in self-test.

    f) Any number of "input" remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable "output".

11.7   Peripheral Pin Select Registers

REGISTER 11-1:   RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT1R<6:0>						
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-8   **INT1R<6:0>:** Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits
                (see Table 11-2 for input pin selection numbers)
                `1111001` = Input tied to RPI121
                .
                .
                .
                `0000001` = Input tied to CMP1
                `0000000` = Input tied to Vss

bit 7-0   **Unimplemented:** Read as '0'

13.0   TIMER2/3 AND TIMER4/5

Note 1:	This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70362) of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
2:	Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

• Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
• Single 32-Bit Timer
• Single 32-Bit Synchronous Counter

They also support these features:

• Timer Gate Operation
• Selectable Prescaler Settings
• Timer Operation during Idle and Sleep modes
• Interrupt on a 32-Bit Period Register Match
• Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
• ADC1 Event Trigger (32-bit timer pairs, and Timer3 and Timer5 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw); Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

Note:	For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note:	Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

REGISTER 17-1:   QEI1CON: QEI1 CONTROL REGISTER (CONTINUED)

bit 6-4   **INTDIV<2:0>:** Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select)[3]

111 = 1:128 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3   **CNTPOL:** Position and Index Counter/Timer Direction Select bit

1 = Counter direction is negative unless modified by external up/down signal
0 = Counter direction is positive unless modified by external up/down signal

bit 2   **GATEN:** External Count Gate Enable bit

1 = External gate signal controls position counter operation
0 = External gate signal does not affect position counter/timer operation

bit 1-0   **CCM<1:0>:** Counter Control Mode Selection bits

11 = Internal Timer mode with optional external count is selected
10 = External clock count with optional external count is selected
01 = External clock count with external up/down direction is selected
00 = Quadrature Encoder Interface (x4 mode) Count mode is selected

Note 1:   When CCM<1:0> = 10 or 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

2:   When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.

3:   The selected clock rate should be at least twice the expected maximum quadrature count rate.

18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
   a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on $\overline{SSx}$.
   b) If FRMPOL = 0, use a pull-up resistor on $\overline{SSx}$.

   > **Note:** This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode, (i.e., not using $\overline{SSx}$ from a master):
   a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on $\overline{SSx}$.
   b) If CKP = 0, always place a pull-down resistor on $\overline{SSx}$.

   > **Note:** This will insure that during power-up and initialization the master/slave will not lose Sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the $\overline{SSx}$ pin, which indicates the start of a data frame.

   > **Note:** Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in **Section 30.0 "Electrical Characteristics"** for details.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPIx data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

18.2.1 KEY RESOURCES

- **"Serial Peripheral Interface (SPI)"** (DS70569) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

BUFFER 21-5: **ECAN™ MESSAGE BUFFER WORD 4**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Byte 3				

bit 15   bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Byte 2				

bit 7   bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   **Byte 3<15:8>:** ECAN Message Byte 3 bits
bit 7-0   **Byte 2<7:0>:** ECAN Message Byte 2 bits

BUFFER 21-6: **ECAN™ MESSAGE BUFFER WORD 5**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Byte 5				

bit 15   bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Byte 4				

bit 7   bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   **Byte 5<15:8>:** ECAN Message Byte 5 bits
bit 7-0   **Byte 4<7:0>:** ECAN Message Byte 4 bits

23.4   ADC Control Registers

REGISTER 23-1:   AD1CON1: ADC1 CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC, HS	R/C-0, HC, HS
SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE[3]
bit 7							bit 0

Legend:			
	HC = Hardware Clearable bit	HS = Hardware Settable bit	C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **ADON:** ADC1 Operating Mode bit
1 = ADC module is operating
0 = ADC is off

bit 14   **Unimplemented:** Read as '0'

bit 13   **ADSIDL:** ADC1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12   **ADDMABM:** DMA Buffer Build Mode bit
1 = DMA buffers are written in the order of conversion; the module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer
0 = DMA buffers are written in Scatter/Gather mode; the module provides a Scatter/Gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer.

bit 11   **Unimplemented:** Read as '0'

bit 10   **AD12B:** ADC1 10-Bit or 12-Bit Operation Mode bit
1 = 12-bit, 1-channel ADC operation
0 = 10-bit, 4-channel ADC operation

bit 9-8   **FORM<1:0>:** Data Output Format bits
For 10-Bit Operation:
11 = Signed fractional (D$_{OUT}$ = sddd dddd dd00 0000, where s = .NOT.d<9>)
10 = Fractional (D$_{OUT}$ = dddd dddd dd00 0000)
01 = Signed integer (D$_{OUT}$ = ssss sssd dddd dddd, where s = .NOT.d<9>)
00 = Integer (D$_{OUT}$ = 0000 00dd dddd dddd)
For 12-Bit Operation:
11 = Signed fractional (D$_{OUT}$ = sddd dddd dddd 0000, where s = .NOT.d<11>)
10 = Fractional (D$_{OUT}$ = dddd dddd dddd 0000)
01 = Signed integer (D$_{OUT}$ = ssss sddd dddd dddd, where s = .NOT.d<11>)
00 = Integer (D$_{OUT}$ = 0000 dddd dddd dddd)

Note 1:   See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for information on this selection.
   2:   This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
   3:   Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

TABLE 24-2: **PTG OUTPUT DESCRIPTIONS**

PTG Output Number	PTG Output Description
PTGO0	Trigger/Synchronization Source for OC1
PTGO1	Trigger/Synchronization Source for OC2
PTGO2	Trigger/Synchronization Source for OC3
PTGO3	Trigger/Synchronization Source for OC4
PTGO4	Clock Source for OC1
PTGO5	Clock Source for OC2
PTGO6	Clock Source for OC3
PTGO7	Clock Source for OC4
PTGO8	Trigger/Synchronization Source for IC1
PTGO9	Trigger/Synchronization Source for IC2
PTGO10	Trigger/Synchronization Source for IC3
PTGO11	Trigger/Synchronization Source for IC4
PTGO12	Sample Trigger for ADC
PTGO13	Sample Trigger for ADC
PTGO14	Sample Trigger for ADC
PTGO15	Sample Trigger for ADC
PTGO16	PWM Time Base Synchronous Source for PWM[1]
PTGO17	PWM Time Base Synchronous Source for PWM[1]
PTGO18	Mask Input Select for Op Amp/Comparator
PTGO19	Mask Input Select for Op Amp/Comparator
PTGO20	Reserved
PTGO21	Reserved
PTGO22	Reserved
PTGO23	Reserved
PTGO24	Reserved
PTGO25	Reserved
PTGO26	Reserved
PTGO27	Reserved
PTGO28	Reserved
PTGO29	Reserved
PTGO30	PTG Output to PPS Input Selection
PTGO31	PTG Output to PPS Input Selection

Note 1: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

26.3 Programmable CRC Registers

REGISTER 26-1: CRCCON1: CRC CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0
CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0
bit 15							bit 8

R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CRCEN:** CRC Enable bit

1 = CRC module is enabled

0 = CRC module is disabled; all state machines, pointers and CRCWDAT/CRCDAT are reset, other SFRs are not reset

bit 14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** CRC Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode

0 = Continues module operation in Idle mode

bit 12-8 **VWORD<4:0>:** Pointer Value bits

Indicates the number of valid words in the FIFO. Has a maximum value of 8 when PLEN<4:0> > 7 or 16 when PLEN<4:0> ≤ 7.

bit 7 **CRCFUL**: CRC FIFO Full bit

1 = FIFO is full

0 = FIFO is not full

bit 6 **CRCMPT:** CRC FIFO Empty Bit

1 = FIFO is empty

0 = FIFO is not empty

bit 5 **CRCISEL:** CRC Interrupt Selection bit

1 = Interrupt on FIFO is empty; final word of data is still shifting through CRC

0 = Interrupt on shift is complete and CRCWDAT results are ready

bit 4 **CRCGO:** Start CRC bit

1 = Starts CRC serial shifter

0 = CRC serial shifter is turned off

bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit

1 = Data word is shifted into the CRC starting with the LSb (little endian)

0 = Data word is shifted into the CRC starting with the MSb (big endian)

bit 2-0 **Unimplemented:** Read as '0'

TABLE 27-2: CONFIGURATION BITS DESCRIPTION

Bit Field	Description
GCP	General Segment Code-Protect bit 1 = User program memory is not code-protected 0 = Code protection is enabled for the entire program memory space
GWRP	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	Two-Speed Oscillator Start-up Enable bit 1 = Start up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start up device with user-selected oscillator source
PWMLOCK[1]	PWM Lock Enable bit 1 = Certain PWM registers may only be written after a key sequence 0 = PWM registers may be written without a key sequence
FNOSC<2:0>	Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Fast RC Oscillator with Divide-by-16 (FRCDIV16) 101 = Low-Power RC Oscillator (LPRC) 100 = Reserved; do not use 011 = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral Pin Select Configuration bit 1 = Allow only one reconfiguration 0 = Allow multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is a general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
FWDTEN	Watchdog Timer Enable bit 1 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WINDIS	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
PLLKEN	PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

TABLE 30-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO10	VOL	**Output Low Voltage** 4x Sink Driver Pins[2]	—	—	0.4	V	VDD = 3.3V, IOL ≤ 6 mA, -40°C ≤ TA ≤ +85°C IOL ≤ 5 mA, +85°C < TA ≤ +125°C
		Output Low Voltage 8x Sink Driver Pins[3]	—	—	0.4	V	VDD = 3.3V, IOL ≤ 12 mA, -40°C ≤ TA ≤ +85°C IOL ≤ 8 mA, +85°C < TA ≤ +125°C
DO20	VOH	**Output High Voltage** 4x Source Driver Pins[2]	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins[3]	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
DO20A	VOH1	**Output High Voltage** 4x Source Driver Pins[2]	1.5[1]	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0[1]	—	—		IOH ≥ -12 mA, VDD = 3.3V
			3.0[1]	—	—		IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins[3]	1.5[1]	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0[1]	—	—		IOH ≥ -18 mA, VDD = 3.3V
			3.0[1]	—	—		IOH ≥ -10 mA, VDD = 3.3V

Note 1: Parameters are characterized but not tested.
  2: Includes all I/O pins that are not 8x Sink Driver pins (see below).
  3: Includes the following pins:
   For devices with less than 64 pins: RA3, RA4, RA9, RB<7:15> and RC3
   For 64-pin devices: RA4, RA9, RB<7:15>, RC3 and RC15

TABLE 30-13: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1] Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.[2]	Typ.	Max.	Units	Conditions
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.65	—	2.95	V	VDD (Notes 2 and 3)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance.
  2: Parameters are for design guidance only and are not tested in manufacturing.
  3: The VBOR specification is relative to VDD.

31.1   High-Temperature DC Characteristics

TABLE 31-1:   OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	Max MIPS
			dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X
HDC5	3.0 to 3.6V**(1)**	-40°C to +150°C	40

Note 1:   Device is functional at VBORMIN < VDD < VDDMIN. Analog modules, such as the ADC, may have degraded performance. Device functionality is tested but not characterized.

TABLE 31-2:   THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
High-Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+155	°C
Operating Ambient Temperature Range	TA	-40	—	+150	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $I/O = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	PD		$P_{INT} + P_{I/O}$		W
Maximum Allowed Power Dissipation	PDMAX		$(T_J - T_A)/\theta_{JA}$		W

TABLE 31-3:   DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40°C \leq T_A \leq +150°C$				
Parameter No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
Operating Voltage							
HDC10	**Supply Voltage**						
	VDD	—	3.0	3.3	3.6	V	-40°C to +150°C