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### What is "[Embedded - Microcontrollers](#)"?

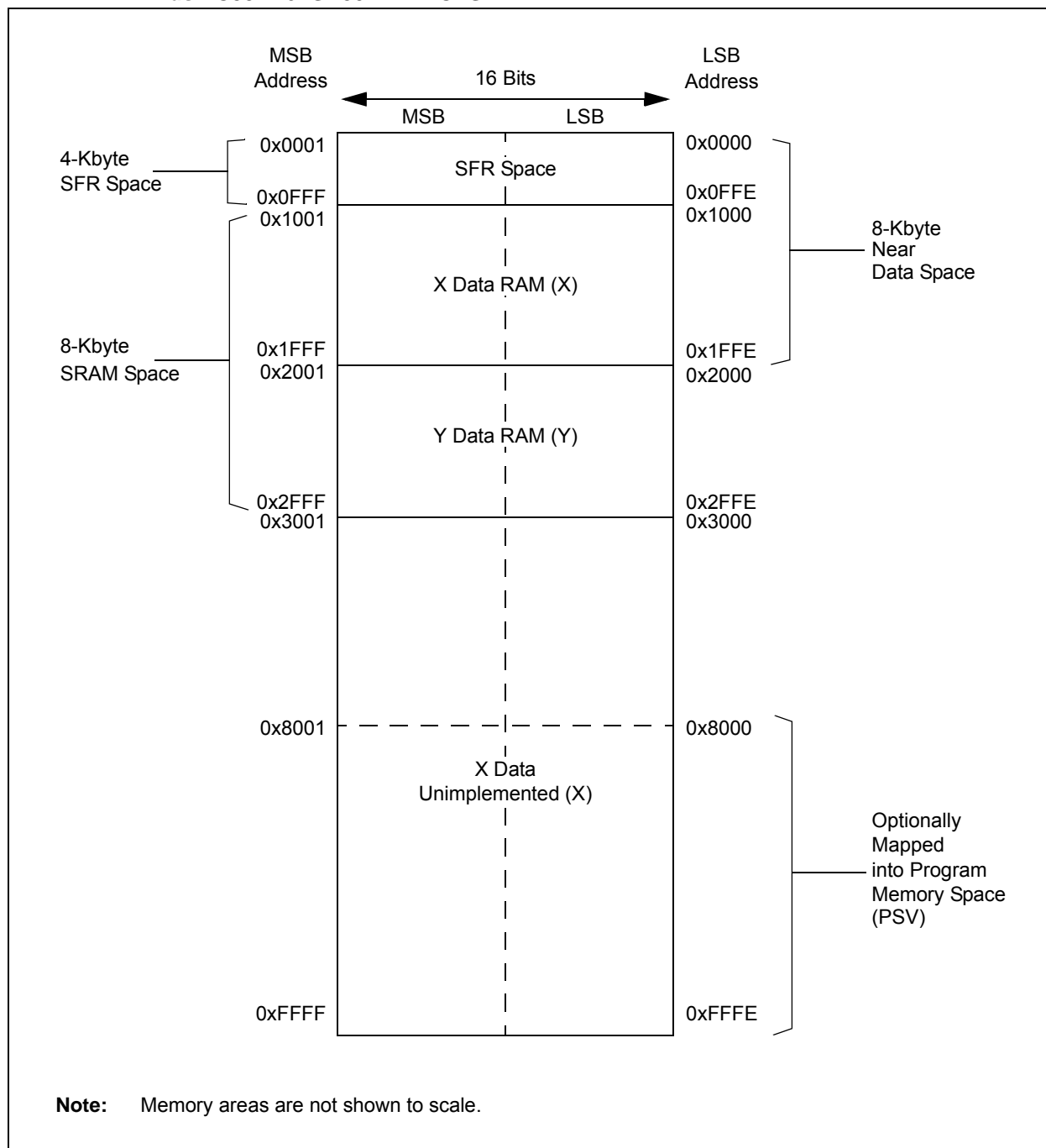
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

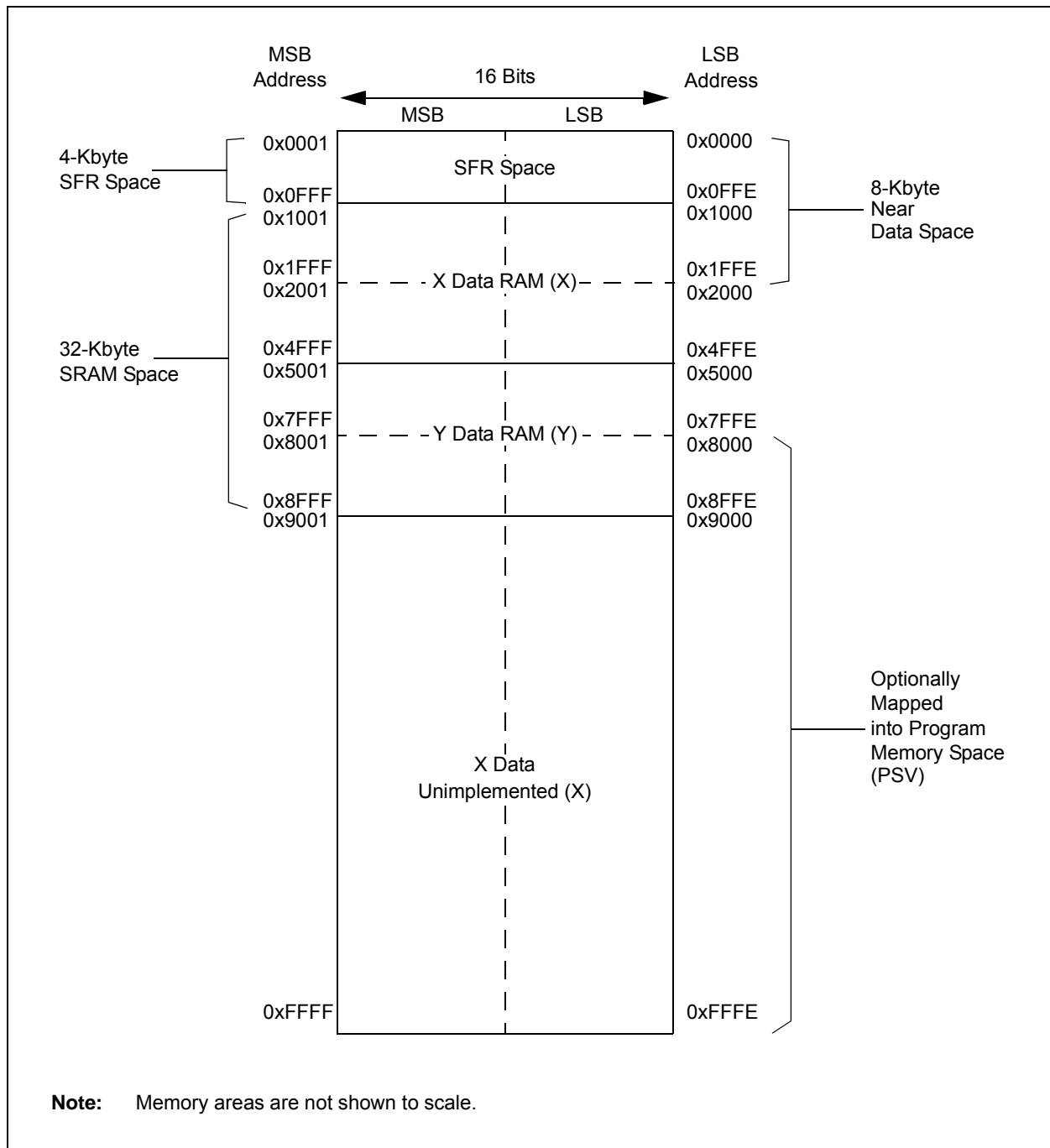
#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gp502-e-sp">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gp502-e-sp</a>

**FIGURE 4-8: DATA MEMORY MAP FOR dsPIC33EP64MC20X/50X AND dsPIC33EP64GP50X DEVICES**



**FIGURE 4-10: DATA MEMORY MAP FOR dsPIC33EP256MC20X/50X AND dsPIC33EP256GP50X DEVICES**



**TABLE 4-59: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	—	—	—	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	001F
PORTA	0E02	—	—	—	—	—	—	—	—	—	—	—	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04	—	—	—	—	—	—	—	—	—	—	—	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	—	—	—	—	—	—	—	—	—	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	—	—	—	—	—	—	—	—	—	—	—	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	—	—	—	—	—	—	—	—	—	—	—	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	—	—	—	—	—	—	—	—	—	—	—	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	ANSA4	—	—	ANSA1	ANSA0	0013

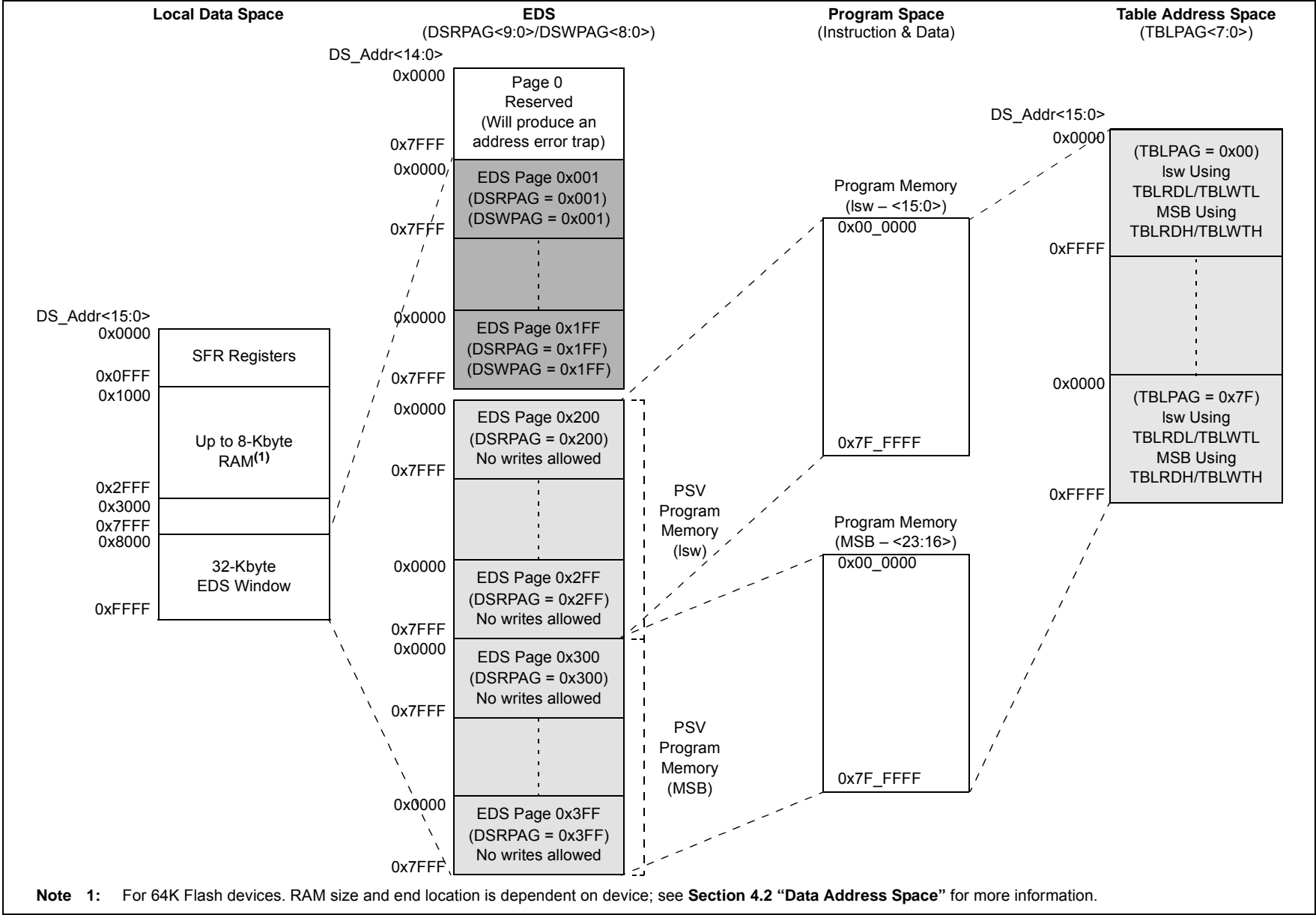
**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-60: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	—	—	—	—	—	—	—	ANSB8	—	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	010F

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

EXAMPLE 4-3: PAGED DATA MEMORY SPACE



- g) The TRISx registers control *only* the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRIS setting. The TRISx register *does not* control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRIS settings, which means that the TRISx bit must be set to input for pins with only remappable input function(s) assigned
- h) All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin has been disabled. Only the Analog Pin Select registers control the digital input buffer, *not* the TRISx register. The user must disable the analog function on a pin using the Analog Pin Select registers in order to use any “digital input(s)” on a corresponding pin, no exceptions.

## 11.6 I/O Ports Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 11.6.1 KEY RESOURCES

- “I/O Ports” (DS70598) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

## 11.7 Peripheral Pin Select Registers

**REGISTER 11-1: RPIR0: PERIPHERAL PIN SELECT INPUT REGISTER 0**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT1R<6:0>						
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **INT1R<6:0>:** Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

**REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)**

- bit 3      **TRIGMODE:** Trigger Status Mode Select bit  
1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software  
0 = TRIGSTAT is cleared only by software
- bit 2-0    **OCM<2:0>:** Output Compare x Mode Select bits  
111 = Center-Aligned PWM mode: Output set high when OCxTMR = OCxR and set low when OCxTMR = OCxRS<sup>(1)</sup>  
110 = Edge-Aligned PWM mode: Output set high when OCxTMR = 0 and set low when OCxTMR = OCxR<sup>(1)</sup>  
101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS  
100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle  
011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin  
010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low  
001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high  
000 = Output compare channel is disabled

**Note 1:** OCxR and OCxRS are double-buffered in PWM mode only.

- 2:** Each Output Compare x module (OCx) has one PTG clock source. See **Section 24.0 “Peripheral Trigger Generator (PTG) Module”** for more information.  
PTG04 = OC1  
PTG05 = OC2  
PTG06 = OC3  
PTG07 = OC4



**REGISTER 16-7: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)**

bit 7-6	<b>DTC&lt;1:0&gt;</b> : Dead-Time Control bits 11 = Dead-Time Compensation mode 10 = Dead-time function is disabled 01 = Negative dead time is actively applied for Complementary Output mode 00 = Positive dead time is actively applied for all output modes
bit 5	<b>DTCP</b> : Dead-Time Compensation Polarity bit <sup>(3)</sup> <u>When Set to '1':</u> If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened. If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened. <u>When Set to '0':</u> If DTCMPx = 0, PWMxH is shortened and PWMxL is lengthened. If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.
bit 4	<b>Unimplemented</b> : Read as '0'
bit 3	<b>MTBS</b> : Master Time Base Select bit 1 = PWM generator uses the secondary master time base for synchronization and as the clock source for the PWM generation logic (if secondary time base is available) 0 = PWM generator uses the primary master time base for synchronization and as the clock source for the PWM generation logic
bit 2	<b>CAM</b> : Center-Aligned Mode Enable bit <sup>(2,4)</sup> 1 = Center-Aligned mode is enabled 0 = Edge-Aligned mode is enabled
bit 1	<b>XPRES</b> : External PWMx Reset Control bit <sup>(5)</sup> 1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode 0 = External pins do not affect PWMx time base
bit 0	<b>IUE</b> : Immediate Update Enable bit <sup>(2)</sup> 1 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are immediate 0 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are synchronized to the PWMx period boundary

- Note**
- 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
  - 2: These bits should not be changed after the PWMx is enabled (PTEN = 1).
  - 3: DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
  - 4: The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
  - 5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

**REGISTER 17-4: POS1CNTH: POSITION COUNTER 1 HIGH WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<23:16>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **POSCNT<31:16>**: High Word Used to Form 32-Bit Position Counter Register (POS1CNT) bits

**REGISTER 17-5: POS1CNTL: POSITION COUNTER 1 LOW WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **POSCNT<15:0>**: Low Word Used to Form 32-Bit Position Counter Register (POS1CNT) bits

**REGISTER 17-6: POS1HLD: POSITION COUNTER 1 HOLD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **POSHLD<15:0>**: Hold Register for Reading and Writing POS1CNTH bits

## 18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
  - a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on  $\overline{SSx}$ .
  - b) If FRMPOL = 0, use a pull-up resistor on  $\overline{SSx}$ .

**Note:** This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode, (i.e., not using  $\overline{SSx}$  from a master):
  - a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on  $\overline{SSx}$ .
  - b) If CKP = 0, always place a pull-down resistor on  $\overline{SSx}$ .

**Note:** This will insure that during power-up and initialization the master/slave will not lose Sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the  $\overline{SSx}$  pin, which indicates the start of a data frame.

**Note:** Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in **Section 30.0 “Electrical Characteristics”** for details.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a ‘1’ for the fastest SPIx data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user’s master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

## 18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 18.2.1 KEY RESOURCES

- “**Serial Peripheral Interface (SPI)**” (DS70569) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

## 20.3 UARTx Control Registers

REGISTER 20-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN <sup>(1)</sup>	—	USIDL	IREN <sup>(2)</sup>	RTSMD	—	UEN1	UEN0
bit 15						bit 8	

R/W-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7						bit 0	

<b>Legend:</b>	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15      **UARTEN:** UARTx Enable bit<sup>(1)</sup>  
 1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>  
 0 = UARTx is disabled; all UARTx pins are controlled by PORT latches; UARTx power consumption is minimal
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **USIDL:** UARTx Stop in Idle Mode bit  
 1 = Discontinues module operation when device enters Idle mode  
 0 = Continues module operation in Idle mode
- bit 12      **IREN:** IrDA<sup>®</sup> Encoder and Decoder Enable bit<sup>(2)</sup>  
 1 = IrDA encoder and decoder are enabled  
 0 = IrDA encoder and decoder are disabled
- bit 11      **RTSMD:** Mode Selection for  $\overline{\text{UxRTS}}$  Pin bit  
 1 =  $\overline{\text{UxRTS}}$  pin is in Simplex mode  
 0 =  $\overline{\text{UxRTS}}$  pin is in Flow Control mode
- bit 10      **Unimplemented:** Read as '0'
- bit 9-8      **UEN<1:0>:** UARTx Pin Enable bits  
 11 = UxTX, UxRX and BCLKx pins are enabled and used;  $\overline{\text{UxCTS}}$  pin is controlled by PORT latches<sup>(3)</sup>  
 10 = UxTX, UxRX,  $\overline{\text{UxCTS}}$  and  $\overline{\text{UxRTS}}$  pins are enabled and used<sup>(4)</sup>  
 01 = UxTX, UxRX and  $\overline{\text{UxRTS}}$  pins are enabled and used;  $\overline{\text{UxCTS}}$  pin is controlled by PORT latches<sup>(4)</sup>  
 00 = UxTX and UxRX pins are enabled and used;  $\overline{\text{UxCTS}}$  and  $\overline{\text{UxRTS/BCLKx}}$  pins are controlled by PORT latches
- bit 7      **WAKE:** Wake-up on Start bit Detect During Sleep Mode Enable bit  
 1 = UARTx continues to sample the UxRX pin; interrupt is generated on the falling edge; bit is cleared in hardware on the following rising edge  
 0 = No wake-up is enabled
- bit 6      **LPBACK:** UARTx Loopback Mode Select bit  
 1 = Enables Loopback mode  
 0 = Loopback mode is disabled

- Note 1:** Refer to the “UART” (DS70582) section in the “dsPIC33/PIC24 Family Reference Manual” for information on enabling the UARTx module for receive or transmit operation.
- 2:** This feature is only available for the 16x BRG mode (BRGH = 0).
- 3:** This feature is only available on 44-pin and 64-pin devices.
- 4:** This feature is only available on 64-pin devices.

## 22.2 CTMU Control Registers

**REGISTER 22-1: CTMUCON1: CTMU CONTROL REGISTER 1**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN <sup>(1)</sup>	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15     **CTMUEN:** CTMU Enable bit  
           1 = Module is enabled  
           0 = Module is disabled
- bit 14     **Unimplemented:** Read as '0'
- bit 13     **CTMUSIDL:** CTMU Stop in Idle Mode bit  
           1 = Discontinues module operation when device enters Idle mode  
           0 = Continues module operation in Idle mode
- bit 12     **TGEN:** Time Generation Enable bit  
           1 = Enables edge delay generation  
           0 = Disables edge delay generation
- bit 11     **EDGEN:** Edge Enable bit  
           1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)  
           0 = Software is used to trigger edges (manual set of EDGxSTAT)
- bit 10     **EDGSEQEN:** Edge Sequence Enable bit  
           1 = Edge 1 event must occur before Edge 2 event can occur  
           0 = No edge sequence is needed
- bit 9      **IDISSEN:** Analog Current Source Control bit<sup>(1)</sup>  
           1 = Analog current source output is grounded  
           0 = Analog current source output is not grounded
- bit 8      **CTTRIG:** ADC Trigger Control bit  
           1 = CTMU triggers ADC start of conversion  
           0 = CTMU does not trigger ADC start of conversion
- bit 7-0    **Unimplemented:** Read as '0'

**Note 1:** The ADC module Sample-and-Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

**NOTES:**

**REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGADJ<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGADJ<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **PTGADJ<15:0>**: PTG Adjust Register bits  
 This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the *PTGADD* command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGL0<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGL0<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **PTGL0<15:0>**: PTG Literal 0 Register bits  
 This register holds the 16-bit value to be written to the AD1CHS0 register with the *PTGCTRL* Step command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER**

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	CVR2OE <sup>(1)</sup>	—	—	—	VREFSEL	—	—
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVR1OE <sup>(1)</sup>	CVRR	CVRSS <sup>(2)</sup>	CVR3	CVR2	CVR1	CVR0
bit 7						bit 0	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'bit 14 **CVR2OE:** Comparator Voltage Reference 2 Output Enable bit<sup>(1)</sup>

1 = (AVDD – AVSS)/2 is connected to the CVREF2O pin

0 = (AVDD – AVSS)/2 is disconnected from the CVREF2O pin

bit 13-11 **Unimplemented:** Read as '0'bit 10 **VREFSEL:** Comparator Voltage Reference Select bit

1 = CVREFIN = VREF+

0 = CVREFIN is generated by the resistor network

bit 9-8 **Unimplemented:** Read as '0'bit 7 **CVREN:** Comparator Voltage Reference Enable bit

1 = Comparator voltage reference circuit is powered on

0 = Comparator voltage reference circuit is powered down

bit 6 **CVR1OE:** Comparator Voltage Reference 1 Output Enable bit<sup>(1)</sup>

1 = Voltage level is output on the CVREF1O pin

0 = Voltage level is disconnected from then CVREF1O pin

bit 5 **CVRR:** Comparator Voltage Reference Range Selection bit

1 = CVRSRC/24 step-size

0 = CVRSRC/32 step-size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit<sup>(2)</sup>

1 = Comparator voltage reference source, CVRSRC = (VREF+) – (AVSS)

0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection  $0 \leq \text{CVR<3:0>} \leq 15$  bitsWhen CVRR = 1: $\text{CVREFIN} = (\text{CVR<3:0>}/24) \cdot (\text{CVRSRC})$ When CVRR = 0: $\text{CVREFIN} = (\text{CVRSRC}/4) + (\text{CVR<3:0>}/32) \cdot (\text{CVRSRC})$ **Note 1:** CVR<sub>x</sub>OE overrides the TRIS<sub>x</sub> and the ANSEL<sub>x</sub> bit settings.**Note 2:** In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.



TABLE 27-2: CONFIGURATION BITS DESCRIPTION

Bit Field	Description
GCP	General Segment Code-Protect bit 1 = User program memory is not code-protected 0 = Code protection is enabled for the entire program memory space
GWRP	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	Two-Speed Oscillator Start-up Enable bit 1 = Start up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start up device with user-selected oscillator source
PWMLOCK <sup>(1)</sup>	PWM Lock Enable bit 1 = Certain PWM registers may only be written after a key sequence 0 = PWM registers may be written without a key sequence
FNOSC<2:0>	Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Fast RC Oscillator with Divide-by-16 (FRCDIV16) 101 = Low-Power RC Oscillator (LPRC) 100 = Reserved; do not use 011 = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral Pin Select Configuration bit 1 = Allow only one reconfiguration 0 = Allow multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is a general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
FWDTEN	Watchdog Timer Enable bit 1 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WINDIS	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
PLLKEN	PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled

**Note 1:** This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**2:** When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

### 30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

#### Absolute Maximum Ratings<sup>(1)</sup>

Ambient temperature under bias .....	-40°C to +125°C
Storage temperature .....	-65°C to +150°C
Voltage on VDD with respect to VSS .....	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS <sup>(3)</sup> .....	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V <sup>(3)</sup> .....	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 3.0V <sup>(3)</sup> .....	-0.3V to +3.6V
Maximum current out of VSS pin .....	300 mA
Maximum current into VDD pin <sup>(2)</sup> .....	300 mA
Maximum current sunk/sourced by any 4x I/O pin .....	15 mA
Maximum current sunk/sourced by any 8x I/O pin .....	25 mA
Maximum current sunk by all ports <sup>(2,4)</sup> .....	200 mA

**Note 1:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

**3:** See the “Pin Diagrams” section for the 5V tolerant pins.

**4:** Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.

**TABLE 30-47: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)  
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	15	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1} \downarrow$ to SCK1 $\uparrow$ or SCK1 $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1} \uparrow$ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	Tsch2ssH, TscL2ssH	$\overline{SS1} \uparrow$ after SCK1 Edge	1.5 TCY + 40	—	—	ns	(Note 4)

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

FIGURE 30-32: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

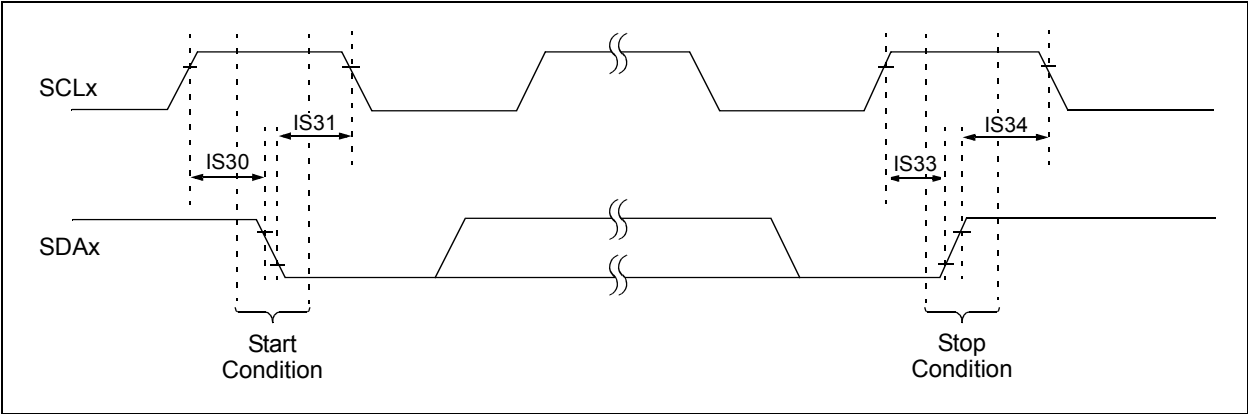
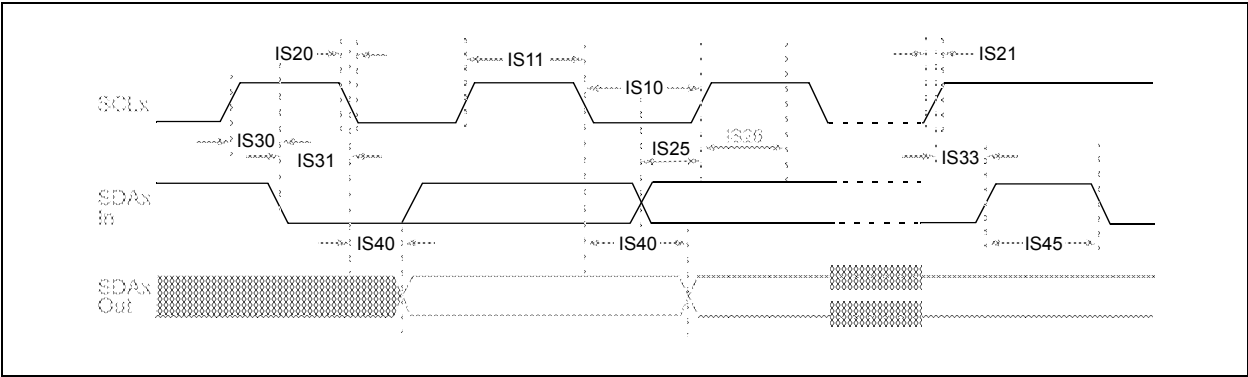


FIGURE 30-33: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



**Revision D (December 2011)**

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

**TABLE A-3: MAJOR SECTION UPDATES**

Section Name	Update Description
<b>“16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High-Speed PWM, Op amps, and Advanced Analog”</b>	Removed the Analog Comparators column and updated the Op amps/Comparators column in Table 1 and Table 2.
<b>Section 21.0 “Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)”</b>	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
<b>Section 30.0 “Electrical Characteristics”</b>	Updated the VBOR specifications and/or its related note in the following electrical characteristics tables: <ul style="list-style-type: none"><li>• Table 30-1</li><li>• Table 30-4</li><li>• Table 30-12</li><li>• Table 30-14</li><li>• Table 30-15</li><li>• Table 30-16</li><li>• Table 30-56</li><li>• Table 30-57</li><li>• Table 30-58</li><li>• Table 30-59</li><li>• Table 30-60</li></ul>