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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gp503t-i-tl

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	—	—	—	—	—	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	C1TXIF	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTIEIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	—	—	—	—	—	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTIEIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC11	0856	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IPC12	0858	—	—	—	—	—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC17	0862	—	—	—	—	—	C1TXIP<2:0>			—	—	—	—	—	—	—	—	0400
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040
IPC35	0886	—	JTAGIP<2:0>			—	ICDIP<2:0>			—	—	—	—	—	—	—	—	4400
IPC36	0888	—	PTG0IP<2:0>			—	PTGWDTIP<2:0>			—	PTGSTIEIP<2:0>			—	—	—	—	4440
IPC37	088A	—	—	—	—	—	PTG3IP<2:0>			—	PTG2IP<2:0>			—	PTG1IP<2:0>			0444

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-9: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 4 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
IC1CON1	0140	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000	
IC1CON2	0142	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D	
IC1BUF	0144	Input Capture 1 Buffer Register																	xxxx
IC1TMR	0146	Input Capture 1 Timer																	0000
IC2CON1	0148	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000	
IC2CON2	014A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D	
IC2BUF	014C	Input Capture 2 Buffer Register																	xxxx
IC2TMR	014E	Input Capture 2 Timer																	0000
IC3CON1	0150	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000	
IC3CON2	0152	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D	
IC3BUF	0154	Input Capture 3 Buffer Register																	xxxx
IC3TMR	0156	Input Capture 3 Timer																	0000
IC4CON1	0158	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000	
IC4CON2	015A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D	
IC4BUF	015C	Input Capture 4 Buffer Register																	xxxx
IC4TMR	015E	Input Capture 4 Timer																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-27: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC204/504 AND PIC24EPXXXGP/MC204 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000
RPOR5	068A	—	—	RP55R<5:0>						—	—	RP54R<5:0>						0000
RPOR6	068C	—	—	RP57R<5:0>						—	—	RP56R<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-28: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC206/506 AND PIC24EPXXXGP/MC206 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000
RPOR5	068A	—	—	RP55R<5:0>						—	—	RP54R<5:0>						0000
RPOR6	068C	—	—	RP57R<5:0>						—	—	RP56R<5:0>						0000
RPOR7	068E	—	—	RP97R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR8	0690	—	—	RP118R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR9	0692	—	—	—	—	—	—	—	—	—	—	RP120R<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-42: OP AMP/COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	PSIDL	—	—	—	C4EVT	C3EVT	C2EVT	C1EVT	—	—	—	—	C4OUT	C3OUT	C2OUT	C1OUT	0000
CVRCON	0A82	—	CVR2OE	—	—	—	VREFSEL	—	—	CVREN	CVR1OE	CVRR	CVRSS	CVR<3:0>				0000
CM1CON	0A84	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM1MSKSRC	0A86	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM1MSKCON	0A88	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM2CON	0A8C	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM2MSKSRC	0A8E	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM2MSKCON	0A90	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM3CON ⁽¹⁾	0A94	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM3MSKSRC ⁽¹⁾	0A96	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM3MSKCON ⁽¹⁾	0A98	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR ⁽¹⁾	0A9A	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM4CON	0A9C	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM4MSKSRC	0A9E	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM4MSKCON	0AA0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM4FLTR	0AA2	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are unavailable on dsPIC33EPXXGP502/MC502/MC202 and PIC24EP256GP/MC202 (28-pin) devices.

TABLE 4-43: CTMU REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTMUCON1	033A	CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	—	—	—	—	—	—	—	—	0000
CTMUCON2	033C	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—	0000
CTMUICON	033E	ITRIM<5:0>						IRNG<1:0>		—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-44: JTAG INTERFACE REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
JDATAH	0FF0	—	—	—	—	JDATAH<27:16>												xxxx
JDATAL	0FF2	JDATAL<15:0>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-53: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	TRISA10	TRISA9	TRISA8	TRISA7	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
PORTA	0E02	—	—	—	—	—	RA10	RA9	RA8	RA7	—	—	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04	—	—	—	—	—	LATA10	LATA9	LATA8	LATA7	—	—	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	—	—	—	—	—	ODCA10	ODCA9	ODCA8	ODCA7	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	—	—	—	—	—	CNIEA10	CNIEA9	CNIEA8	CNIEA7	—	—	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	—	—	—	—	—	CNPUA10	CNPUA9	CNPUA8	CNPUA7	—	—	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	—	—	—	—	—	CNPDA10	CNPDA9	CNPDA8	CNPDA7	—	—	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	ANSA4	—	—	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	—	—	—	—	—	—	—	ANSB8	—	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-55: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	—	—	—	—	—	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	03FF
PORTC	0E22	—	—	—	—	—	—	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	—	—	—	—	—	—	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	—	—	—	—	—	—	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	—	—	—	—	—	—	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	—	—	—	—	—	—	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	—	—	—	—	—	—	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSC2	ANSC1	ANSC0	0007

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.5.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions, which apply to dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and the DSP accumulator class of instructions, which apply to the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.5.4 MAC INSTRUCTIONS (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X DEVICES ONLY)

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSA and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The Two-Source Operand Prefetch registers must be members of the set: {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.5.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	xx	101	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	1
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

9.2 Oscillator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

9.2.1 KEY RESOURCES

- **“Oscillator”** (DS70580) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name ⁽¹⁾	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<6:0>
External Interrupt 2	INT2	RPINR1	INT2R<6:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<6:0>
Input Capture 1	IC1	RPINR7	IC1R<6:0>
Input Capture 2	IC2	RPINR7	IC2R<6:0>
Input Capture 3	IC3	RPINR8	IC3R<6:0>
Input Capture 4	IC4	RPINR8	IC4R<6:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<6:0>
PWM Fault 1 ⁽³⁾	FLT1	RPINR12	FLT1R<6:0>
PWM Fault 2 ⁽³⁾	FLT2	RPINR12	FLT2R<6:0>
QE11 Phase A ⁽³⁾	QEA1	RPINR14	QEA1R<6:0>
QE11 Phase B ⁽³⁾	QEB1	RPINR14	QEB1R<6:0>
QE11 Index ⁽³⁾	INDX1	RPINR15	INDX1R<6:0>
QE11 Home ⁽³⁾	HOME1	RPINR15	HOM1R<6:0>
UART1 Receive	U1RX	RPINR18	U1RXR<6:0>
UART2 Receive	U2RX	RPINR19	U2RXR<6:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<6:0>
SPI2 Clock Input	SCK2	RPINR22	SCK2R<6:0>
SPI2 Slave Select	SS2	RPINR23	SS2R<6:0>
CAN1 Receive ⁽²⁾	C1RX	RPINR26	C1RXR<6:0>
PWM Sync Input 1 ⁽³⁾	SYNCI1	RPINR37	SYNCI1R<6:0>
PWM Dead-Time Compensation 1 ⁽³⁾	DTCMP1	RPINR38	DTCMP1R<6:0>
PWM Dead-Time Compensation 2 ⁽³⁾	DTCMP2	RPINR39	DTCMP2R<6:0>
PWM Dead-Time Compensation 3 ⁽³⁾	DTCMP3	RPINR39	DTCMP3R<6:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

2: This input source is available on dsPIC33EPXXXGP/MC50X devices only.

3: This input source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

REGISTER 11-17: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39
(dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP3R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP2R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

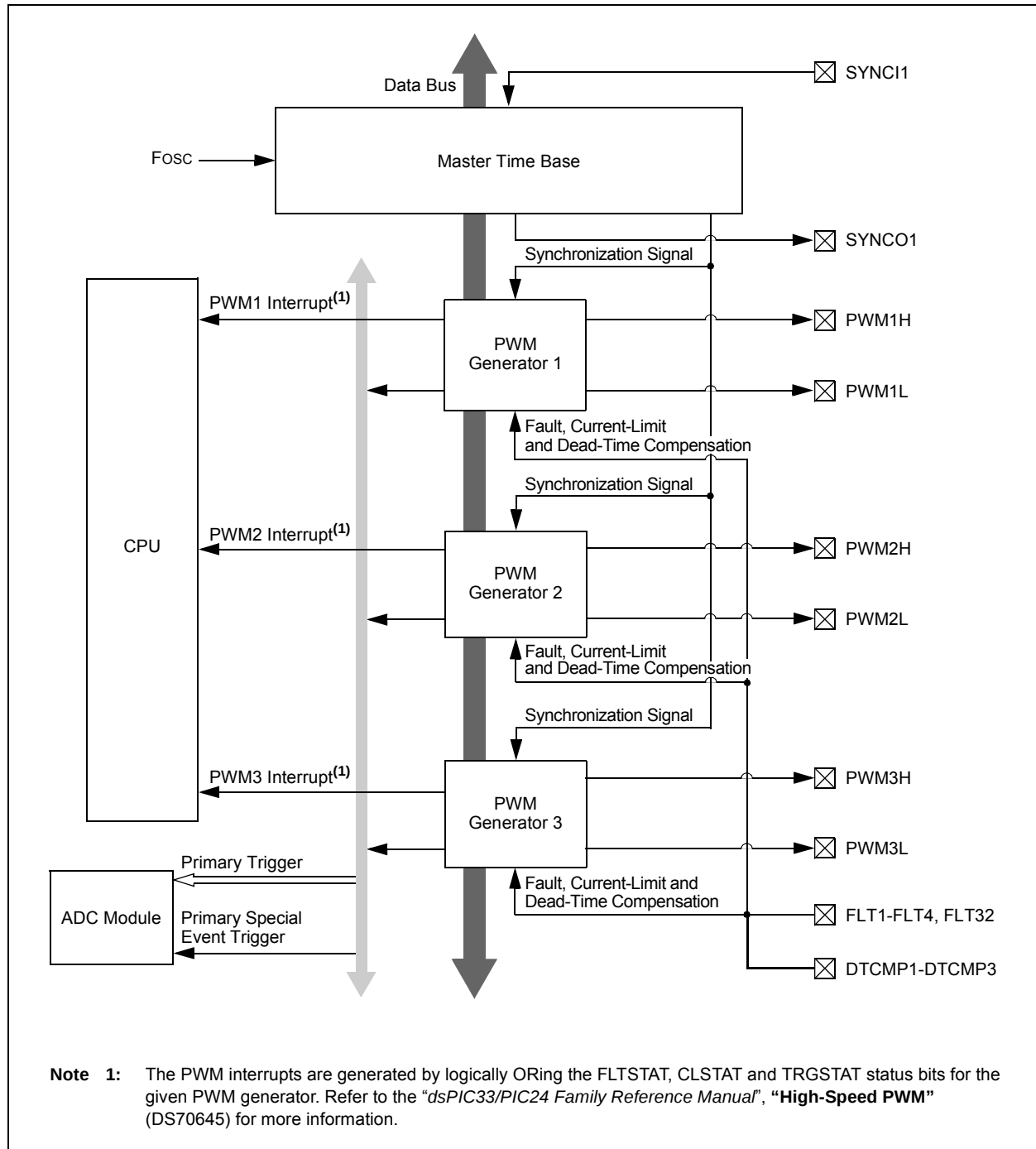
bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP3R<6:0>:** Assign PWM Dead-Time Compensation Input 3 to the Corresponding RPN Pin bits
(see Table 11-2 for input pin selection numbers)
1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **DTCMP2R<6:0>:** Assign PWM Dead-Time Compensation Input 2 to the Corresponding RPN Pin bits
(see Table 11-2 for input pin selection numbers)
1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

FIGURE 16-1: HIGH-SPEED PWMx MODULE ARCHITECTURAL OVERVIEW



REGISTER 17-3: QE1STAT: QE1 STATUS REGISTER (CONTINUED)

bit 2	HOMIEN: Home Input Event Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled
bit 1	IDXIRQ: Status Flag for Index Event Status bit 1 = Index event has occurred 0 = No Index event has occurred
bit 0	IDXIEN: Index Input Event Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled

Note 1: This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
 - a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on $\overline{SSx}$.
 - b) If FRMPOL = 0, use a pull-up resistor on $\overline{SSx}$.

Note: This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode, (i.e., not using $\overline{SSx}$ from a master):
 - a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on $\overline{SSx}$.
 - b) If CKP = 0, always place a pull-down resistor on $\overline{SSx}$.

Note: This will insure that during power-up and initialization the master/slave will not lose Sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the $\overline{SSx}$ pin, which indicates the start of a data frame.

Note: Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in **Section 30.0 "Electrical Characteristics"** for details.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPIx data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

18.2.1 KEY RESOURCES

- "Serial Peripheral Interface (SPI)" (DS70569) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

REGISTER 21-20: CxRXMnSID: ECANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15						bit 8	

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	MIDE	—	EID17	EID16
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-5 **SID<10:0>**: Standard Identifier bits
1 = Includes bit, SIDx, in filter comparison
0 = SIDx bit is a don't care in filter comparison
- bit 4 **Unimplemented**: Read as '0'
- bit 3 **MIDE**: Identifier Receive Mode bit
1 = Matches only message types (standard or extended address) that correspond to EXIDE bit in the filter
0 = Matches either standard or extended address message if filters match (i.e., if (Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID))
- bit 2 **Unimplemented**: Read as '0'
- bit 1-0 **EID<17:16>**: Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = EIDx bit is a don't care in filter comparison

REGISTER 21-21: CxRXMnEID: ECANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15						bit 8	

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-0 **EID<15:0>**: Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = EIDx bit is a don't care in filter comparison

21.5 ECAN Message Buffers

ECAN Message Buffers are part of RAM memory. They are not ECAN Special Function Registers. The user application must directly write into the RAM area that is configured for ECAN Message Buffers. The location and size of the buffer area is defined by the user application.

BUFFER 21-1: ECAN™ MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	SID10	SID9	SID8	SID7	SID6
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID5	SID4	SID3	SID2	SID1	SID0	SRR	IDE
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'
 bit 12-2 **SID<10:0>:** Standard Identifier bits
 bit 1 **SRR:** Substitute Remote Request bit
 When IDE = 0:
 1 = Message will request remote transmission
 0 = Normal message
 When IDE = 1:
 The SRR bit must be set to '1'.
 bit 0 **IDE:** Extended Identifier bit
 1 = Message will transmit Extended Identifier
 0 = Message will transmit Standard Identifier

BUFFER 21-2: ECAN™ MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	EID17	EID16	EID15	EID14
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID13	EID12	EID11	EID10	EID9	EID8	EID7	EID6
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'
 bit 11-0 **EID<17:6>:** Extended Identifier bits

BUFFER 21-3: ECAN™ MESSAGE BUFFER WORD 2

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15							bit 8

U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-10 **EID<5:0>**: Extended Identifier bits
bit 9 **RTR**: Remote Transmission Request bit
When IDE = 1:
1 = Message will request remote transmission
0 = Normal message
When IDE = 0:
The RTR bit is ignored.
bit 8 **RB1**: Reserved Bit 1
User must set this bit to '0' per CAN protocol.
bit 7-5 **Unimplemented**: Read as '0'
bit 4 **RB0**: Reserved Bit 0
User must set this bit to '0' per CAN protocol.
bit 3-0 **DLC<3:0>**: Data Length Code bits

BUFFER 21-4: ECAN™ MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 1							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 0							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Byte 1<15:8>**: ECAN Message Byte 1 bits
bit 7-0 **Byte 0<7:0>**: ECAN Message Byte 0 bits

REGISTER 23-7: AD1CSSH: ADC1 INPUT SCAN SELECT REGISTER HIGH⁽¹⁾

R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
CSS31	CSS30	—	—	—	CSS26 ⁽²⁾	CSS25 ⁽²⁾	CSS24 ⁽²⁾
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CSS31:** ADC1 Input Scan Selection bit
1 = Selects CTMU capacitive and time measurement for input scan (Open)
0 = Skips CTMU capacitive and time measurement for input scan (Open)
- bit 14 **CSS30:** ADC1 Input Scan Selection bit
1 = Selects CTMU on-chip temperature measurement for input scan (CTMU TEMP)
0 = Skips CTMU on-chip temperature measurement for input scan (CTMU TEMP)
- bit 13-11 **Unimplemented:** Read as '0'
- bit 10 **CSS26:** ADC1 Input Scan Selection bit⁽²⁾
1 = Selects OA3/AN6 for input scan
0 = Skips OA3/AN6 for input scan
- bit 9 **CSS25:** ADC1 Input Scan Selection bit⁽²⁾
1 = Selects OA2/AN0 for input scan
0 = Skips OA2/AN0 for input scan
- bit 8 **CSS24:** ADC1 Input Scan Selection bit⁽²⁾
1 = Selects OA1/AN3 for input scan
0 = Skips OA1/AN3 for input scan
- bit 7-0 **Unimplemented:** Read as '0'

Note 1: All AD1CSSH bits can be selected by user software. However, inputs selected for scan, without a corresponding input on the device, convert VREFL.

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

29.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

29.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

29.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

29.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

29.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

TABLE 30-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO10	VOL	Output Low Voltage 4x Sink Driver Pins ⁽²⁾	—	—	0.4	V	VDD = 3.3V, IOL ≤ 6 mA, -40°C ≤ TA ≤ +85°C IOL ≤ 5 mA, +85°C < TA ≤ +125°C
		Output Low Voltage 8x Sink Driver Pins ⁽³⁾	—	—	0.4	V	VDD = 3.3V, IOL ≤ 12 mA, -40°C ≤ TA ≤ +85°C IOL ≤ 8 mA, +85°C < TA ≤ +125°C
DO20	VOH	Output High Voltage 4x Source Driver Pins ⁽²⁾	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins ⁽³⁾	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
DO20A	VOH1	Output High Voltage 4x Source Driver Pins ⁽²⁾	1.5 ⁽¹⁾	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0 ⁽¹⁾	—	—		IOH ≥ -12 mA, VDD = 3.3V
			3.0 ⁽¹⁾	—	—		IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins ⁽³⁾	1.5 ⁽¹⁾	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0 ⁽¹⁾	—	—		IOH ≥ -18 mA, VDD = 3.3V
			3.0 ⁽¹⁾	—	—		IOH ≥ -10 mA, VDD = 3.3V

Note 1: Parameters are characterized but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).

3: Includes the following pins:

For devices with less than 64 pins: RA3, RA4, RA9, RB<7:15> and RC3

For 64-pin devices: RA4, RA9, RB<7:15>, RC3 and RC15

TABLE 30-13: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min. ⁽²⁾	Typ.	Max.	Units	Conditions
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.65	—	2.95	V	VDD (Notes 2 and 3)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance.

2: Parameters are for design guidance only and are not tested in manufacturing.

3: The VBOR specification is relative to VDD.

FIGURE 30-32: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

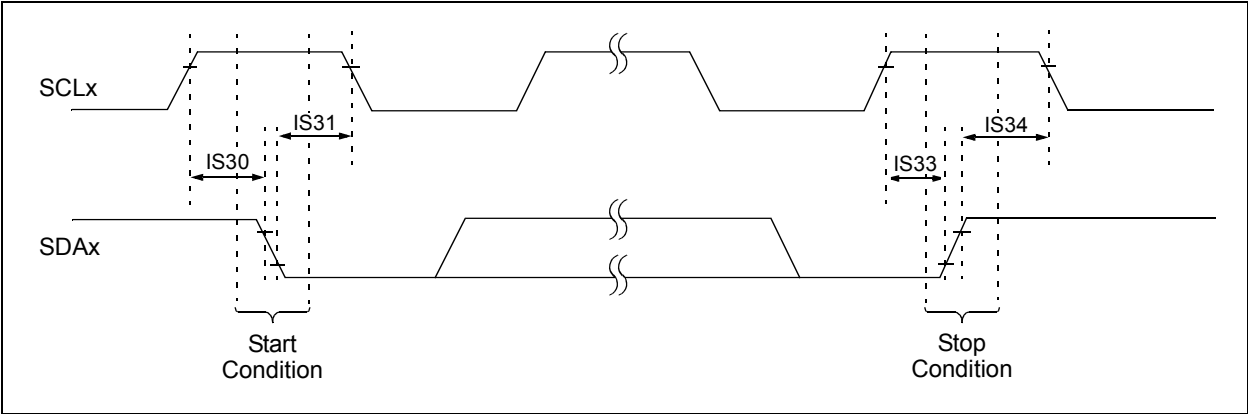


FIGURE 30-33: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

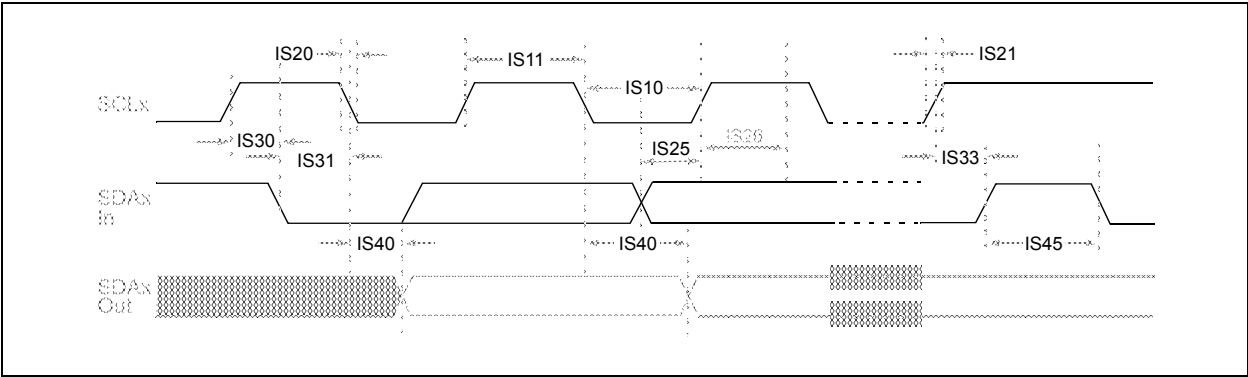


FIGURE 32-5: TYPICAL I_{PD} CURRENT @ $V_{DD} = 3.3V$

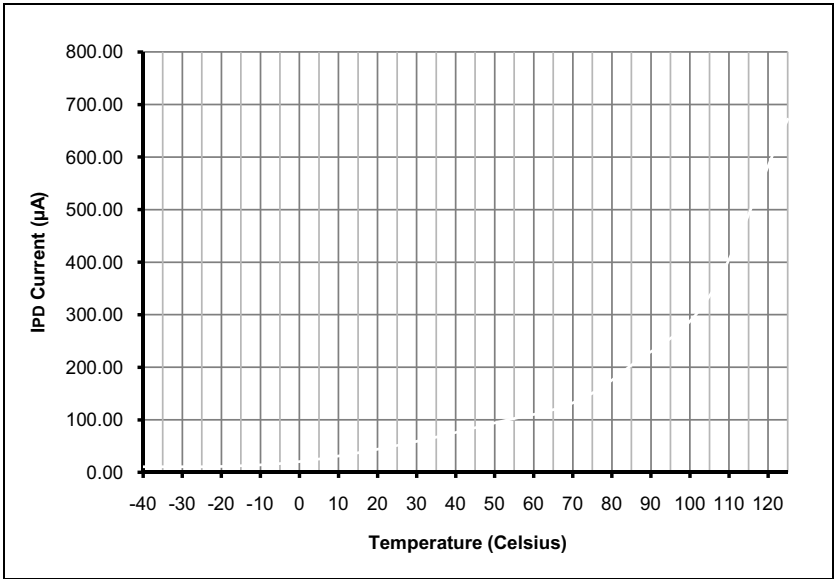


FIGURE 32-6: TYPICAL/MAXIMUM I_{DD} CURRENT @ $V_{DD} = 3.3V$

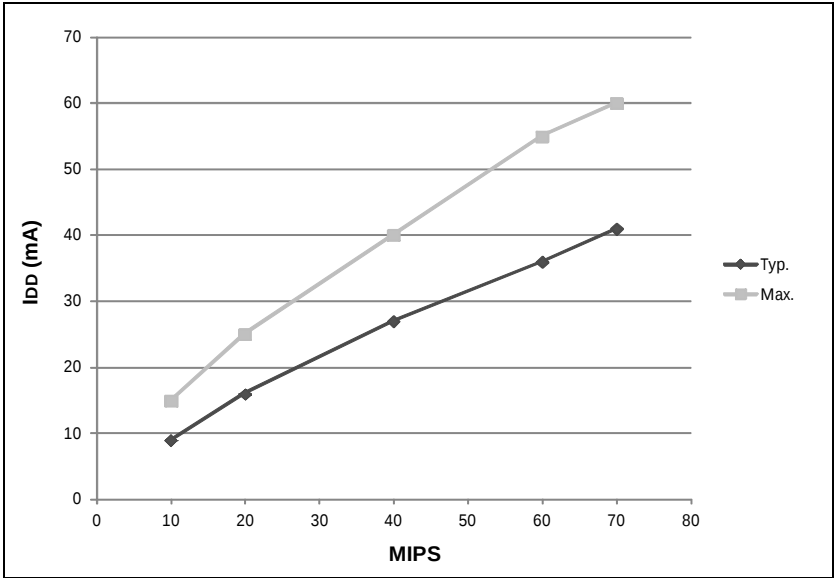


FIGURE 32-7: TYPICAL I_{DOZE} CURRENT @ $V_{DD} = 3.3V$

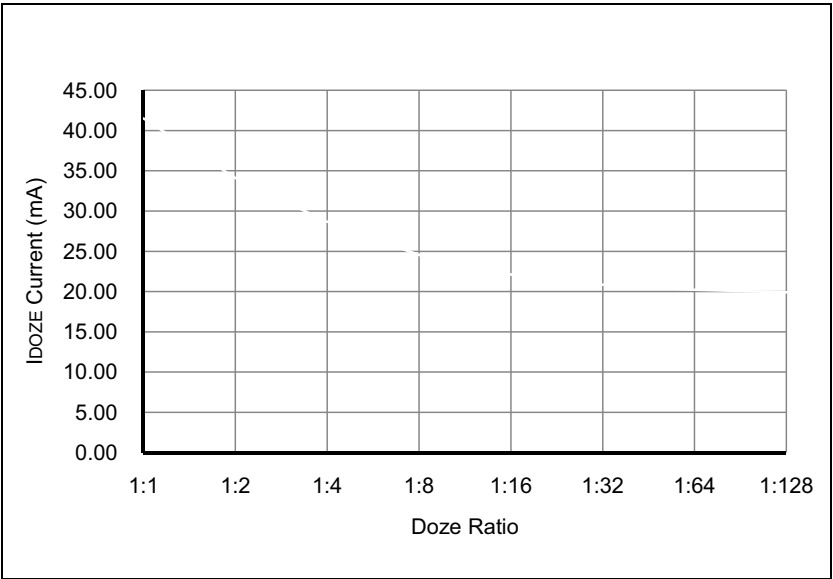


FIGURE 32-8: TYPICAL I_{IDLE} CURRENT @ $V_{DD} = 3.3V$

