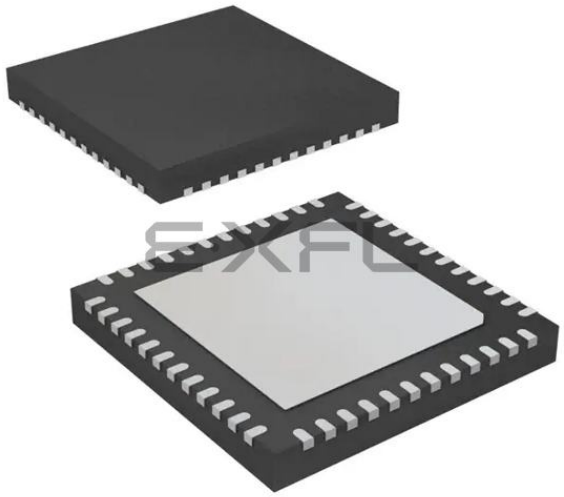
Microchip Technology - DSPIC33EP32GP504-E/MV Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gp504-e-mv

FIGURE 2-5: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER

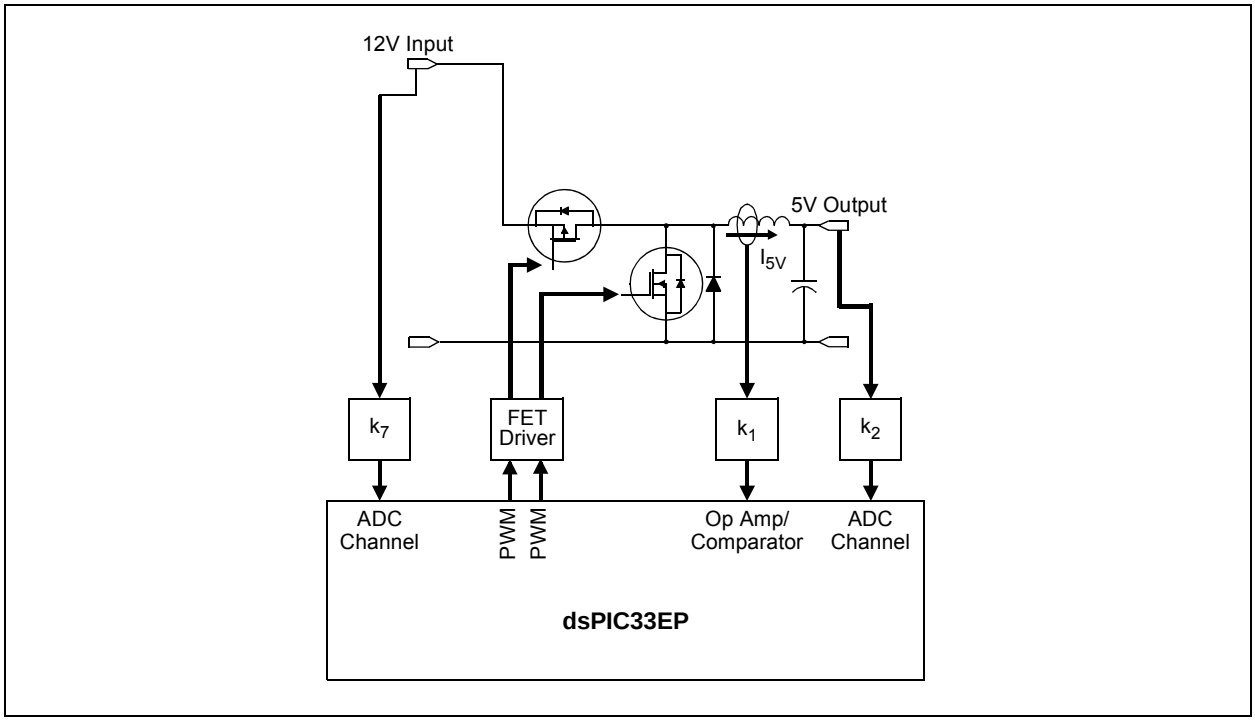


FIGURE 2-6: MULTIPHASE SYNCHRONOUS BUCK CONVERTER

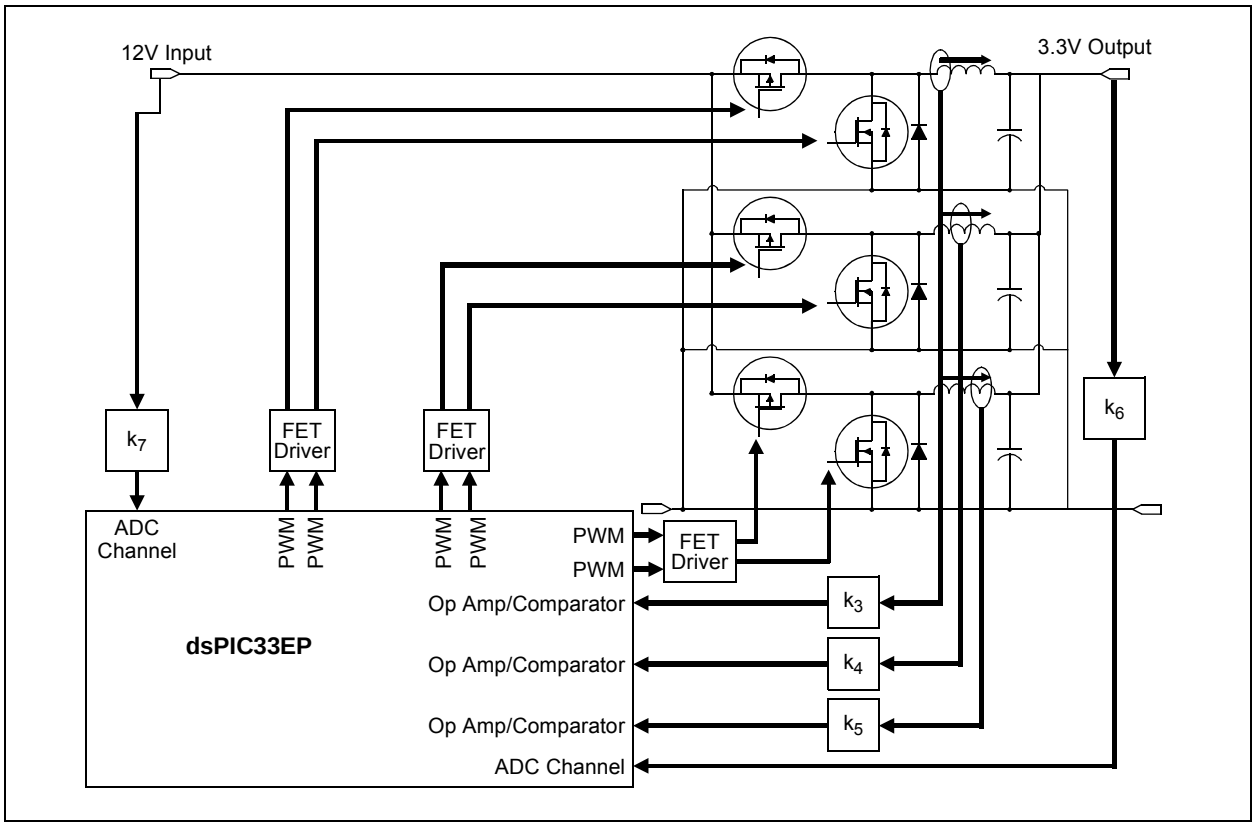
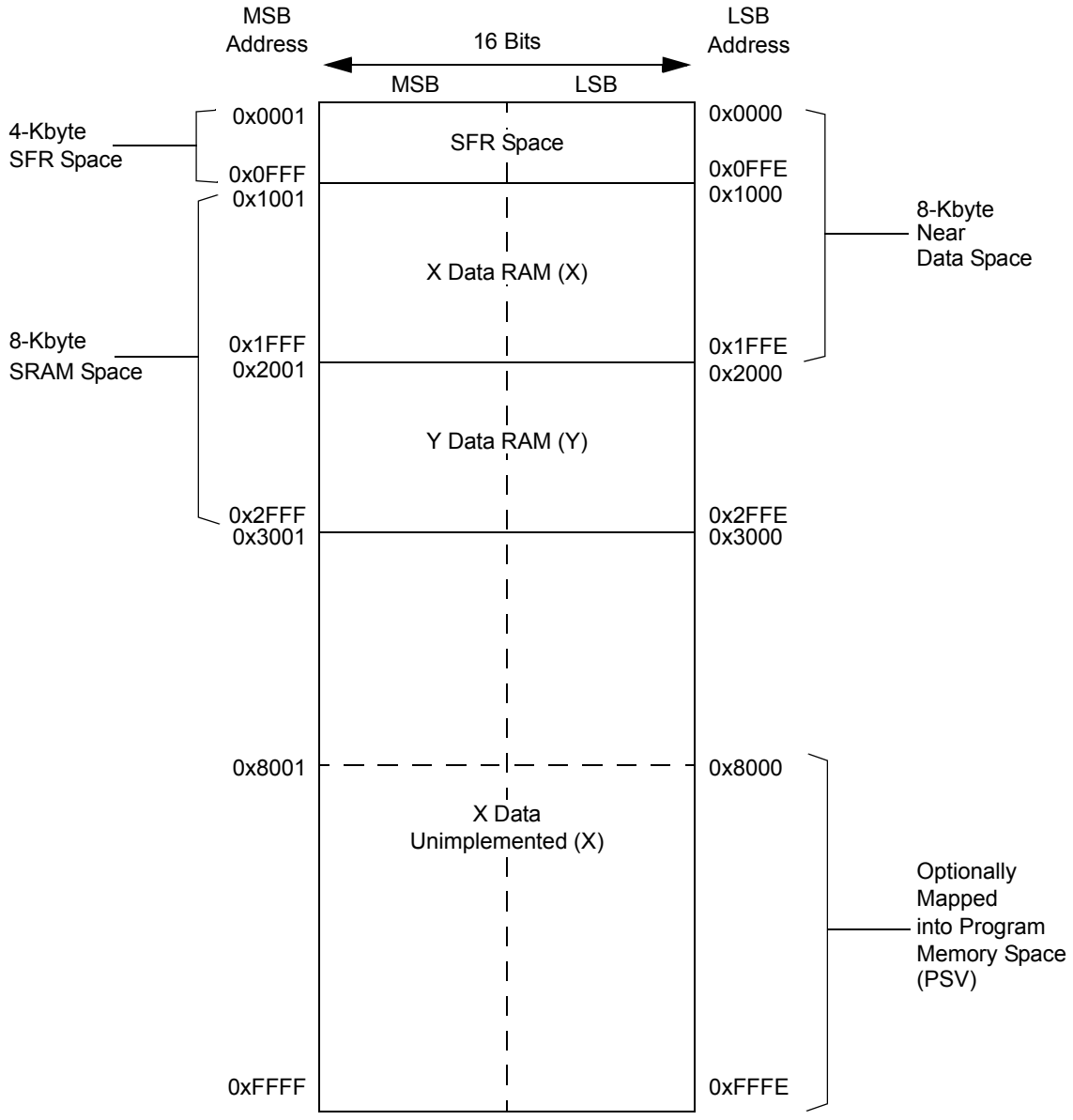


FIGURE 4-8: DATA MEMORY MAP FOR dsPIC33EP64MC20X/50X AND dsPIC33EP64GP50X DEVICES



Note: Memory areas are not shown to scale.

TABLE 4-52: PORTG REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E60	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	—	—	03C0
PORTG	0E62	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	—	—	—	—	xxxx
LATG	0E64	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	—	—	xxxx
ODCG	0E66	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	—	—	0000
CNENG	0E68	—	—	—	—	—	—	CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	—	—	—	—	—	0000
CNPUG	0E6A	—	—	—	—	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	—	—	0000
CNPDG	0E6C	—	—	—	—	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 7-1: INTERRUPT VECTOR DETAILS

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
Highest Natural Order Priority						
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
IC1 – Input Capture 1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
OC1 – Output Compare 1	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
T1 – Timer1	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
IC2 – Input Capture 2	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>
OC2 – Output Compare 2	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
T2 – Timer2	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
T3 – Timer3	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1E – SPI1 Error	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 – SPI1 Transfer Done	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
AD1 – ADC1 Convert Done	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
DMA1 – DMA Channel 1	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
Reserved	23	15	0x000032	—	—	—
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
CM – Comparator Combined Event	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
CN – Input Change Interrupt	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
INT1 – External Interrupt 1	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
Reserved	29-31	21-23	0x00003E-0x000042	—	—	—
DMA2 – DMA Channel 2	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
OC3 – Output Compare 3	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
OC4 – Output Compare 4	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
T4 – Timer4	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
T5 – Timer5	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
SPI2E – SPI2 Error	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 – SPI2 Transfer Done	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>
C1RX – CAN1 RX Data Ready(1)	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
C1 – CAN1 Event(1)	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
DMA3 – DMA Channel 3	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
IC3 – Input Capture 3	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
IC4 – Input Capture 4	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
Reserved	47-56	39-48	0x000062-0x000074	—	—	—
SI2C2 – I2C2 Slave Event	57	49	0x000076	IFS3<1>	IEC3<1>	IPC12<6:4>
MI2C2 – I2C2 Master Event	58	50	0x000078	IFS3<2>	IEC3<2>	IPC12<10:8>
Reserved	59-64	51-56	0x00007A-0x000084	—	—	—
PSEM – PWM Special Event Match(2)	65	57	0x000086	IFS3<9>	IEC3<9>	IPC14<6:4>

Note 1: This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

2: This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

10.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Watchdog Timer and Power-Saving Modes"** (DS70615) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

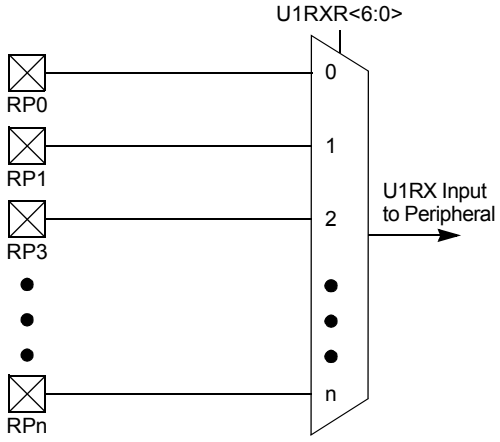
```
PWRSAV  #SLEEP_MODE    ; Put the device into Sleep mode
PWRSAV  #IDLE_MODE     ; Put the device into Idle mode
```

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



Note: For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 25-1 in **Section 25.0 "Op Amp/Comparator Module"**), and the PTG module (see **Section 24.0 "Peripheral Trigger Generator (PTG) Module"**).

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QEI module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in **Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"**.

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of 'b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEI module allows peripherals to be connected to the QEI digital filter input. To utilize this filter, the QEI module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEI digital filter.

EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE

```
RPINR15 = 0x2500;      /* Connect the QEI1 HOME1 input to RP37 (pin 43) */
RPINR7  = 0x009;       /* Connect the IC1 input to the digital filter on the FHOME1 input */

QEI1IOC = 0x4000;      /* Enable the QEI digital filter */
QEI1CON = 0x8000;      /* Enable the QEI module */
```

12.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

12.1.1 KEY RESOURCES

- **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Input Source Select for Synchronization and Trigger Operation bits(4)

11111 = No Sync or Trigger source for ICx
11110 = Reserved
11101 = Reserved
11100 = CTMU module synchronizes or triggers ICx
11011 = ADC1 module synchronizes or triggers ICx(5)
11010 = CMP3 module synchronizes or triggers ICx(5)
11001 = CMP2 module synchronizes or triggers ICx(5)
11000 = CMP1 module synchronizes or triggers ICx(5)
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = Reserved
10011 = IC4 module synchronizes or triggers ICx
10010 = IC3 module synchronizes or triggers ICx
10001 = IC2 module synchronizes or triggers ICx
10000 = IC1 module synchronizes or triggers ICx
01111 = Timer5 synchronizes or triggers ICx
01110 = Timer4 synchronizes or triggers ICx
01101 = Timer3 synchronizes or triggers ICx **(default)**
01100 = Timer2 synchronizes or triggers ICx
01011 = Timer1 synchronizes or triggers ICx
01010 = PTGOx module synchronizes or triggers ICx(6)
01001 = Reserved
01000 = Reserved
00111 = Reserved
00110 = Reserved
00101 = Reserved
00100 = OC4 module synchronizes or triggers ICx
00011 = OC3 module synchronizes or triggers ICx
00010 = OC2 module synchronizes or triggers ICx
00001 = OC1 module synchronizes or triggers ICx
00000 = No Sync or Trigger source for ICx

Note 1: The IC32 bit in both the Odd and Even IC must be set to enable Cascade mode.

2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.

3: This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set and cleared in software.

4: Do not use the ICx module as its own Sync or Trigger source.

5: This option should only be selected as a trigger source and not as a synchronization source.

6: Each Input Capture x (ICx) module has one PTG input source. See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO8 = IC1
PTGO9 = IC2
PTGO10 = IC3
PTGO11 = IC4

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Quadrature Encoder Interface (QEI)"** (DS70601) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High register
- 32-Bit Position Compare Low register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

20.1 UART Helpful Tips

1. In multi-node, direct-connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
   a) If URXINV = 0, use a pull-up resistor on the RX pin.
   b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UARTx module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

20.2.1 KEY RESOURCES

- **"UART"** (DS70582) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

20.3 UARTx Control Registers

REGISTER 20-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN(1)	—	USIDL	IREN(2)	RTSMD	—	UEN1	UEN0
bit 15							bit 8

R/W-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **UARTEN:** UARTx Enable bit(1)
- 1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
- 0 = UARTx is disabled; all UARTx pins are controlled by PORT latches; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **USIDL:** UARTx Stop in Idle Mode bit
- 1 = Discontinues module operation when device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit(2)
- 1 = IrDA encoder and decoder are enabled
- 0 = IrDA encoder and decoder are disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Pin Enable bits
- 11 = UxTX, UxRX and BCLKx pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches(3)
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used(4)
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches(4)
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/BCLKx pins are controlled by PORT latches

bit 7 **WAKE:** Wake-up on Start bit Detect During Sleep Mode Enable bit
- 1 = UARTx continues to sample the UxRX pin; interrupt is generated on the falling edge; bit is cleared in hardware on the following rising edge
- 0 = No wake-up is enabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Enables Loopback mode
- 0 = Loopback mode is disabled

Note 1: Refer to the **"UART"** (DS70582) section in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for receive or transmit operation.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

3: This feature is only available on 44-pin and 64-pin devices.

4: This feature is only available on 64-pin devices.

REGISTER 21-19: CxFMSKSEL2: ECANx FILTER 15-8 MASK SELECTION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15MSK<1:0>		F14MSK<1:0>		F13MSK<1:0>		F12MSK<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F8MSK<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **F15MSK<1:0>:** Mask Source for Filter 15 bits
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F14MSK<1:0>:** Mask Source for Filter 14 bits (same values as bits<15:14>)

bit 11-10 **F13MSK<1:0>:** Mask Source for Filter 13 bits (same values as bits<15:14>)

bit 9-8 **F12MSK<1:0>:** Mask Source for Filter 12 bits (same values as bits<15:14>)

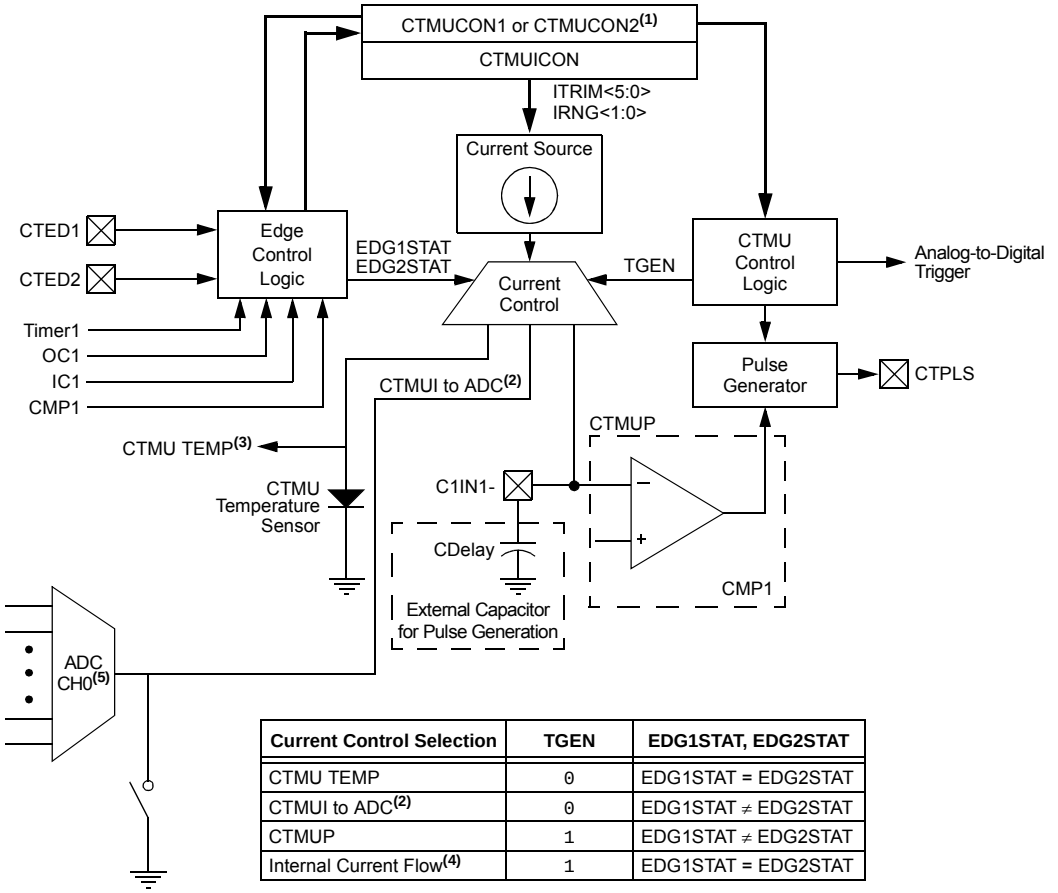
bit 7-6 **F11MSK<1:0>:** Mask Source for Filter 11 bits (same values as bits<15:14>)

bit 5-4 **F10MSK<1:0>:** Mask Source for Filter 10 bits (same values as bits<15:14>)

bit 3-2 **F9MSK<1:0>:** Mask Source for Filter 9 bits (same values as bits<15:14>)

bit 1-0 **F8MSK<1:0>:** Mask Source for Filter 8 bits (same values as bits<15:14>)

FIGURE 22-1: CTMU BLOCK DIAGRAM



Current Control Selection	TGEN	EDG1STAT, EDG2STAT
CTMU TEMP	0	EDG1STAT = EDG2STAT
CTMUI to ADC(2)	0	EDG1STAT ≠ EDG2STAT
CTMUP	1	EDG1STAT ≠ EDG2STAT
Internal Current Flow(4)	1	EDG1STAT = EDG2STAT

Note 1: When the CTMU is not actively used, set TGEN = 1, and ensure that EDG1STAT = EDG2STAT. All other settings allow current to flow into the ADC or the C1IN1- pin. If using the ADC for other purposes besides the CTMU, set IDISSEN = 0. If IDISSEN is set to '1', it will short the output of the ADC CH0 MUX to VSS.

2: CTMUI connects to the output of the ADC CH0 MUX. When CTMU current is steered into this node, the current will flow out through the selected ADC channel determined by the CH0 MUX (see the CH0Sx bits in the AD1CHS0 register).

3: CTMU TEMP connects to one of the ADC CH0 inputs; see CH0SA and CH0SB (AD1CHS0<12:8,4:0).

4: If TGEN = 1 and EDG1STAT = EDG2STAT, CTMU current source is still enabled and may be shunted to VSS internally. This should be considered in low-power applications.

5: The switch connected to ADC CH0 is closed when IDISSEN (CTMUCON1<9>) = 1, and opened when IDISSEN = 0.

22.1 CTMU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

22.1.1 KEY RESOURCES

- **"Charge Time Measurement Unit (CTMU)"** (DS70661) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCTS4	ADCTS3	ADCTS2	ADCTS1	IC4TSS	IC3TSS	IC2TSS	IC1TSS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC4CS	OC3CS	OC2CS	OC1CS	OC4TSS	OC3TSS	OC2TSS	OC1TSS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADCTS4:** Sample Trigger PTGO15 for ADC bit
1 = Generates Trigger when the broadcast command is executed
0 = Does not generate Trigger when the broadcast command is executed

bit 14 **ADCTS3:** Sample Trigger PTGO14 for ADC bit
1 = Generates Trigger when the broadcast command is executed
0 = Does not generate Trigger when the broadcast command is executed

bit 13 **ADCTS2:** Sample Trigger PTGO13 for ADC bit
1 = Generates Trigger when the broadcast command is executed
0 = Does not generate Trigger when the broadcast command is executed

bit 12 **ADCTS1:** Sample Trigger PTGO12 for ADC bit
1 = Generates Trigger when the broadcast command is executed
0 = Does not generate Trigger when the broadcast command is executed

bit 11 **IC4TSS:** Trigger/Synchronization Source for IC4 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 10 **IC3TSS:** Trigger/Synchronization Source for IC3 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 9 **IC2TSS:** Trigger/Synchronization Source for IC2 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 8 **IC1TSS:** Trigger/Synchronization Source for IC1 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 7 **OC4CS:** Clock Source for OC4 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

bit 6 **OC3CS:** Clock Source for OC3 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

bit 5 **OC2CS:** Clock Source for OC2 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

2: This register is only used with the PTGCTRL OPTION = 1111 Step command.

REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGADJ<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGADJ<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGADJ<15:0>:** PTG Adjust Register bits
This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGADD command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGL0<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGL0<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGL0<15:0>:** PTG Literal 0 Register bits
This register holds the 16-bit value to be written to the AD1CHS0 register with the PTGCTRL Step command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	CVR2OE(1)	—	—	—	VREFSEL	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVR1OE(1)	CVRR	CVRSS(2)	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **CVR2OE:** Comparator Voltage Reference 2 Output Enable bit(1)
1 = (AVDD – AVSS)/2 is connected to the CVREF2O pin
0 = (AVDD – AVSS)/2 is disconnected from the CVREF2O pin

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **VREFSEL:** Comparator Voltage Reference Select bit
1 = CVREFIN = VREF+
0 = CVREFIN is generated by the resistor network

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 6 **CVR1OE:** Comparator Voltage Reference 1 Output Enable bit(1)
1 = Voltage level is output on the CVREF1O pin
0 = Voltage level is disconnected from then CVREF1O pin

bit 5 **CVRR:** Comparator Voltage Reference Range Selection bit
1 = CVRSRC/24 step-size
0 = CVRSRC/32 step-size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit(2)
1 = Comparator voltage reference source, CVRSRC = (VREF+) – (AVSS)
0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection 0 ≤ CVR<3:0> ≤ 15 bits
When CVRR = 1:
CVREFIN = (CVR<3:0>/24) • (CVRSRC)
When CVRR = 0:
CVREFIN = (CVRSRC/4) + (CVR<3:0>/32) • (CVRSRC)

Note 1: CVRxOE overrides the TRISx and the ANSELx bit settings.
2: In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(2)	Status Flags Affected
53	NEG	NEG	Acc(1)	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG	f	f = $\bar{f}$ + 1	1	1	C,DC,N,OV,Z
		NEG	f,WREG	WREG = $\bar{f}$ + 1	1	1	C,DC,N,OV,Z
		NEG	Ws,Wd	Wd = $\overline{Ws}$ + 1	1	1	C,DC,N,OV,Z
54	NOP	NOP		No Operation	1	1	None
		NOPR		No Operation	1	1	None
55	POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		POP.S		Pop Shadow Registers	1	1	All
56	PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S		Push Shadow Registers	1	1	None
57	PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep
58	RCALL	RCALL	Expr	Relative Call	1	4	SFA
		RCALL	Wn	Computed Call	1	4	SFA
59	REPEAT	REPEAT	#lit15	Repeat Next Instruction lit15 + 1 times	1	1	None
		REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
60	RESET	RESET		Software device Reset	1	1	None
61	RETFIE	RETFIE		Return from interrupt	1	6 (5)	SFA
62	RETLW	RETLW	#lit10,Wn	Return with literal in Wn	1	6 (5)	SFA
63	RETURN	RETURN		Return from Subroutine	1	6 (5)	SFA
64	RLC	RLC	f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
		RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z
65	RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z
66	RRC	RRC	f	f = Rotate Right through Carry f	1	1	C,N,Z
		RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z
		RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z
67	RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	f,WREG	WREG = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N,Z
68	SAC	SAC	Acc,#Slit4,Wdo(1)	Store Accumulator	1	1	None
		SAC.R	Acc,#Slit4,Wdo(1)	Store Rounded Accumulator	1	1	None
69	SE	SE	Ws,Wnd	Wnd = sign-extended Ws	1	1	C,N,Z
70	SETM	SETM	f	f = 0xFFFF	1	1	None
		SETM	WREG	WREG = 0xFFFF	1	1	None
		SETM	Ws	Ws = 0xFFFF	1	1	None
71	SFTAC	SFTAC	Acc,Wn(1)	Arithmetic Shift Accumulator by (Wn)	1	1	OA,OB,OAB, SA,SB,SAB
		SFTAC	Acc,#Slit6(1)	Arithmetic Shift Accumulator by Slit6	1	1	OA,OB,OAB, SA,SB,SAB

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 30-22: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

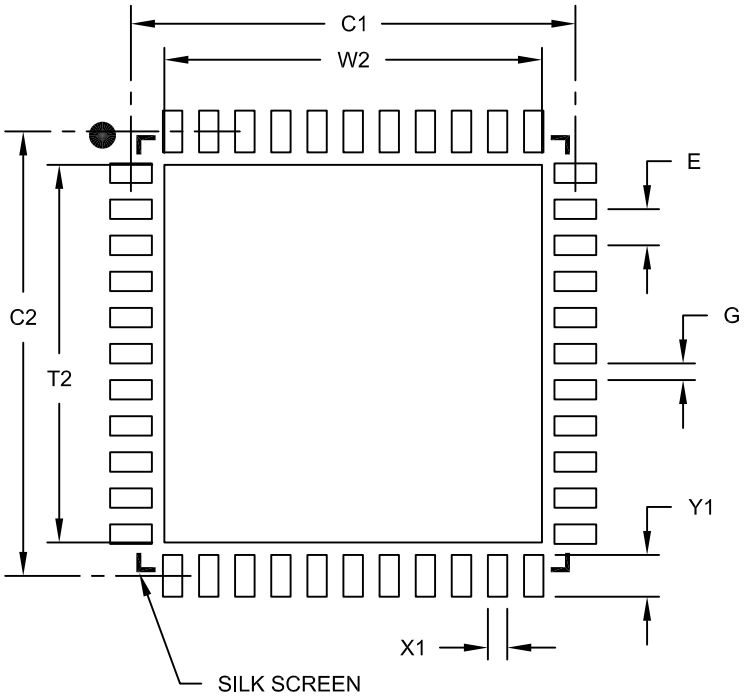
AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SY00	TPU	Power-up Period	—	400	600	μs	
SY10	TOST	Oscillator Start-up Time	—	1024 TOSC	—	—	TOSC = OSC1 period
SY12	TWDT	Watchdog Timer Time-out Period	0.81	0.98	1.22	ms	WDTPRE = 0, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85ºC
			3.26	3.91	4.88	ms	WDTPRE = 1, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85ºC
SY13	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	μs	
SY20	TMCLR	MCLR Pulse Width (low)	2	—	—	μs	
SY30	TBOR	BOR Pulse Width (low)	1	—	—	μs	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	μs	-40°C to +85°C
SY36	TVREG	Voltage Regulator Standby-to-Active mode Transition Time	—	—	30	μs	
SY37	TOSCDFRC	FRC Oscillator Start-up Delay	46	48	54	μs	
SY38	TOSCDLPRC	LPRC Oscillator Start-up Delay	—	—	70	μs	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

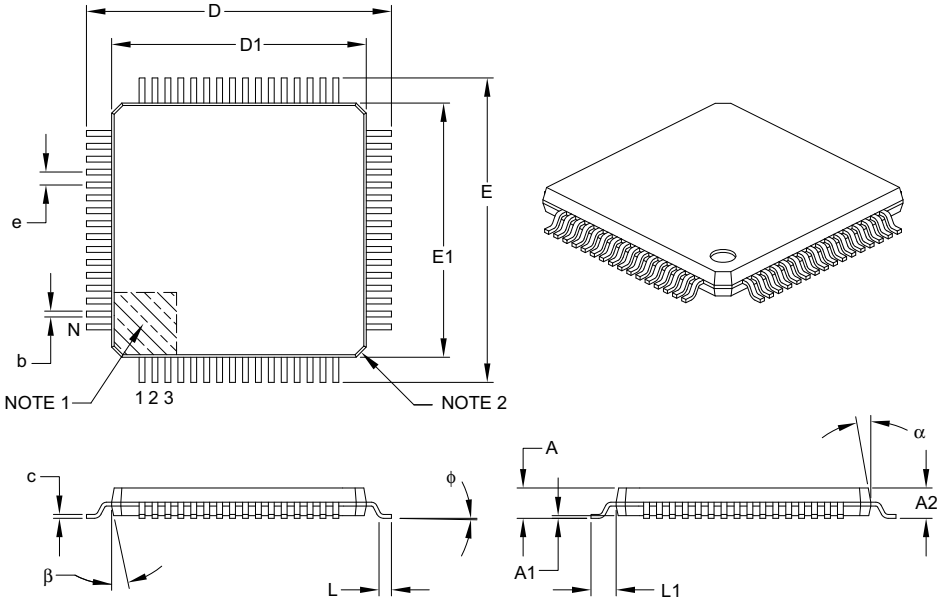
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B

64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		64	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B