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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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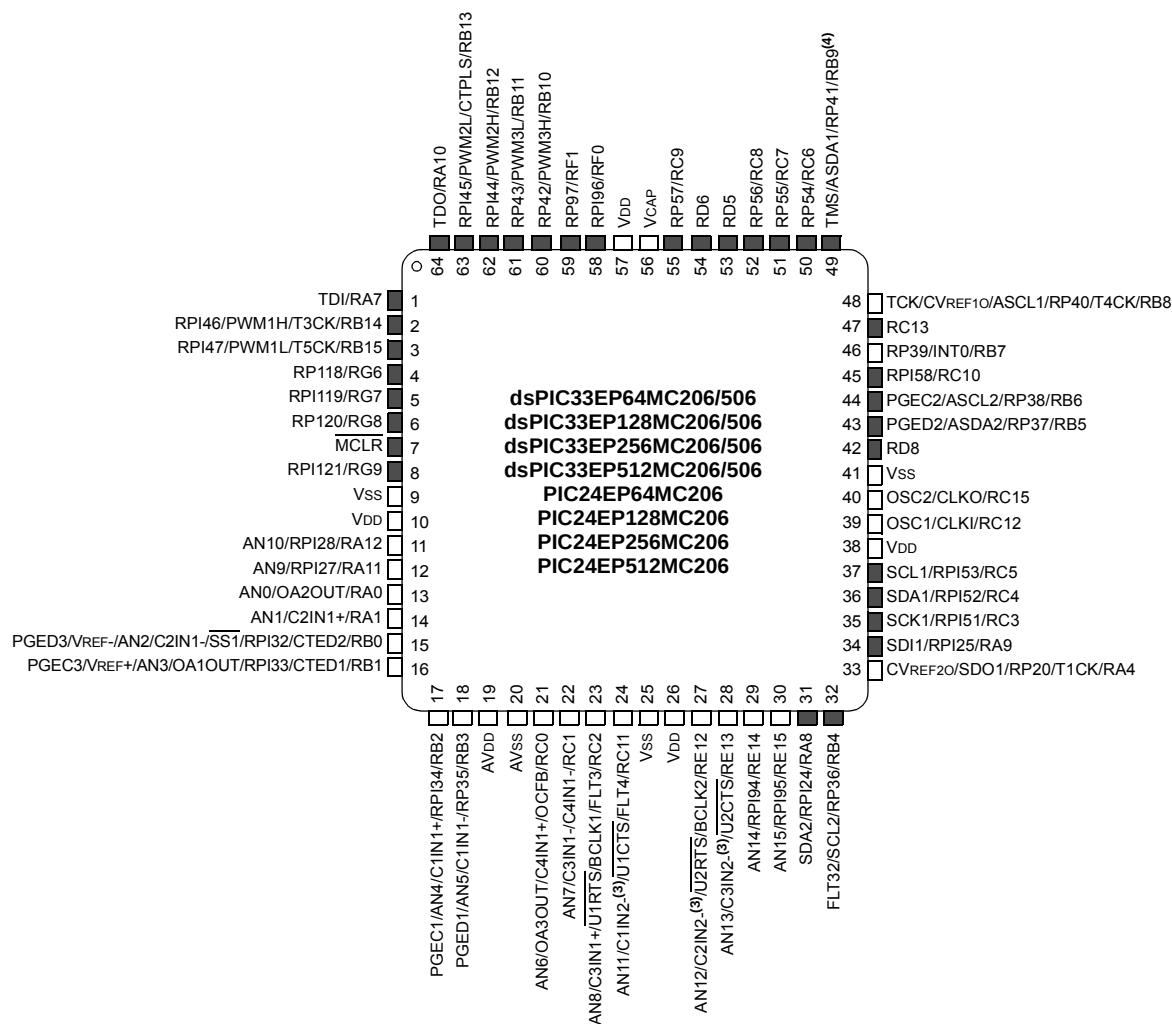
Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gp504-h-pt

Pin Diagrams (Continued)

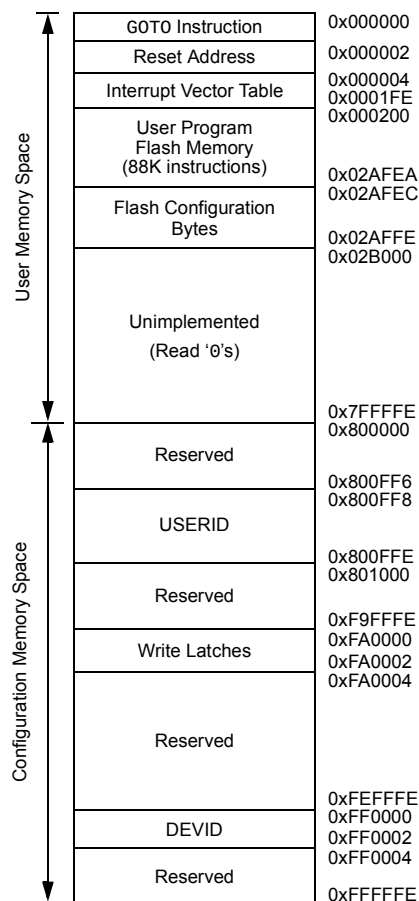
64-Pin TQFP^(1,2,3)

■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
 - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X AND PIC24EP256GP/MC20X DEVICES



Note: Memory areas are not shown to scale.

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	—	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	QE11IF	PSEMIF	—	—	—	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	—	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	QE11IE	PSEMIE	—	—	—	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	—	—	—	—	CRCIE	U2EIE	U1EIE	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IE	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTIEIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	—	—	—	—	—	—	—	—	SPI2IP<2:0>			—	SPI2EIP<2:0>			0044
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC12	0858	—	—	—	—	—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC14	085C	—	—	—	—	—	QE11IP<2:0>			—	PSEMIP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040
IPC23	086E	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC24	0870	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IP<2:0>			4004

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 7-5: INTCON3: INTERRUPT CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	—	DAE	DOOVR	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'
bit 5 **DAE:** DMA Address Error Soft Trap Status bit
 1 = DMA address error soft trap has occurred
 0 = DMA address error soft trap has not occurred
bit 4 **DOOVR:** D0 Stack Overflow Soft Trap Status bit
 1 = D0 stack overflow soft trap has occurred
 0 = D0 stack overflow soft trap has not occurred
bit 3-0 **Unimplemented:** Read as '0'

REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SGHT
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-1 **Unimplemented:** Read as '0'
bit 0 **SGHT:** Software Generated Hard Trap Status bit
 1 = Software generated hard trap has occurred
 0 = Software generated hard trap has not occurred

12.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

12.1.1 KEY RESOURCES

- **“Timers”** (DS70362) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

16.1.2 WRITE-PROTECTED REGISTERS

On dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FOSCSEL<6>). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring, PWMLOCK = 0.

To gain write access to these locked registers, the user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

The correct unlocking sequence is described in Example 16-1.

EXAMPLE 16-1: PWMx WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

```
; FLT32 pin must be pulled low externally in order to clear and disable the fault
; Writing to FCLCON1 register requires unlock sequence

mov #0xabcd,w10      ; Load first unlock key to w10 register
mov #0x4321,w11      ; Load second unlock key to w11 register
mov #0x0000,w0       ; Load desired value of FCLCON1 register in w0
mov w10, PWMKEY      ; Write first unlock key to PWMKEY register
mov w11, PWMKEY      ; Write second unlock key to PWMKEY register
mov w0, FCLCON1      ; Write desired value to FCLCON1 register

; Set PWM ownership and polarity using the IOCON1 register
; Writing to IOCON1 register requires unlock sequence

mov #0xabcd,w10      ; Load first unlock key to w10 register
mov #0x4321,w11      ; Load second unlock key to w11 register
mov #0xF000,w0       ; Load desired value of IOCON1 register in w0
mov w10, PWMKEY      ; Write first unlock key to PWMKEY register
mov w11, PWMKEY      ; Write second unlock key to PWMKEY register
mov w0, IOCON1       ; Write desired value to IOCON1 register
```

21.0 ENHANCED CAN (ECAN™) MODULE (dsPIC33EPXXXGP/ MC50X DEVICES ONLY)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Enhanced Controller Area Network (ECAN™)**” (DS70353) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

21.1 Overview

The Enhanced Controller Area Network (ECAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/protocol was designed to allow communications within noisy environments. The dsPIC33EPXXXGP/MC50X devices contain one ECAN module.

The ECAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details.

The ECAN module features are as follows:

- Implementation of the CAN protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and extended data frames
- 0-8 bytes data length
- Programmable bit rate up to 1 Mbit/sec
- Automatic response to remote transmission requests
- Up to eight transmit buffers with application specified prioritization and abort capability (each buffer can contain up to 8 bytes of data)
- Up to 32 receive buffers (each buffer can contain up to 8 bytes of data)
- Up to 16 full (Standard/Extended Identifier) acceptance filters
- Three full acceptance filter masks
- DeviceNet™ addressing support
- Programmable wake-up functionality with integrated low-pass filter
- Programmable Loopback mode supports self-test operation
- Signaling via interrupt capabilities for all CAN receiver and transmitter error states
- Programmable clock source
- Programmable link to Input Capture (IC2) module for time-stamping and network synchronization
- Low-power Sleep and Idle mode

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

REGISTER 21-8: CxEC: ECANx TRANSMIT/RECEIVE ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TERRCNT<7:0>							
bit 15							
bit 8							

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RERRCNT<7:0>							
bit 7							
bit 0							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **TERRCNT<7:0>**: Transmit Error Count bits

bit 7-0 **RERRCNT<7:0>**: Receive Error Count bits

REGISTER 21-9: CxCFG1: ECANx BAUD RATE CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							
bit 8							

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
bit 7							
bit 0							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **SJW<1:0>**: Synchronization Jump Width bits

11 = Length is 4 x T_Q

10 = Length is 3 x T_Q

01 = Length is 2 x T_Q

00 = Length is 1 x T_Q

bit 5-0 **BRP<5:0>**: Baud Rate Prescaler bits

11 1111 = T_Q = 2 x 64 x 1/FCAN

•

•

•

00 0010 = T_Q = 2 x 3 x 1/FCAN

00 0001 = T_Q = 2 x 2 x 1/FCAN

00 0000 = T_Q = 2 x 1 x 1/FCAN

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0
bit 7							bit 0

Legend: C = Writable bit, but only '0' can be written to clear the bit
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **RXOVF<15:0>**: Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

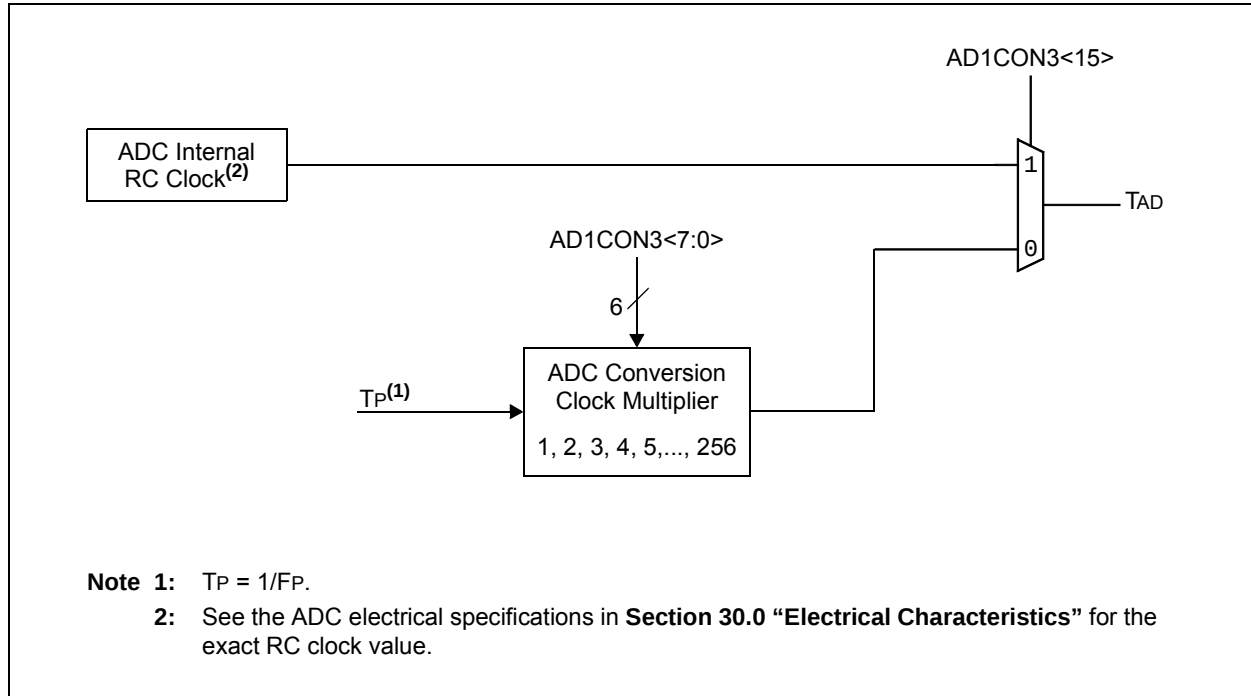
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16
bit 7							bit 0

Legend: C = Writable bit, but only '0' can be written to clear the bit
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **RXOVF<31:16>**: Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

FIGURE 23-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCTS4	ADCTS3	ADCTS2	ADCTS1	IC4TSS	IC3TSS	IC2TSS	IC1TSS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC4CS	OC3CS	OC2CS	OC1CS	OC4TSS	OC3TSS	OC2TSS	OC1TSS
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **ADCTS4:** Sample Trigger PTGO15 for ADC bit
 1 = Generates Trigger when the broadcast command is executed
 0 = Does not generate Trigger when the broadcast command is executed
- bit 14 **ADCTS3:** Sample Trigger PTGO14 for ADC bit
 1 = Generates Trigger when the broadcast command is executed
 0 = Does not generate Trigger when the broadcast command is executed
- bit 13 **ADCTS2:** Sample Trigger PTGO13 for ADC bit
 1 = Generates Trigger when the broadcast command is executed
 0 = Does not generate Trigger when the broadcast command is executed
- bit 12 **ADCTS1:** Sample Trigger PTGO12 for ADC bit
 1 = Generates Trigger when the broadcast command is executed
 0 = Does not generate Trigger when the broadcast command is executed
- bit 11 **IC4TSS:** Trigger/Synchronization Source for IC4 bit
 1 = Generates Trigger/Synchronization when the broadcast command is executed
 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
- bit 10 **IC3TSS:** Trigger/Synchronization Source for IC3 bit
 1 = Generates Trigger/Synchronization when the broadcast command is executed
 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
- bit 9 **IC2TSS:** Trigger/Synchronization Source for IC2 bit
 1 = Generates Trigger/Synchronization when the broadcast command is executed
 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
- bit 8 **IC1TSS:** Trigger/Synchronization Source for IC1 bit
 1 = Generates Trigger/Synchronization when the broadcast command is executed
 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
- bit 7 **OC4CS:** Clock Source for OC4 bit
 1 = Generates clock pulse when the broadcast command is executed
 0 = Does not generate clock pulse when the broadcast command is executed
- bit 6 **OC3CS:** Clock Source for OC3 bit
 1 = Generates clock pulse when the broadcast command is executed
 0 = Does not generate clock pulse when the broadcast command is executed
- bit 5 **OC2CS:** Clock Source for OC2 bit
 1 = Generates clock pulse when the broadcast command is executed
 0 = Does not generate clock pulse when the broadcast command is executed

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

2: This register is only used with the PTGCTRL OPTION = 1111 Step command.

25.1 Op Amp Application Considerations

There are two configurations to take into consideration when designing with the op amp modules that are available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices. Configuration A (see Figure 25-6) takes advantage of the internal connection to the ADC module to route the output of the op amp directly to the ADC for measurement. Configuration B (see Figure 25-7) requires that the designer externally route the output of the op amp (OAxOUT) to a separate analog input pin (ANy) on the device. Table 30-55 in **Section 30.0 “Electrical Characteristics”** describes the performance characteristics for the op amps, distinguishing between the two configuration types where applicable.

25.1.1 OP AMP CONFIGURATION A

Figure 25-6 shows a typical inverting amplifier circuit taking advantage of the internal connections from the op amp output to the input of the ADC. The advantage of this configuration is that the user does not need to consume another analog input (ANy) on the device, and allows the user to simultaneously sample all three op amps with the ADC module, if needed. However, the presence of the internal resistance, RINT1, adds an error in the feedback path. Since RINT1 is an internal resistance, in relation to the op amp output (VOAxOUT) and ADC internal connection (VADC), RINT1 must be included in the numerator term of the transfer function. See Table 30-53 in **Section 30.0 “Electrical Characteristics”** for the typical value of RINT1. Table 30-60 and Table 30-61 in **Section 30.0 “Electrical Characteristics”** describe the minimum sample time (TSAMP) requirements for the ADC module in this configuration. Figure 25-6 also defines the equations that should be used when calculating the expected voltages at points, VADC and VOAxOUT.

FIGURE 25-6: OP AMP CONFIGURATION A

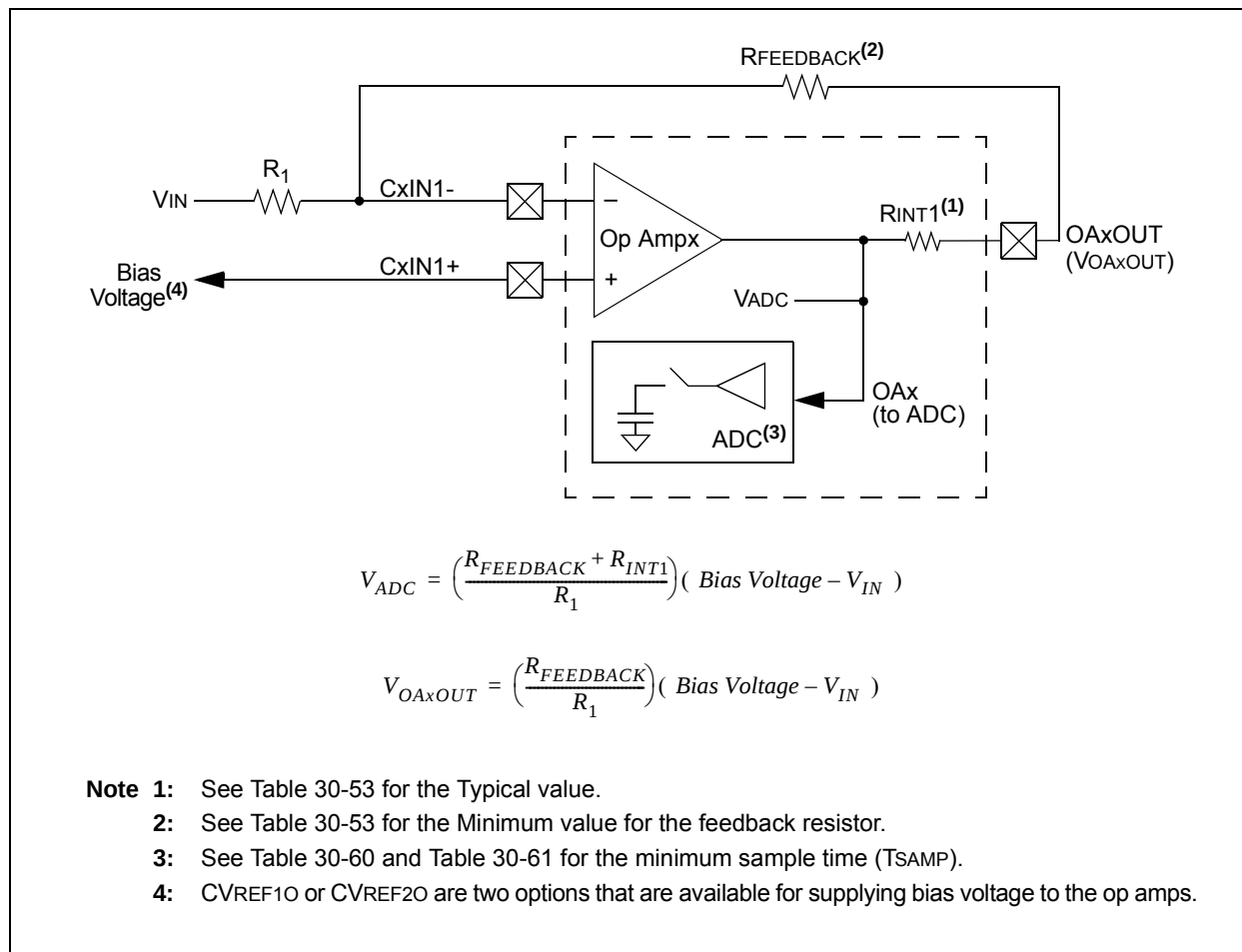


TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
72	SL	SL f	f = Left Shift f	1	1	C,N,OV,Z
		SL f, WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL Ws, Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL Wb, Wns, Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL Wb, #lit5, Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
73	SUB	SUB Acc ⁽¹⁾	Subtract Accumulators	1	1	OA,OB,OAB,SA,SB,SAB
		SUB f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB f, WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB #lit10, Wn	Wn = Wn – lit10	1	1	C,DC,N,OV,Z
		SUB Wb, Ws, Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB Wb, #lit5, Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
74	SUBB	SUBB f	f = f – WREG – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB f, WREG	WREG = f – WREG – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB #lit10, Wn	Wn = Wn – lit10 – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB Wb, Ws, Wd	Wd = Wb – Ws – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB Wb, #lit5, Wd	Wd = Wb – lit5 – ($\overline{C}$)	1	1	C,DC,N,OV,Z
75	SUBR	SUBR f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR f, WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR Wb, Ws, Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR Wb, #lit5, Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
76	SUBBR	SUBBR f	f = WREG – f – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR f, WREG	WREG = WREG – f – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR Wb, Ws, Wd	Wd = Ws – Wb – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR Wb, #lit5, Wd	Wd = lit5 – Wb – ($\overline{C}$)	1	1	C,DC,N,OV,Z
77	SWAP	SWAP.b Wn	Wn = nibble swap Wn	1	1	None
		SWAP Wn	Wn = byte swap Wn	1	1	None
78	TBLRDH	TBLRDH Ws, Wd	Read Prog<23:16> to Wd<7:0>	1	5	None
79	TBLRDL	TBLRDL Ws, Wd	Read Prog<15:0> to Wd	1	5	None
80	TBLWTH	TBLWTH Ws, Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
81	TBLWTL	TBLWTL Ws, Wd	Write Ws to Prog<15:0>	1	2	None
82	ULNK	ULNK	Unlink Frame Pointer	1	1	SFA
83	XOR	XOR f	f = f .XOR. WREG	1	1	N,Z
		XOR f, WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR #lit10, Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR Wb, Ws, Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR Wb, #lit5, Wd	Wd = Wb .XOR. lit5	1	1	N,Z
84	ZE	ZE Ws, Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 30-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO10	VOL	Output Low Voltage 4x Sink Driver Pins ⁽²⁾	—	—	0.4	V	VDD = 3.3V, IOL ≤ 6 mA, -40°C ≤ TA ≤ +85°C IOL ≤ 5 mA, +85°C < TA ≤ +125°C
		Output Low Voltage 8x Sink Driver Pins ⁽³⁾	—	—	0.4	V	VDD = 3.3V, IOL ≤ 12 mA, -40°C ≤ TA ≤ +85°C IOL ≤ 8 mA, +85°C < TA ≤ +125°C
DO20	VOH	Output High Voltage 4x Source Driver Pins ⁽²⁾	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins ⁽³⁾	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
DO20A	VOH1	Output High Voltage 4x Source Driver Pins ⁽²⁾	1.5 ⁽¹⁾	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0 ⁽¹⁾	—	—		IOH ≥ -12 mA, VDD = 3.3V
			3.0 ⁽¹⁾	—	—		IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins ⁽³⁾	1.5 ⁽¹⁾	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0 ⁽¹⁾	—	—		IOH ≥ -18 mA, VDD = 3.3V
			3.0 ⁽¹⁾	—	—		IOH ≥ -10 mA, VDD = 3.3V

Note 1: Parameters are characterized but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).

3: Includes the following pins:

For devices with less than 64 pins: RA3, RA4, RA9, RB<7:15> and RC3

For 64-pin devices: RA4, RA9, RB<7:15>, RC3 and RC15

TABLE 30-13: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min. ⁽²⁾	Typ.	Max.	Units	Conditions
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.65	—	2.95	V	VDD (Notes 2 and 3)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance.

2: Parameters are for design guidance only and are not tested in manufacturing.

3: The VBOR specification is relative to VDD.

TABLE 30-24: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Typ.	Max.	Units	Conditions
TB10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	—	—	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	—	—	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	—	—	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Typ.	Max.	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous, with prescaler	2 Tcy + 40	—	—	ns	N = prescale value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

**TABLE 30-45: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	Lesser of FP or 15	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1} \downarrow$ to SCK1 $\uparrow$ or SCK1 $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1} \uparrow$ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	Tsch2ssH, TscL2ssH	$\overline{SS1} \uparrow$ after SCK1 Edge	1.5 Tcy + 40	—	—	ns	(Note 4)
SP60	TssL2doV	SDO1 Data Output Valid after $\overline{SS1}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 31-12: ADC MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-Bit Mode) ⁽¹⁾							
HAD20a	Nr	Resolution ⁽³⁾	12 Data Bits			bits	
HAD21a	INL	Integral Nonlinearity	-5.5	—	5.5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD22a	DNL	Differential Nonlinearity	-1	—	1	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD23a	GERR	Gain Error	-10	—	10	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD24a	EOFF	Offset Error	-5	—	5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
Dynamic Performance (12-Bit Mode) ⁽²⁾							
HAD33a	FNYQ	Input Signal Bandwidth	—	—	200	kHz	

Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

TABLE 31-13: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (10-Bit Mode) ⁽¹⁾							
HAD20b	Nr	Resolution ⁽³⁾	10 Data Bits			bits	
HAD21b	INL	Integral Nonlinearity	-1.5	—	1.5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD22b	DNL	Differential Nonlinearity	-0.25	—	0.25	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD23b	GERR	Gain Error	-2.5	—	2.5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD24b	EOFF	Offset Error	-1.25	—	1.25	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
Dynamic Performance (10-Bit Mode) ⁽²⁾							
HAD33b	FNYQ	Input Signal Bandwidth	—	—	400	kHz	

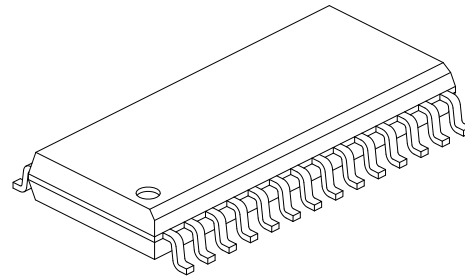
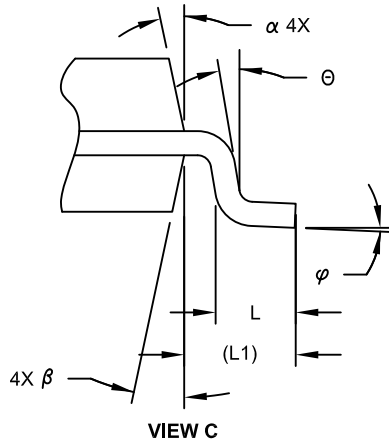
Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

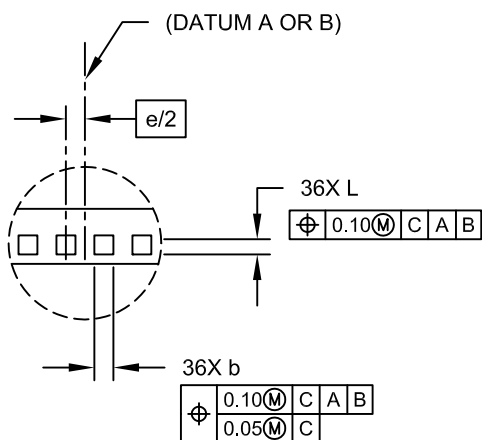
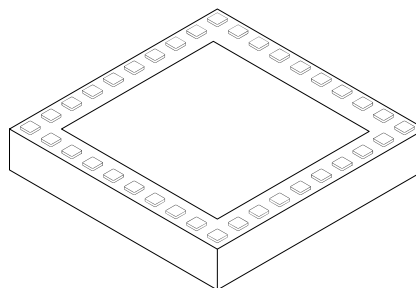
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

**DETAIL A**

Dimension	Units	MILLIMETERS		
	Limits	MIN	NOM	MAX
Number of Pins	N	36		
Number of Pins per Side	ND	10		
Number of Pins per Side	NE	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	3.60	3.75	3.90
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	3.60	3.75	3.90
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

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