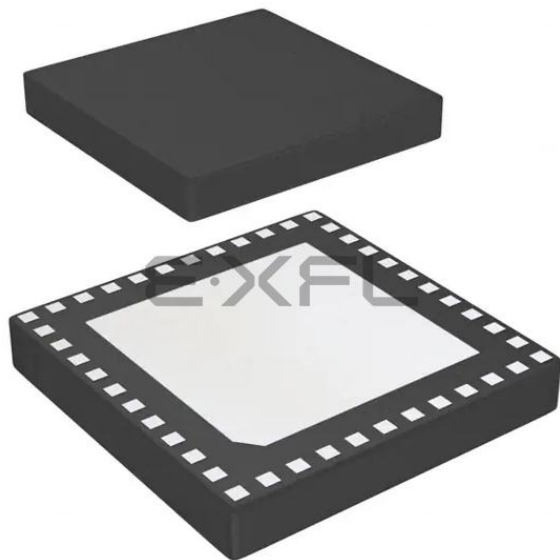




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gp504-h-tl

3.7 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA ⁽¹⁾	OB ⁽¹⁾	SA ^(1,4)	SB ^(1,4)	OAB ⁽¹⁾	SAB ⁽¹⁾	DA ⁽¹⁾	DC
bit 15							bit 8

R/W-0 ^(2,3)	R/W-0 ^(2,3)	R/W-0 ^(2,3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2	IPL1	IPL0	RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **OA:** Accumulator A Overflow Status bit⁽¹⁾
 1 = Accumulator A has overflowed
 0 = Accumulator A has not overflowed
- bit 14 **OB:** Accumulator B Overflow Status bit⁽¹⁾
 1 = Accumulator B has overflowed
 0 = Accumulator B has not overflowed
- bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit^(1,4)
 1 = Accumulator A is saturated or has been saturated at some time
 0 = Accumulator A is not saturated
- bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit^(1,4)
 1 = Accumulator B is saturated or has been saturated at some time
 0 = Accumulator B is not saturated
- bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit⁽¹⁾
 1 = Accumulators A or B have overflowed
 0 = Neither Accumulators A or B have overflowed
- bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit⁽¹⁾
 1 = Accumulators A or B are saturated or have been saturated at some time
 0 = Neither Accumulators A or B are saturated
- bit 9 **DA:** D0 Loop Active bit⁽¹⁾
 1 = D0 loop is in progress
 0 = D0 loop is not in progress
- bit 8 **DC:** MCU ALU Half Carry/Borrow bit
 1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
 0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

- Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
- Note 2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- Note 3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- Note 4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC35	0886	—	JTAGIP<2:0>			—	ICDIP<2:0>			—	—	—	—	—	—	—	—	4400
IPC36	0888	—	PTG0IP<2:0>			—	PTGWDTP<2:0>			—	PTGSTEPIP<2:0>			—	—	—	—	4440
IPC37	088A	—	—	—	—	—	PTG3IP<2:0>			—	PTG2IP<2:0>			—	PTG1IP<2:0>			0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVATE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR<3:0>				VECNUM<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: CRC REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON1	0640	CRCEN	—	CSIDL	VWORD<4:0>					CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—	0000
CRCCON2	0642	—	—	—	DWIDTH<4:0>					—	—	—	PLEN<4:0>					0000
CRCXORL	0644	X<15:1>															—	0000
CRCXORH	0646	X<31:16>															0000	
CRCDATL	0648	CRC Data Input Low Word															0000	
CRCDATH	064A	CRC Data Input High Word															0000	
CRCWDATL	064C	CRC Result Low Word															0000	
CRCWDATH	064E	CRC Result High Word															0000	

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

TABLE 4-25: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC202/502 AND PIC24EPXXXGP/MC202 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC203/503 AND PIC24EPXXXGP/MC203 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000
RPOR5	068A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
RPOR6	068C	—	—	—	—	—	—	—	—	—	—	RP56R<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible regardless of the contents of the Data Space Page registers. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of base Data Space, in combination with DSRPAG = 0x000 or DSWPAG = 0x000. Consequently, DSRPAG and DSWPAG are initialized to 0x001 at Reset.

Note 1: DSxPAG should not be used to access Page 0. An EDS access with DSxPAG set to 0x000 will generate an address error trap.

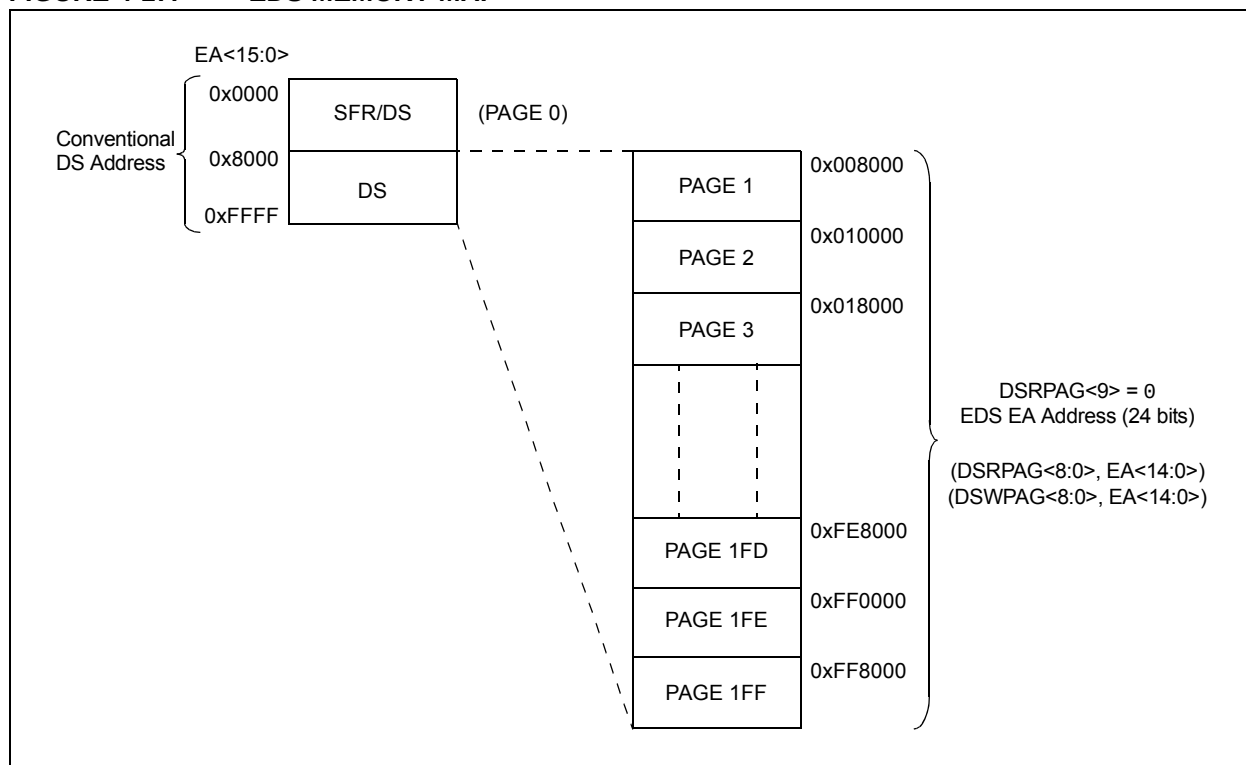
2: Clearing the DSxPAG in software has no effect.

The remaining pages, including both EDS and PSV pages, are only accessible using the DSRPAG or DSWPAG registers in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA<15> = 1.

For example, when DSRPAG = 0x001 or DSWPAG = 0x001, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF, of the Data Space will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x002 or DSWPAG = 0x002, accesses to the upper 32 Kbytes of the Data Space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-17.

For more information on the PSV page access using Data Space Page registers, refer to the “**Program Space Visibility from Data Space**” section in “**Program Memory**” (DS70613) of the “*dsPIC33/PIC24 Family Reference Manual*”.

FIGURE 4-17: EDS MEMORY MAP



17.2 QEI Control Registers

REGISTER 17-1: QE1CON: QE1 CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QE1EN	—	QE1SIDL	PIMOD2 ⁽¹⁾	PIMOD1 ⁽¹⁾	PIMOD0 ⁽¹⁾	IMV1 ⁽²⁾	IMV0 ⁽²⁾
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INTDIV2 ⁽³⁾	INTDIV1 ⁽³⁾	INTDIV0 ⁽³⁾	CNTPOL	GATEN	CCM1	CCM0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

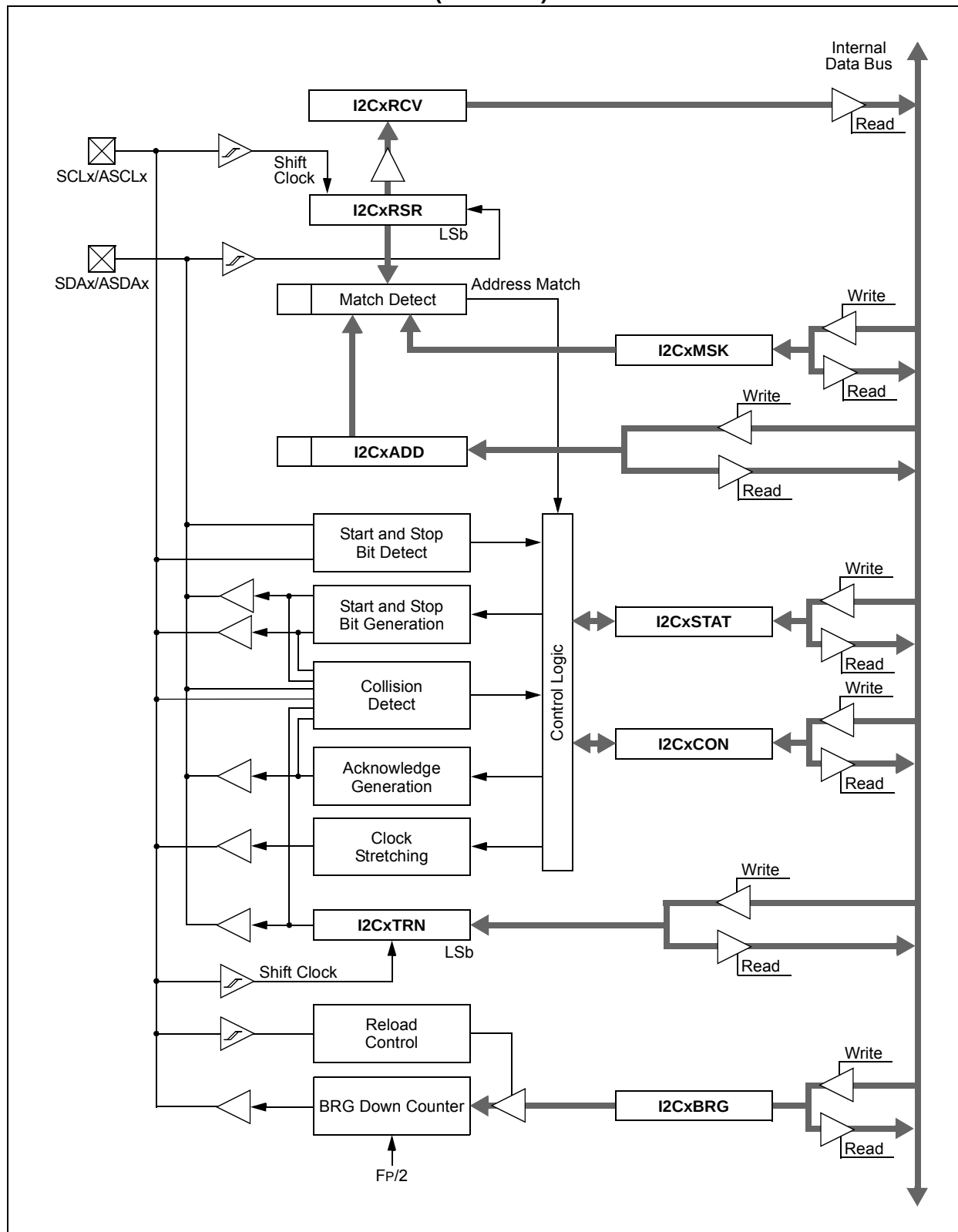
x = Bit is unknown

- bit 15 **QE1EN:** Quadrature Encoder Interface Module Counter Enable bit
 1 = Module counters are enabled
 0 = Module counters are disabled, but SFRs can be read or written to
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **QE1SIDL:** QE1 Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-10 **PIMOD<2:0>:** Position Counter Initialization Mode Select bits⁽¹⁾
 111 = Reserved
 110 = Modulo Count mode for position counter
 101 = Resets the position counter when the position counter equals QE1GEC register
 100 = Second index event after home event initializes position counter with contents of QE1IIC register
 011 = First index event after home event initializes position counter with contents of QE1IIC register
 010 = Next index input event initializes the position counter with contents of QE1IIC register
 001 = Every index input event resets the position counter
 000 = Index input event does not affect position counter
- bit 9 **IMV1:** Index Match Value for Phase B bit⁽²⁾
 1 = Phase B match occurs when QEB = 1
 0 = Phase B match occurs when QEB = 0
- bit 8 **IMV0:** Index Match Value for Phase A bit⁽²⁾
 1 = Phase A match occurs when QEA = 1
 0 = Phase A match occurs when QEA = 0
- bit 7 **Unimplemented:** Read as '0'

- Note 1:** When CCM<1:0> = 10 or 11, all of the QE1 counters operate as timers and the PIMOD<2:0> bits are ignored.
- 2:** When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.
- 3:** The selected clock rate should be at least twice the expected maximum quadrature count rate.

Note 1: In Standard mode, the FIFO is only one level deep.

FIGURE 19-1: I2Cx BLOCK DIAGRAM (x = 1 OR 2)



REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

- bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I²C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching
- bit 5 **ACKDT:** Acknowledge Data bit (when operating as I²C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge
- bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I²C master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit. Hardware is clear at the end of the master Acknowledge sequence.
0 = Acknowledge sequence is not in progress
- bit 3 **RCEN:** Receive Enable bit (when operating as I²C master)
1 = Enables Receive mode for I²C. Hardware is clear at the end of the eighth bit of the master receive data byte.
0 = Receive sequence is not in progress
- bit 2 **PEN:** Stop Condition Enable bit (when operating as I²C master)
1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of the master Stop sequence.
0 = Stop condition is not in progress
- bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I²C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Repeated Start sequence.
0 = Repeated Start condition is not in progress
- bit 0 **SEN:** Start Condition Enable bit (when operating as I²C master)
1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Start sequence.
0 = Start condition is not in progress

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

REGISTER 23-3: AD1CON3: ADC1 CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC4 ⁽¹⁾	SAMC3 ⁽¹⁾	SAMC2 ⁽¹⁾	SAMC1 ⁽¹⁾	SAMC0 ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7 ⁽²⁾	ADCS6 ⁽²⁾	ADCS5 ⁽²⁾	ADCS4 ⁽²⁾	ADCS3 ⁽²⁾	ADCS2 ⁽²⁾	ADCS1 ⁽²⁾	ADCS0 ⁽²⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ADRC:** ADC1 Conversion Clock Source bit

1 = ADC internal RC clock

0 = Clock derived from system clock

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits⁽¹⁾

11111 = 31 TAD

•

•

•

00001 = 1 TAD

00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** ADC1 Conversion Clock Select bits⁽²⁾

11111111 = $T_P \cdot (ADCS<7:0> + 1) = T_P \cdot 256 = T_{AD}$

•

•

•

00000010 = $T_P \cdot (ADCS<7:0> + 1) = T_P \cdot 3 = T_{AD}$

00000001 = $T_P \cdot (ADCS<7:0> + 1) = T_P \cdot 2 = T_{AD}$

00000000 = $T_P \cdot (ADCS<7:0> + 1) = T_P \cdot 1 = T_{AD}$

Note 1: This bit is only used if SSRC<2:0> (AD1CON1<7:5>) = 111 and SSRCG (AD1CON1<4>) = 0.

2: This bit is not used if ADRC (AD1CON3<15>) = 1.

TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)

bit 3-0	Step Command	OPTION<3:0>	Option Description
	PTGWHI ⁽¹⁾ or PTGWLO ⁽¹⁾	0000	PWM Special Event Trigger. ⁽³⁾
		0001	PWM master time base synchronization output. ⁽³⁾
		0010	PWM1 interrupt. ⁽³⁾
		0011	PWM2 interrupt. ⁽³⁾
		0100	PWM3 interrupt. ⁽³⁾
		0101	Reserved.
		0110	Reserved.
		0111	OC1 Trigger event.
		1000	OC2 Trigger event.
		1001	IC1 Trigger event.
		1010	CMP1 Trigger event.
		1011	CMP2 Trigger event.
		1100	CMP3 Trigger event.
		1101	CMP4 Trigger event.
		1110	ADC conversion done interrupt.
		1111	INT2 external interrupt.
	PTGIRQ ⁽¹⁾	0000	Generate PTG Interrupt 0.
		0001	Generate PTG Interrupt 1.
		0010	Generate PTG Interrupt 2.
		0011	Generate PTG Interrupt 3.
		0100	Reserved.
		.	.
		.	.
		1111	Reserved.
	PTGTRIG ⁽²⁾	00000	PTGO0.
		00001	PTGO1.
		.	.
		.	.
		11110	PTGO30.
		11111	PTGO31.

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING
CONTROL REGISTER (CONTINUED)**

bit 3	ABEN: AND Gate B Input Enable bit 1 = MBI is connected to AND gate 0 = MBI is not connected to AND gate
bit 2	ABNEN: AND Gate B Input Inverted Enable bit 1 = Inverted MBI is connected to AND gate 0 = Inverted MBI is not connected to AND gate
bit 1	AAEN: AND Gate A Input Enable bit 1 = MAI is connected to AND gate 0 = MAI is not connected to AND gate
bit 0	AAENEN: AND Gate A Input Inverted Enable bit 1 = Inverted MAI is connected to AND gate 0 = Inverted MAI is not connected to AND gate

REGISTER 25-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **CFSEL<2:0>:** Comparator Filter Input Clock Select bits

111 = T5CLK⁽¹⁾

110 = T4CLK⁽²⁾

101 = T3CLK⁽¹⁾

100 = T2CLK⁽²⁾

011 = Reserved

010 = SYNCO1⁽³⁾

001 = FOSC⁽⁴⁾

000 = Fp⁽⁴⁾

bit 3 **CFLTREN:** Comparator Filter Enable bit

1 = Digital filter is enabled

0 = Digital filter is disabled

bit 2-0 **CFDIV<2:0>:** Comparator Filter Clock Divide Select bits

111 = Clock Divide 1:128

110 = Clock Divide 1:64

101 = Clock Divide 1:32

100 = Clock Divide 1:16

011 = Clock Divide 1:8

010 = Clock Divide 1:4

001 = Clock Divide 1:2

000 = Clock Divide 1:1

Note 1: See the Type C Timer Block Diagram (Figure 13-2).

Note 2: See the Type B Timer Block Diagram (Figure 13-1).

Note 3: See the High-Speed PWMx Module Register Interconnection Diagram (Figure 16-2).

Note 4: See the Oscillator System Diagram (Figure 9-1).

26.3 Programmable CRC Registers

REGISTER 26-1: CRCCON1: CRC CONTROL REGISTER 1

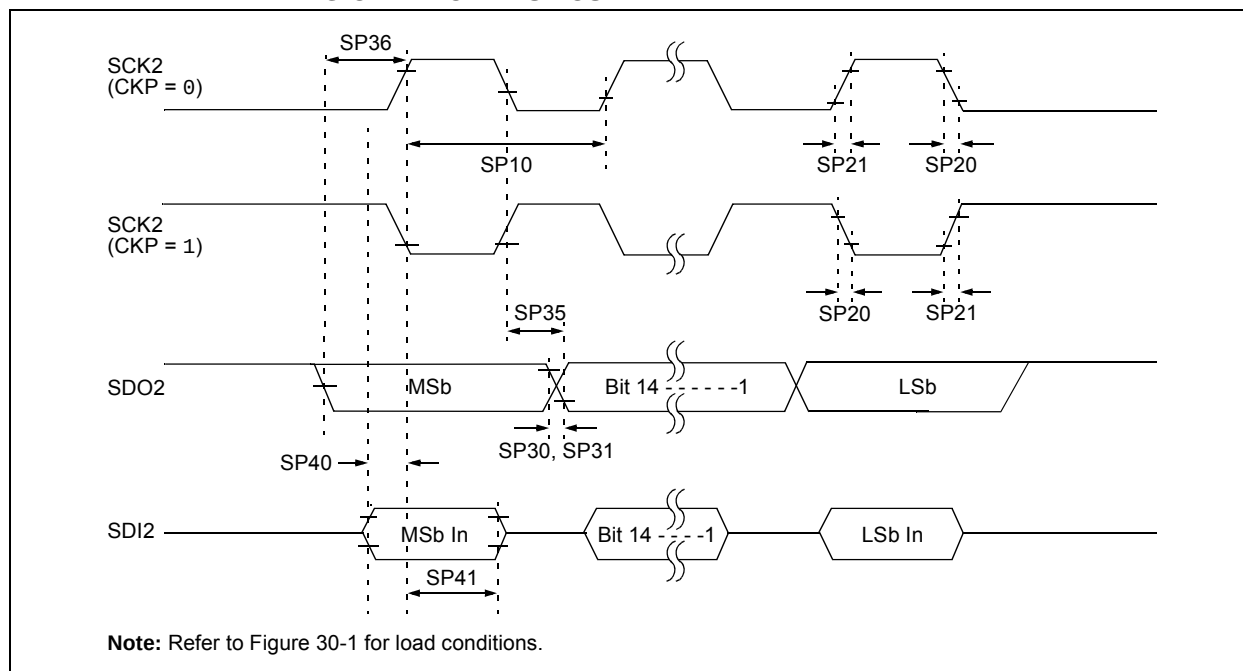
R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0
CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0
bit 15							bit 8
R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **CRCEN:** CRC Enable bit
 1 = CRC module is enabled
 0 = CRC module is disabled; all state machines, pointers and CRCWDAT/CRCDAT are reset, other SFRs are not reset
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **CSIDL:** CRC Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-8 **VWORD<4:0>:** Pointer Value bits
 Indicates the number of valid words in the FIFO. Has a maximum value of 8 when PLEN<4:0> > 7 or 16 when PLEN<4:0> ≤ 7.
- bit 7 **CRCFUL:** CRC FIFO Full bit
 1 = FIFO is full
 0 = FIFO is not full
- bit 6 **CRCMPT:** CRC FIFO Empty Bit
 1 = FIFO is empty
 0 = FIFO is not empty
- bit 5 **CRCISEL:** CRC Interrupt Selection bit
 1 = Interrupt on FIFO is empty; final word of data is still shifting through CRC
 0 = Interrupt on shift is complete and CRCWDAT results are ready
- bit 4 **CRCGO:** Start CRC bit
 1 = Starts CRC serial shifter
 0 = CRC serial shifter is turned off
- bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit
 1 = Data word is shifted into the CRC starting with the LSb (little endian)
 0 = Data word is shifted into the CRC starting with the MSb (big endian)
- bit 2-0 **Unimplemented:** Read as '0'

**FIGURE 30-16: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1)
TIMING CHARACTERISTICS**



**TABLE 30-35: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	(Note 3)
SP20	TscF	SCK2 Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK2 Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2sch, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

31.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40°C to +150°C are identical to those shown in **Section 30.0 “Electrical Characteristics”** for operation between -40°C to +125°C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in **Section 30.0 “Electrical Characteristics”** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias ⁽²⁾	-40°C to +150°C
Storage temperature	-65°C to +160°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to VSS ⁽³⁾	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD < 3.0V ⁽³⁾	-0.3V to 3.6V
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V ⁽³⁾	-0.3V to 5.5V
Maximum current out of VSS pin	60 mA
Maximum current into VDD pin ⁽⁴⁾	60 mA
Maximum junction temperature	+155°C
Maximum current sourced/sunk by any 4x I/O pin	10 mA
Maximum current sourced/sunk by any 8x I/O pin	15 mA
Maximum current sunk by all ports combined	70 mA
Maximum current sourced by all ports combined ⁽⁴⁾	70 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

2: AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time from +125°C to +150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

3: Refer to the “Pin Diagrams” section for 5V tolerant pins.

4: Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

TABLE 31-11: INTERNAL RC ACCURACY

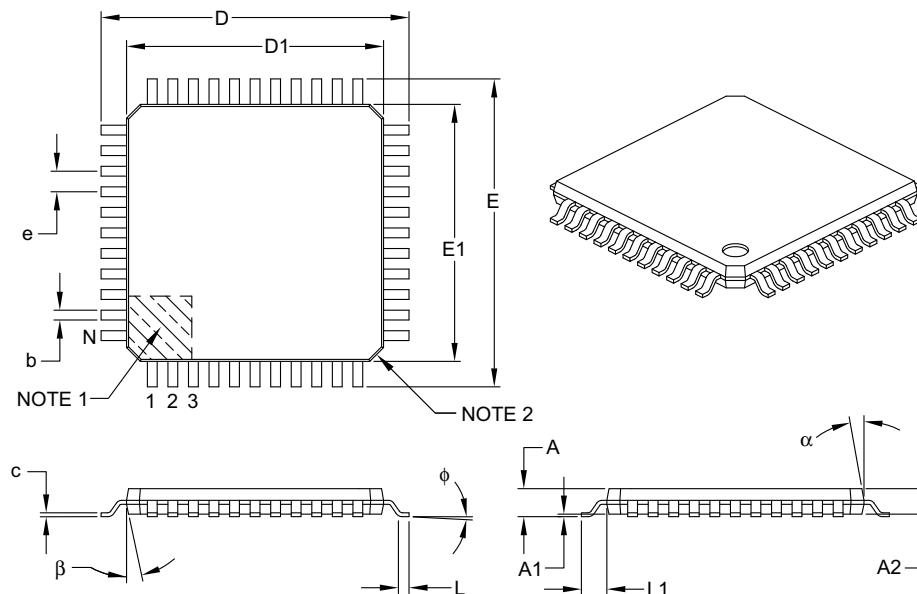
AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
HF21	LPRC @ 32.768 kHz ^(1,2)						
	LPRC	-30	—	+30	%	$-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$	VDD = 3.0-3.6V

Note 1: Change of LPRC frequency as VDD changes.

Note 2: LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT). See **Section 27.5 “Watchdog Timer (WDT)”** for more information.

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	44		
Lead Pitch	e	0.80 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

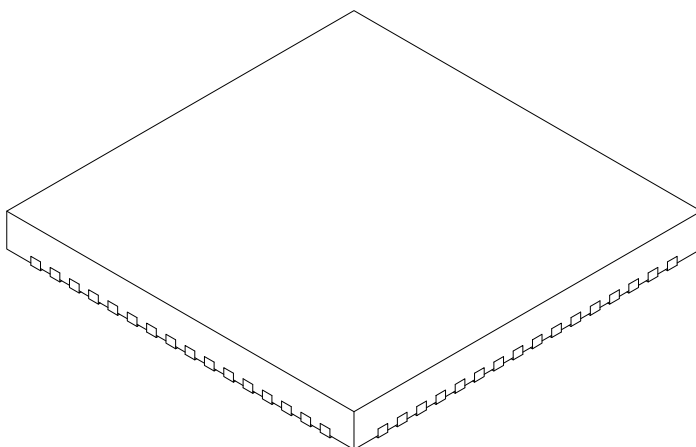
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2

INDEX

A

Absolute Maximum Ratings	401
AC Characteristics	413, 471
10-Bit ADC Conversion Requirements	465
12-Bit ADC Conversion Requirements	463
ADC Module	459
ADC Module (10-Bit Mode)	461, 473
ADC Module (12-Bit Mode)	460, 473
Capacitive Loading Requirements on Output Pins	413
DMA Module Requirements	465
ECANx I/O Requirements	454
External Clock	414
High-Speed PWMx Requirements	422
I/O Timing Requirements	416
I2Cx Bus Data Requirements (Master Mode)	451
I2Cx Bus Data Requirements (Slave Mode)	453
Input Capture x Requirements	420
Internal FRC Accuracy	415
Internal LPRC Accuracy	415
Internal RC Accuracy	472
Load Conditions	413, 471
OCx/PWMx Mode Requirements	421
Op Amp/Comparator Voltage Reference Settling Time Specifications	457
Output Compare x Requirements	421
PLL Clock	415, 471
QE1 External Clock Requirements	423
QE1 Index Pulse Requirements	425
Quadrature Decoder Requirements	424
Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer Requirements	417
SPI1 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) Requirements	441
SPI1 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) Requirements	440
SPI1 Master Mode (Half-Duplex, Transmit Only) Requirements	439
SPI1 Maximum Data/Clock Rate Summary	438
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) Requirements	449
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) Requirements	447
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) Requirements	443
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) Requirements	445
SPI2 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) Requirements	429
SPI2 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) Requirements	428
SPI2 Master Mode (Half-Duplex, Transmit Only) Requirements	427
SPI2 Maximum Data/Clock Rate Summary	426
SPI2 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) Requirements	437
SPI2 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) Requirements	435
SPI2 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) Requirements	431
SPI2 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) Requirements	433

Timer1 External Clock Requirements	418
Timer2/Timer4 External Clock Requirements	419
Timer3/Timer5 External Clock Requirements	419
UARTx I/O Requirements	454
ADC	
Control Registers	325
Helpful Tips	324
Key Features	321
Resources	324
Arithmetic Logic Unit (ALU)	44
Assembler	
MPASM Assembler	398
B	
Bit-Reversed Addressing	115
Example	116
Implementation	115
Sequence Table (16-Entry)	116
Block Diagrams	
Data Access from Program Space	
Address Generation	117
16-Bit Timer1 Module	203
ADC Conversion Clock Period	323
ADC with Connection Options for ANx Pins and Op Amps	322
Arbiter Architecture	110
BEMF Voltage Measurement Using ADC	34
Boost Converter Implementation	32
CALL Stack Frame	111
Comparator (Module 4)	356
Connections for On-Chip Voltage Regulator	384
CPU Core	36
CRC Module	373
CRC Shift Engine	374
CTMU Module	316
Digital Filter Interconnect	357
DMA Controller	141
DMA Controller Module	139
dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X	25
ECAN Module	288
EDS Read Address Generation	105
EDS Write Address Generation	106
Example of MCLR Pin Connections	30
High-Speed PWMx Architectural Overview	227
High-Speed PWMx Register Interconnection	228
I2Cx Module	274
Input Capture x	213
Interleaved PFC	34
Multiphase Synchronous Buck Converter	33
Multiplexing Remappable Output for RPN	180
Op Amp Configuration A	358
Op Amp Configuration B	359
Op Amp/Comparator Voltage Reference Module	356
Op Amp/Comparator x (Modules 1, 2, 3)	355
Oscillator System	153
Output Compare x Module	219
PLL	154
Programmer's Model	38
PTG Module	338
Quadrature Encoder Interface	250
Recommended Minimum Connection	30

Remappable Input for U1RX	176	Memory Map for PIC24EP256GP/MC20X/50X Devices	60
Reset System	123	Memory Map for PIC24EP32GP/MC20X/50X Devices	57
Shared Port Structure	173	Memory Map for PIC24EP512GP/MC20X/50X Devices	61
Single-Phase Synchronous Buck Converter	33	Memory Map for PIC24EP64GP/MC20X/50X Devices	58
SP1x Module	266	Near Data Space	51
Suggested Oscillator Circuit Placement	31	Organization, Alignment	51
Type B Timer (Timer2 and Timer4)	208	SFR Space	51
Type B/Type C Timer Pair (32-Bit Timer)	209	Width	51
Type C Timer (Timer3 and Timer5)	208	Data Memory Arbitration and Bus Master Priority	110
UARTx Module	281	Data Space Extended X	109
User-Programmable Blanking Function	357	Paged Memory Scheme	105
Watchdog Timer (WDT)	385	DC and AC Characteristics Graphs	475
Brown-out Reset (BOR)	384	DC Characteristics BOR	411
C		CTMU Current Source Requirements	458
C Compilers MPLAB XC Compilers	398	Doze Current (IDOE)	407, 469
Charge Time Measurement Unit. See CTMU.		High Temperature	468
Code Examples IC1 Connection to QE11 Input on Pin 43 of dsPIC33EPXXXMC206	176	I/O Pin Input Specifications	408
Port Write/Read	174	I/O Pin Output Specifications	411, 470
PWMx Write-Protected Register Unlock Sequence	226	Idle Current (IDLE)	405, 469
PWRSV Instruction Syntax	163	Op Amp/Comparator Requirements	455
Code Protection	379, 386	Op Amp/Comparator Voltage Reference Requirements	457
CodeGuard Security	379, 386	Operating Current (IDD)	404, 469
Configuration Bits	379	Operating MIPS vs. Voltage	402, 468
Description	381	Power-Down Current (IPD)	406, 469
Configuration Byte Register Map	380	Program Memory	412
Configuring Analog and Digital Port Pins	174	Temperature and Voltage	468
CPU Addressing Modes	35	Temperature and Voltage Specifications	403
Clocking System Options	154	Thermal Operating Conditions	468
Fast RC (FRC) Oscillator	154	Watchdog Timer Delta Current	407
FRC Oscillator with PLL	154	Demo/Development Boards, Evaluation and Starter Kits	400
FRC Oscillator with Postscaler	154	Development Support	397
Low-Power RC (LPRC) Oscillator	154	Third-Party Tools	400
Primary (XT, HS, EC) Oscillator	154	DMA Controller Channel to Peripheral Associations	140
Primary Oscillator with PLL	154	Control Registers	141
Control Registers	40	DMAxCNT	141
Data Space Addressing	35	DMAxCON	141
Instruction Set	35	DMAxPAD	141
Resources	39	DMAxREQ	141
CTMU Control Registers	317	DMAxSTA	141
Resources	316	DMAxSTB	141
Customer Change Notification Service	524	Resources	141
Customer Notification Service	524	Supported Peripherals	139
Customer Support	524	Doze Mode	165
D		DSP Engine	44
Data Address Space	51	E	
Memory Map for dsPIC33EP128MC20X/50X, dsPIC33EP128GP50X Devices	54	ECAN Message Buffers Word 0	310
Memory Map for dsPIC33EP256MC20X/50X, dsPIC33EP256GP50X Devices	55	Word 1	310
Memory Map for dsPIC33EP32MC20X/50X, dsPIC33EP32GP50X Devices	52	Word 2	311
Memory Map for dsPIC33EP512MC20X/50X, dsPIC33EP512GP50X Devices	56	Word 3	311
Memory Map for dsPIC33EP64MC20X/50X, dsPIC33EP64GP50X Devices	53	Word 4	312
Memory Map for PIC24EP128GP/MC20X/50X Devices	59	Word 5	312
		Word 6	313
		Word 7	313