



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gp504-i-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS AND MICROCONTROLLERS

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Familv Reference Manual", which is available from the Microchip web site (www.microchip.com)
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and Vss pins (see Section 2.2 "Decoupling Capacitors")
- All AVDD and AVss pins (regardless if ADC module is not used)

(see Section 2.2 "Decoupling Capacitors")
• VCAP

(see Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)")

- MCLR pin (see Section 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins used for In-Circuit Serial Programming[™] (ICSP[™]) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used

(see Section 2.6 "External Oscillator Pins")

Additionally, the following pins may be required:

• VREF+/VREF- pins are used when external voltage reference for the ADC module is implemented

Note: The AVDD and AVSS pins must be connected, independent of the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: Recommendation of 0.1 μ F (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- Handling high-frequency noise: If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of $0.01 \ \mu\text{F}$ to $0.001 \ \mu\text{F}$. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, $0.1 \ \mu\text{F}$ in parallel with $0.001 \ \mu\text{F}$.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.





TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC35	0886	_		JTAGIP<2:()>	—		ICDIP<2:0	>	_	—	—	—	—	_	—	—	4400
IPC36	0888			PTG0IP<2:0)>	—	PT	GWDTIP<	2:0>		P	TGSTEPIP<2	:0>	—	—		—	4440
IPC37	088A		_		_	—	F	PTG3IP<2:)>			PTG2IP<2:0	>	—	F	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	_	_				—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4		—		_	_	_				—	DAE	DOOVR	—	—		—	0000
INTCON4	08C6		—		_	_	_				—	—	—	—	—		SGHT	0000
INTTREG	08C8	_	_	_	_		ILR<	3:0>					VECNU	M<7:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-33:	: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC20X DEVIC	ES ONLY
-------------	--	---------

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—				INT1R<6:0>	•			—	_	—	—	—	—	—	_	0000
RPINR1	06A2	_	_	_	_	_	_	_	—	_				INT2R<6:0>	`			0000
RPINR3	06A6	_		_	_	_	_	_	—	_			-	[2CKR<6:0	>			0000
RPINR7	06AE	_				IC2R<6:0>				_				IC1R<6:0>				0000
RPINR8	06B0	_				IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6	_	_	—	—	—	—	_	—	_			(DCFAR<6:0	>			0000
RPINR12	06B8	_		FLT2R<6:0>						_				FLT1R<6:0>	>			0000
RPINR14	06BC	_			(QEB1R<6:0	>			_			(QEA1R<6:0	>			0000
RPINR15	06BE	_			Н	OME1R<6:0)>			_	INDX1R<6:0>							0000
RPINR18	06C4	_	_	_	_	_	_	_	_	_			ι	J1RXR<6:0	>			0000
RPINR19	06C6	_	_	_	_	_	_	_	—	_			ι	J2RXR<6:0	>			0000
RPINR22	06CC	_		•	S	CK2INR<6:0)>	•	•	_				SDI2R<6:0>	>			0000
RPINR23	06CE	_	_	—	—	—	—	_	_	_							0000	
RPINR37	06EA	_		SYNCI1R<6:0>												0000		
RPINR38	06EC	_		DTCMP1R<6:0>						_	·					_	0000	
RPINR39	06EE	_		DTCMP3R<6:0>								D	CMP2R<6:	0>			0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-37: PMD REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	-	-	-	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	AD1MD	0000
PMD2	0762	_	_	—	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	_	-	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	CRCMD	_	_	_	_	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	_	_	_	_	_	_	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
													DMA0MD					
	0760												DMA1MD	DTCMD				0000
PIVID7	0760	_	_	_	_	_	_	_	_	_	_	_	DMA2MD	PIGMD	_	_	_	0000
													DMA3MD					

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-38: PMD REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	_	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	_	_	AD1MD	0000
PMD2	0762	_	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	_	—		OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	CRCMD	_	_	_	_	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	_	_	_	_	_	_	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	_	_	PWM3MD	PWM2MD	PWM1MD	_	_	_	_	_	_	_	_	0000
													DMA0MD					
	0760												DMA1MD	DTCMD				0000
FIND	0/00	_	_	_	_	_	_	_	_	_	_	_	DMA2MD	FIGND	_	_		0000
													DMA3MD					1

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.4 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating of the Stack Pointer (for example, creating stack frames).

Note:	То	protec	t	agains	st	misal	lign	ed	st	ack
	acc	esses,	W	15<0>	is	fixed	to	'0'	by	the
	hard	dware.								

W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

The Software Stack Pointer always points to the first available free word and fills the software stack working from lower toward higher addresses. Figure 4-19 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-19. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

- **Note 1:** To maintain system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).
 - 2: As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment

FIGURE 4-19: CALL STACK FRAME



dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

		11.0	11.0		11.0		
		0-0	0-0	VREGSE	0-0		VREGS
hit 15		—		VNEGSF	—	Civi	bit 8
bit 10							Dit 0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
bit 7						.1	bit 0
Legend:							
R = Reada	able bit	W = Writable I	oit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	TRAPR: Trap	Reset Flag bit					
	$1 = A \operatorname{Trap} Co$	onflict Reset ha	s occurred	d			
hit 11			s not occurre		ot Elog bit		
DIL 14	1 = An illega	l oncode deter	viinniiaiizeu	v Access Res	et Flay Dit ode or Uninitial	lized W registe	er used as an
	Address	Pointer caused	a Reset			ized w regiote	
	0 = An illegal	l opcode or Uni	nitialized W r	egister Reset h	as not occurred	t	
bit 13-12	Unimplemen	ted: Read as 'o)'				
bit 11	VREGSF: Fla	ish Voltage Reg	ulator Stand	by During Slee	p bit		
	1 = Flash vol	tage regulator i	s active durin	ng Sleep			
bit 10		tage regulator (naby mode dui	ing Sleep		
bit Q	CM: Configur	ation Mismatch	, Elac bit				
bit 5	1 = A Configur	ration Mismatch	h Reset has	occurred			
	0 = A Configu	ration Mismatc	h Reset has	not occurred			
bit 8	VREGS: Volta	age Regulator S	Standby Durii	ng Sleep bit			
	1 = Voltage r	egulator is activ	e during Sle	ер			
	0 = Voltage r	egulator goes in	nto Standby i	mode during SI	еер		
bit 7	EXTR: Extern	nal Reset (MCL	R) Pin bit				
	\perp = A Master 0 = A Master	Clear (pin) Res Clear (pin) Res	et has occur et has not or	rea ccurred			
bit 6	SWR: Softwa	re RESET (Instr	uction) Flag	bit			
	1 = A reset	instruction has	been execut	ed			
	0 = A RESET	instruction has	not been exe	ecuted			
bit 5	SWDTEN: So	oftware Enable/	Disable of W	DT bit ⁽²⁾			
	1 = WDT is er	nabled					
bit 4		ISADIEU hdog Timor Tim	o out Elog b	:+			
DIL 4	1 = WDT time		e-oul Flay D	IL			
	0 = WDT time	e-out has not oc	curred				
Note 1.	All of the Peset sta	itus hits can bo	set or cleare	d in software S	Setting one of th	ese hits in soft	vara does not
	cause a device Re	set.					
2:	If the FWDTEN Co SWDTEN bit settin	onfiguration bit i	s '1' (unprog	rammed), the V	VDT is always e	enabled, regard	less of the

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

FIGURE 7-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X INTERRUPT VECTOR TABLE



Internut Course	Vector	IRQ		Inte	errupt Bit L	ocation
Interrupt Source	#	#	IVI Address	Flag	Enable	Priority
	Highe	est Natura	al Order Priority			
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
IC1 – Input Capture 1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
OC1 – Output Compare 1	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
T1 – Timer1	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
IC2 – Input Capture 2	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>
OC2 – Output Compare 2	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
T2 – Timer2	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
T3 – Timer3	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1E – SPI1 Error	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 – SPI1 Transfer Done	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
AD1 – ADC1 Convert Done	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
DMA1 – DMA Channel 1	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
Reserved	23	15	0x000032	_	_	_
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
CM – Comparator Combined Event	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
CN – Input Change Interrupt	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
INT1 – External Interrupt 1	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
Reserved	29-31	21-23	0x00003E-0x000042	_	_	_
DMA2 – DMA Channel 2	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
OC3 – Output Compare 3	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
OC4 – Output Compare 4	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
T4 – Timer4	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
T5 – Timer5	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
SPI2E – SPI2 Error	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 – SPI2 Transfer Done	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>
C1RX – CAN1 RX Data Ready ⁽¹⁾	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
C1 – CAN1 Event ⁽¹⁾	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
DMA3 – DMA Channel 3	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
IC3 – Input Capture 3	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
IC4 – Input Capture 4	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
Reserved	47-56	39-48	0x000062-0x000074	—	—	_
SI2C2 – I2C2 Slave Event	57	49	0x000076	IFS3<1>	IEC3<1>	IPC12<6:4>
MI2C2 – I2C2 Master Event	58	50	0x000078	IFS3<2>	IEC3<2>	IPC12<10:8>
Reserved	59-64	51-56	0x00007A-0x000084			
PSEM – PWM Special Event Match ⁽²⁾	65	57	0x000086	IFS3<9>	IEC3<9>	IPC14<6:4>

TABLE 7-1: INTERRUPT VECTOR DETAILS

Note 1: This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

2: This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	-	_	_	—	_	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				OCFAR<6:0>	>		
bit 7	-						bit 0
Legend:							

REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 Unimplemented: Read as '0'

bit 6-0 OCFAR<6:0>: Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121

> . 0000001 = Input tied to CMP1 0000000 = Input tied to Vss

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—			RP57	R<5:0>		
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—			RP56	R<5:0>		
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimplem	nented bit, rea	d as '0'	
-n = Value a	t POR	'1' = Bit is set	t	'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-14	Unimpleme	nted: Read as '	0'				
bit 13-8	RP57R<5:0> (see Table 1 [*]	 Peripheral Out 1-3 for peripheral 	utput Functior al function nu	n is Assigned to mbers)	RP57 Output	Pin bits	
bit 7-6	Unimpleme	nted: Read as '	0'				

REGISTER 11-24: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

(see Table	11-3 for peripheral function numbers)	

REGISTER 11-25: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—	—		RP97R<5:0>						
bit 15							bit 8		

RP56R<5:0>: Peripheral Output Function is Assigned to RP56 Output Pin bits

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8 **RP97R<5:0>:** Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-0 Unimplemented: Read as '0'

bit 5-0

15.0 OUTPUT COMPARE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual" for OCxR and OCxRS register restrictions.





REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)

- bit 3 TRIGMODE: Trigger Status Mode Select bit
 - 1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
 - 0 = TRIGSTAT is cleared only by software
- bit 2-0 OCM<2:0>: Output Compare x Mode Select bits
 - 111 = Center-Aligned PWM mode: Output set high when OCxTMR = OCxR and set low when OCxTMR = OCxRS⁽¹⁾
 - 110 = Edge-Aligned PWM mode: Output set high when OCxTMR = 0 and set low when OCxTMR = OCxR⁽¹⁾
 - 101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS
 - 100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle
 - 011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin
 - 010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low
 - 001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high
 - 000 = Output compare channel is disabled
- Note 1: OCxR and OCxRS are double-buffered in PWM mode only.
 - 2: Each Output Compare x module (OCx) has one PTG clock source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.
 - PTGO4 = OC1PTGO5 = OC2
 - PTGO6 = OC3 PTGO7 = OC4

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC	
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	
bit 15							bit 8	
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	
bit 7							bit 0	
Legend:		C = Clearable bit		HS = Hardware Settable bit		HSC = Hardware Settable/Clearable bit		
R = Readab	le bit	W = Writable	e bit	U = Unimplen	nented bit, read	as '0'		
-n = Value at POR		'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknown		

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

bit 15	ACKSTAT: Acknowledge Status bit (when operating as I^2C^{TM} master, applicable to master transmit operation)
	1 = NACK received from slave 0 = ACK received from slave
	Hardware is set or clear at the end of slave Acknowledge.
bit 14	TRSTAT: Transmit Status bit (when operating as I^2C master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK)
	0 = Master transmit is not in progress Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
bit 13-11	Unimplemented: Read as '0'
bit 10	BCL: Master Bus Collision Detect bit
	1 = A bus collision has been detected during a master operation0 = No bus collision detected
	Hardware is set at detection of a bus collision.
bit 9	GCSTAT: General Call Status bit
	1 = General call address was received
	0 = General call address was not received
1.1.0	Hardware is set when address matches general call address. Hardware is clear at Stop detection.
DIT 8	ADD10: 10-Bit Address Status bit
	I = 10-bit address was matched 0 = 10-bit address was not matched
	Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
bit 7	IWCOL: I2Cx Write Collision Detect bit
~	1 = An attempt to write to the I2CxTRN register failed because the I^2 C module is busy 0 = No collision
	Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
bit 6	I2COV: I2Cx Receive Overflow Flag bit
	 1 = A byte was received while the I2CxRCV register was still holding the previous byte 0 = No overflow
	Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
bit 5	D_A: Data/Address bit (when operating as I ² C slave)
	1 = Indicates that the last byte received was data
	 Indicates that the last byte received was a device address Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.

REGISTER 20-1: UXMODE: UARTX MODE REGISTER (CONTINUED)

bit 5	ABAUD: Auto-Baud Enable bit
	 1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion 0 = Baud rate measurement is disabled or completed
bit 4	URXINV: UARTx Receive Polarity Inversion bit
	1 = UxRX Idle state is '0' 0 = UxRX Idle state is '1'
bit 3	BRGH: High Baud Rate Enable bit
	 1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode) 0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
bit 2-1	PDSEL<1:0>: Parity and Data Selection bits
	 11 = 9-bit data, no parity 10 = 8-bit data, odd parity 01 = 8-bit data, even parity 00 = 8-bit data, no parity
bit 0	STSEL: Stop Bit Selection bit
	1 = Two Stop bits 0 = One Stop bit
Note 1:	Refer to the " UART " (DS70582) section in the "dsPIC33/PIC24 Family Reference Manual" for information on enabling the UARTx module for receive or transmit operation.

- 2: This feature is only available for the 16x BRG mode (BRGH = 0).
- 3: This feature is only available on 44-pin and 64-pin devices.
- 4: This feature is only available on 64-pin devices.

21.4 ECAN Control Registers

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0		
		CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0		
bit 15				·			bit 8		
R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0		
OPMODE2	OPMODE1	OPMODE0		CANCAP	—		WIN		
bit 7							bit 0		
[
Legend:									
		'1' = Bit is set	JIL	$0^{\circ} = \text{Bit is closed}$	ared	v – Bitis unkr			
		I - DILIS SEL			aleu		IOWIT		
bit 15-14	Unimplemen	ted: Read as '()'						
bit 13	CSIDL: ECAN	Nx Stop in Idle I	Mode bit						
	1 = Discontin	ues module ope	eration when	device enters I	dle mode				
	0 = Continues	s module opera	tion in Idle m	ode					
bit 12	ABAT: Abort	All Pending Tra	nsmissions b	it					
	1 = Signals al	I transmit buffe	rs to abort tra when all tran	ansmission smissions are a	aborted				
bit 11		CANx Module C	lock (ECAN) S	Source Select b	bit				
2	1 = FCAN is e	qual to 2 * FP							
	0 = FCAN is e	qual to FP							
bit 10-8	REQOP<2:0>	Request Ope	ration Mode	bits					
	111 = Set Lis	ten All Messag	es mode						
	101 = Reserv	red							
	100 = Set Co	nfiguration mod	le						
	011 = Set Lis	ten Only mode							
	001 = Set Dis	able mode							
	000 = Set No	rmal Operation	mode						
bit 7-5	OPMODE<2:	0> : Operation N	/lode bits						
	111 = Module	e is in Listen All	Messages m	node					
	110 = Reserv 101 = Reserv	red red							
	100 = Module	e is in Configura	ation mode						
	011 = Module	e is in Listen Or	ly mode						
	010 = Module	e is in Loopback s is in Disable n	k mode node						
	000 = Module	e is in Normal C	peration mod	de					
bit 4	Unimplemen	ted: Read as 'd)'						
bit 3	CANCAP: CA	AN Message Re	eceive Timer	Capture Event	Enable bit				
	1 = Enables in 0 = Disables (nput capture ba CAN capture	sed on CAN	message recei	ive				
bit 2-1	Unimplemen	ted: Read as '()'						
bit 0	WIN: SFR Ma	ap Window Sele	ect bit						
	1 = Uses filter	r window							
	0 = Uses buff	er window							

25.0 OP AMP/COMPARATOR MODULE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP/MC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Op Amp/Comparator" (DS70357) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices contain up to four comparators, which can be configured in various ways. Comparators, CMP1, CMP2 and CMP3, also have the option to be configured as op amps, with the output being brought to an external pin for gain/filtering connections. As shown in Figure 25-1, individual comparator options are specified by the comparator module's Special Function Register (SFR) control bits.

Note: Op Amp/Comparator 3 is not available on the dsPIC33EPXXXGP502/MC502/MC202 and PIC24EP256GP/MC202 (28-pin) devices.

These options allow users to:

- · Select the edge for trigger and interrupt generation
- · Configure the comparator voltage reference
- · Configure output blanking and masking
- Configure as a comparator or op amp (CMP1, CMP2 and CMP3 only)

Note: Not all op amp/comparator input/output connections are available on all devices. See the "Pin Diagrams" section for available connections.

FIGURE 25-1: OP AMP/COMPARATOR x MODULE BLOCK DIAGRAM (MODULES 1, 2 AND 3)



АС СНА	RACTER	ISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic ⁽⁴⁾		Min. ⁽¹⁾	Max.	Units	Conditions	
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Tcy/2 (BRG + 2)	_	μS		
			400 kHz mode	TCY/2 (BRG + 2)	—	μS		
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	_	μS		
IM11	THI:SCL	Clock High Time	100 kHz mode	Tcy/2 (BRG + 2)	_	μS		
			400 kHz mode	Tcy/2 (BRG + 2)	_	μs		
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	_	μs		
IM20	TF:SCL	SDAx and SCLx	100 kHz mode	_	300	ns	CB is specified to be	
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF	
			1 MHz mode ⁽²⁾	_	100	ns		
IM21	TR:SCL	SDAx and SCLx	100 kHz mode		1000	ns	CB is specified to be	
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF	
			1 MHz mode ⁽²⁾		300	ns		
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	_	ns		
			400 kHz mode	100	_	ns		
			1 MHz mode ⁽²⁾	40	—	ns		
IM26	THD:DAT	Data Input	100 kHz mode	0	_	μS		
		Hold Time	400 kHz mode	0	0.9	μS		
			1 MHz mode ⁽²⁾	0.2	_	μS		
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	Tcy/2 (BRG + 2)	_	μS	Only relevant for	
			400 kHz mode	Tcy/2 (BRG + 2)	_	μS	Repeated Start	
			1 MHz mode ⁽²⁾	TCY/2 (BRG + 2)	_	μS	condition	
IM31	THD:STA	Start Condition	100 kHz mode	Tcy/2 (BRG + 2)	_	μs	After this period, the	
		Hold Time	400 kHz mode	Tcy/2 (BRG +2)	_	μS	first clock pulse is	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	_	μS	generated	
IM33	Tsu:sto	Stop Condition	100 kHz mode	Tcy/2 (BRG + 2)	_	μs		
		Setup Time	400 kHz mode	Tcy/2 (BRG + 2)	_	μs		
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	_	μS		
IM34	THD:STO	Stop Condition	100 kHz mode	Tcy/2 (BRG + 2)	—	μs		
		Hold Time	400 kHz mode	Tcy/2 (BRG + 2)	_	μs		
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	_	μS		
IM40	TAA:SCL	Output Valid	100 kHz mode	_	3500	ns		
		From Clock	400 kHz mode		1000	ns		
			1 MHz mode ⁽²⁾	_	400	ns		
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be	
			400 kHz mode	1.3	_	μs	free before a new	
			1 MHz mode ⁽²⁾	0.5	_	μs	transmission can start	
IM50	Св	Bus Capacitive L	oading	—	400	pF		
IM51	Tpgd	Pulse Gobbler De	elay	65	390	ns	(Note 3)	

TABLE 30-49: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

Note 1: BRG is the value of the l²C[™] Baud Rate Generator. Refer to "Inter-Integrated Circuit (l²C[™])" (DS70330) in the "dsPIC33/PIC24 Family Reference Manual". Please see the Microchip web site for the latest family reference manual sections.

- 2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).
- **3:** Typical value for this parameter is 130 ns.
- 4: These parameters are characterized, but not tested in manufacturing.

32.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 32-1: VOH – 4x DRIVER PINS VOH (V) -0.050 -0.045 3.6V -0.040 3.3V -0.035 3V -0.030 IOH(A) -0.025 -0.020 Absolute Maximum -0.015 -0.010 -0.005 0.000 0.50 1.00 2.00 2.50 3.00 3.50 0.00 1.50 4.00

FIGURE 32-2: VOH – 8x DRIVER PINS





FIGURE 32-4: Vol – 8x DRIVER PINS



Note the following details of the code protection feature on Microchip devices:

- · Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV == ISO/TS 16949 ==

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rfPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rfLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2011-2013, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN: 9781620773949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEEL0Q® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and mulfacture of development systems is ISO 9001:2000 certified.