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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8×8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gp504t-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



TABLE 4-27: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC204/504 AND PIC24EPXXXGP/MC204 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
RPOR0	0680				RP35R<5:0>					_	_		RP20R<5:0> 00						
RPOR1	0682	—	—		RP37R<5:0>					—			RP36R<5:0> 000						
RPOR2	0684	—	—		RP39R<5:0>					_	_			RP38	R<5:0>			0000	
RPOR3	0686	_	_			RP41	R<5:0>			—	_			RP40	R<5:0>			0000	
RPOR4	0688	_	_		RP43R<5:0>					—	_	RP42R<5:0>					0000		
RPOR5	068A	_	_		RP55R<5:0>				—	_			RP54	R<5:0>			0000		
RPOR6	068C	_	_		RP57R<5:0>				_	—			RP56	R<5:0>			0000		

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-28: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC206/506 AND PIC24EPXXXGP/MC206 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—			RP35	R<5:0>			_	_			RP20I	R<5:0>			0000
RPOR1	0682	_	_			RP37	R<5:0>			_	_			RP36	R<5:0>			0000
RPOR2	0684	_	_			RP39	R<5:0>			—	—			RP38	R<5:0>			0000
RPOR3	0686	_	_		RP41R<5:0>				—	—			RP40	R<5:0>			0000	
RPOR4	0688	_	_		RP43R<5:0>				—	—			RP42I	R<5:0>			0000	
RPOR5	068A	_	_		RP55R<5:0> — ·				—	RP54R<5:0>					0000			
RPOR6	068C	_	_		RP57R<5:0> — — RP56R<5:0>							0000						
RPOR7	068E	_	_			RP97	R<5:0>			—	—	_	_	_	_	_	_	0000
RPOR8	0690	_	_			RP118	R<5:0>			—	—	_	_	_	_	_	_	0000
RPOR9	0692	_	_	_	_	_	_	_	_	_	_			RP120	R<5:0>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 8-3: DMAXSTAH: DMA CHANNEL X START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—		—	—	—	—	—	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STA<	23:16>			
bit 7							bit 0
Legend:							
R = Readable b	it	W = Writable bi	t	U = Unimplei	mented bit read	d as '0'	

•••			-		
-n =	= Value at POR	'1' = Bit is set	'0' =	Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 STA<23:16>: Primary Start Address bits (source or destination)

REGISTER 8-4: DMAXSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STA	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STA	<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at P	' OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unki	nown

bit 15-0 STA<15:0>: Primary Start Address bits (source or destination)

REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_	—	—	_	—	—	—
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSADR	<23:16>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable bi	t	U = Unimpler	mented bit, read	as '0'	

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 DSADR<23:16>: Most Recent DMA Address Accessed by DMA bits

REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSAI	DR<15:8>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable bit		U = Unimplemer	nted bit, re	ad as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleare	d	x = Bit is unknown	

bit 15-0 DSADR<15:0>: Most Recent DMA Address Accessed by DMA bits

INE OID LEN	10-5. I MD5						
U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
	—	—	—	—	CMPMD	—	—
bit 15							bit 8
R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
CRCMD	—	—	—	—	—	I2C2MD	—
bit 7		•				•	bit 0
Legend:							
R = Readable	e bit	W = Writable I	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown
bit 15-11	Unimplement	ted: Read as 'o)'				

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

bit 10	CMPMD: Comparator Module Disable bit
	1 = Comparator module is disabled
	0 = Comparator module is enabled
bit 9-8	Unimplemented: Read as '0'
bit 7	CRCMD: CRC Module Disable bit
	1 = CRC module is disabled
	0 = CRC module is enabled
bit 6-2	Unimplemented: Read as '0'
bit 1	I2C2MD: I2C2 Module Disable bit
	1 = I2C2 module is disabled
	0 = I2C2 module is enabled
bit 0	Unimplemented: Read as '0'

REGISTER 10-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—		—	—
						bit 8
U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
	—	—	REFOMD	CTMUMD	—	—
		•	•			bit 0
	U-0 — U-0 —	U-0 U-0 — — U-0 U-0 — —	U-0 U-0 U-0 — — — — U-0 U-0 U-0 — — — —	U-0 U-0 U-0 U-0 	U-0 U-0 U-0 U-0 - - - - - U-0 U-0 U-0 U-0 - U-0 U-0 U-0 R/W-0 R/W-0 - - - REFOMD CTMUMD	U-0 U-0 U-0 U-0 U-0 - - - - - - U-0 U-0 U-0 U-0 U-0 - U-0 U-0 U-0 R/W-0 U-0 - U-0 U-0 R/W-0 R/W-0 U-0 - - - REFOMD CTMUMD -

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4	Unimplemented: Read as '0'
bit 3	REFOMD: Reference Clock Module Disable bit
	1 = Reference clock module is disabled
	0 = Reference clock module is enabled
bit 2	CTMUMD: CTMU Module Disable bit
	1 = CTMU module is disabled
	0 = CTMU module is enabled
bit 1-0	Unimplemented: Read as '0'

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r							
R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8
R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIC	G TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0
bit 7							bit 0
r							
Legend:		HS = Hardwa	ire Settable bit				
R = Reada	able bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value	at POR	'1' = Bit is set	['0' = Bit is clea	ared	x = Bit is unkn	own
bit 15	FLTMD: Fault	Mode Select I	bit				
	1 = Fault mo	de is maintain	ed until the Fa	ault source is r	removed; the c	orresponding	OCFLTx bit is
	cleared in	n software and	a new PWM pe	eriod starts	loved and a po	N DWM poriod	etarte
hit 14							Starts
DIL 14	1 = PWM out	nut is driven h	iah on a Fault				
	0 = PWM out	put is driven lo	w on a Fault				
bit 13	FLTTRIEN: Fa	ault Output Sta	ate Select bit				
	1 = OCx pin i	s tri-stated on	a Fault conditio	on			
	0 = OCx pin I	/O state is def	ined by the FLT	OUT bit on a F	ault condition		
bit 12	OCINV: Outpu	ut Compare x I	nvert bit				
	1 = OCx outp	out is inverted	bo				
hit 11_9		ted: Read as '	0'				
bit 8	OC32. Casca	de Two OCx M	° Iodules Enable	hit (32-hit oper	ration)		
bit 0	1 = Cascade	module opera	tion is enabled		allony		
	0 = Cascade	module opera	tion is disabled				
bit 7	OCTRIG: Out	put Compare >	k Trigger/Sync S	Select bit			
	1 = Triggers (0 = Synchron	OCx from the s izes OCx with	source designat the source des	ted by the SYN	CSELx bits SYNCSELx bit	s	
bit 6	TRIGSTAT: Ti	mer Trigger St	atus bit	0 ,			
	1 = Timer sou	urce has been	triggered and is	s running			
	0 = Timer sou	urce has not be	een triggered a	nd is being held	d clear		
bit 5	OCTRIS: Out	put Compare x	Coutput Pin Dir	ection Select b	it		
	1 = OCx is tri	-stated					
		ompare x mod	ule drives the C	DCx pin			
Note 1:	Do not use the O	Cx module as i	its own Synchro	nization or Trig	ger source.		
2:	When the OCy module as a Trigg	odule is turned jer source, the	l OFF, it sends a OCy module m	a trigger out sig nust be unseled	gnal. If the OCx	module uses t source prior	he OCy to disabling it.
3:	Each Output Com	ipare x module	e (OCx) has one	e PTG Trigger/S	Synchronization	n source. See S	Section 24.0
	PTGO0 = OC1	Jei Generator			malion.		
	PTGO1 = OC2						
	PTGO2 = OC3						
	PTGO3 = OC4						

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

REGISTER 16-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'			
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			

bit 15-0 **PDCx<15:0>:** PWMx Generator # Duty Cycle Value bits

REGISTER 16-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	Ex<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	SEx<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable bit U = Unimplemented bit, read as '0'			ad as '0'		
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknow			nown

bit 15-0 PHASEx<15:0>: PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs

 If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			TRGC	/IP<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			TRGC	MP<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unkno		nown	

REGISTER 16-14: TRIGX: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

bit 15-0 TRGCMP<15:0>: Trigger Control Value bits

When the primary PWMx functions in local time base, this register contains the compare values that can trigger the ADC module.

REGISTER 17-19: INT1HLDH: INTERVAL 1 TIMER HOLD HIGH WORD REGIS	TER
---	-----

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTHL	D<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTHL	D<23:16>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'			d as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	t is cleared x = Bit is unknown		nown

bit 15-0 INTHLD<31:16>: Hold Register for Reading and Writing INT1TMRH bits

REGISTER 17-20: INT1HLDL: INTERVAL 1 TIMER HOLD LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTHL	D<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTH	_D<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'				d as '0'			
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	y' = Bit is cleared x = Bit is unknown		nown

bit 15-0 INTHLD<15:0>: Hold Register for Reading and Writing INT1TMRL bits

REGISTER 18-1: SPIx STAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 1 SPITBF: SPIx Transmit Buffer Full Status bit
 - 1 = Transmit not yet started, SPIxTXB is full
 - 0 = Transmit started, SPIxTXB is empty

Standard Buffer mode:

Automatically set in hardware when core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer mode:

Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 SPIRBF: SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full

0 = Receive is incomplete, SPIxRXB is empty

Standard Buffer mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 6	STREN: SCLx Clock Stretch Enable bit (when operating as I ² C slave) Used in conjunction with the SCLREL bit. 1 = Enables software or receives clock stretching 0 = Disables software or receives clock stretching
bit 5	ACKDT: Acknowledge Data bit (when operating as I ² C master, applicable during master receive)
	Value that is transmitted when the software initiates an Acknowledge sequence. 1 = Sends NACK during Acknowledge 0 = Sends ACK during Acknowledge
bit 4	ACKEN: Acknowledge Sequence Enable bit (when operating as I ² C master, applicable during master receive)
	 1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit. Hardware is clear at the end of the master Acknowledge sequence. 0 = Acknowledge sequence is not in progress
bit 3	RCEN: Receive Enable bit (when operating as I ² C master)
	 1 = Enables Receive mode for I²C. Hardware is clear at the end of the eighth bit of the master receive data byte. a Receive acquirement in program.
hit 2	0 = Receive sequence is not in progress
511 2	 1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of the master Stop sequence. a Stop condition is not in processor.
h :+ 4	0 = Stop condition is not in progress
DIT	RSEN: Repeated Start Condition Enable bit (when operating as I-C master)
	 Initiates Repeated Start condition on SDAx and SCLX pins. Hardware is clear at the end of the master Repeated Start sequence. 0 = Repeated Start condition is not in progress
bit 0	SEN: Start Condition Enable bit (when operating as l^2C master)
	 1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Start sequence. 0 = Start condition is not in progress

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

RXOVF4

bit 7			bit 0
Legend:	C = Writable bit, but or	nly '0' can be written to clear the bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	

RXOVF3

RXOVF2

R = Readable bit	vv = vvritable bit	U = Unimplemented bit, read	as 0
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 RXOVF<15:0>: Receive Buffer n Overflow bits

RXOVF6

RXOVF7

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

RXOVF5

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 RXOVF<31:16>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

RXOVF0

RXOVF1

REGISTER 2	5-3: CM4C	ON: COMPA	RATOR 4 CO	ONTROL RE	GISTER		
R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
CON	COE	CPOL	_		_	CEVT	COUT
bit 15							bit 8
R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0		CREF ⁽¹⁾			CCH1 ⁽¹⁾	CCH0 ⁽¹⁾
bit 7	•		1				bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	iown
bit 15	CON: Compa	rator Enable bi	t				
	1 = Comparat	tor is enabled					
	0 = Comparat	tor is disabled					
bit 14	COE: Compa	rator Output Er	hable bit				
	1 = Comparat	tor output is pre	esent on the C	xOUT pin			
bit 12		orator Output IS Inte	elliai Uliiy Dolority Soloot	hit			
DIL 13	1 = Comparat	tor output is inv		DI			
	0 = Comparat	tor output is not	t inverted				
bit 12-10	Unimplemen	ted: Read as '	כ'				
bit 9	CEVT: Compa	arator Event bit					
	1 = Compara	tor event acco	ording to EVF	POL<1:0> sett	ings occurred;	disables future	triggers and
	interrupts	s until the bit is	cleared				
hit 0		areter Output h					
DILO	When CPOL	= 0 (non-invert	nt ad polarity):				
	1 = VIN + > VII	<u>- 0 (11011-1117C110</u> N-	cu polanty).				
	0 = VIN + < VII	N-					
	When CPOL	= 1 (inverted po	olarity):				
	1 = VIN + < VII	N-					
bit 7-6		• Trigger/Event		arity Salact hits	e		
bit 7-0	11 = Trigger/e	event/interrupt	denerated on	any change of	, f the comparato	r output (while (CEVT = 0
	10 = Trigger/e output (v	event/interrupt g while CEVT = 0	generated only)	on high-to-low	v transition of the	e polarity selecte	ed comparator
	<u>If CPOL</u> Low-to-ł	= 1 (inverted p nigh transition o	olarity): of the compara	ator output.			
	<u>If CPOL</u> High-to-	= 0 (non-inver low transition o	<u>ted polarity):</u> f the compara	ator output.			
	01 = Trigger/e output (v	event/interrupt g while CEVT = 0	generated only)	on low-to-high	transition of the	e polarity selecte	ed comparator
	If CPOL High-to-	= 1 (inverted p low transition o	olarity): f the compara	ator output.			
	<u>If CPOL</u> Low-to-t	= 0 (non-inver	ted polarity): of the compara	ator output.			
	00 = Trigger/e	event/interrupt	generation is	disabled			
				(1.1.1.) / O	() (() () () () () () () () () () () () () ()		

Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.



FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch		0.65 BSC		
Contact Pad Spacing	С		7.20	
Contact Pad Width (X28)			0.45	
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units			S
Dimension	Dimension Limits			MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX			
Number of Pins	N		44				
Pitch	е		0.65 BSC				
Overall Height	A	0.80	0.90	1.00			
Standoff	A1	0.00	0.02	0.05			
Terminal Thickness	A3		0.20 REF				
Overall Width	E		8.00 BSC				
Exposed Pad Width	E2	6.25	6.45	6.60			
Overall Length	D		8.00 BSC				
Exposed Pad Length	D2	6.25	6.45	6.60			
Terminal Width	b	0.20	0.30	0.35			
Terminal Length	L	0.30	0.40	0.50			
Terminal-to-Exposed-Pad	K	0.20	-	-			

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension. usually without tolerance. for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2

48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			S	
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	N	48			
Pitch	е		0.40 BSC		
Overall Height	Α	0.45	0.50	0.55	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3		0.127 REF		
Overall Width	E	6.00 BSC			
Exposed Pad Width	E2	4.45	4.60	4.75	
Overall Length	D		6.00 BSC		
Exposed Pad Length	D2	4.45	4.60	4.75	
Contact Width	b	0.15	0.20	0.25	
Contact Length	L	0.30	0.40	0.50	
Contact-to-Exposed Pad	K	0.20	-	_	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-153A Sheet 2 of 2

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Microchip Tradema Architecture — Flash Memory Fam Program Memory S Product Group — Pin Count — Tape and Reel Flag Temperature Range Package Pattern	rk ily ize (Kb (if app	dsPI	C 33 EP 64 MC5 04 T 1/PT - XXX	Examples: dsPIC33EP64MC504-I/PT: dsPIC33, Enhanced Performance, 64-Kbyte Program Memory, Motor Control, 44-Pin, Industrial Temperature, TQFP package.
Architecture:	33 24	= =	16-bit Digital Signal Controller 16-bit Microcontroller	
Flash Memory Family:	EP	=	Enhanced Performance	
Product Group:	GP MC	= =	General Purpose family Motor Control family	
Pin Count:	02 03 04 06	= = =	28-pin 36-pin 44-pin 64-pin	
Temperature Range:	l E	= =	-40°C to+85°C (Industrial) -40°C to+125°C (Extended)	
Package:	ML MR MV PT SO SP SS TL TL		Plastic Quad, No Lead Package - (44-pin) 8x8 mm body (QFN) Plastic Quad, No Lead Package - (28-pin) 6x6 mm body (QFN-S) Plastic Quad, No Lead Package - (64-pin) 9x9 mm body (QFN) Thin Quad, No Lead Package - (64-pin) 9x9 mm body (UQFN) Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) Plastic Small Outline, Wide - (28-pin) 7.50 mm body (SOIC) Skinny Plastic Dual In-Line - (28-pin) 300 mil body (SPDIP) Plastic Smink Small Outline - (28-pin) 5.30 mm body (SOP) Very Thin Leadless Array - (36-pin) 5x5 mm body (VTLA) Very Thin Leadless Array - (44-pin) 6x6 mm body (VTLA)	