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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gp504t-i-mv

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Pin Diagrams (Continued)



Pin Diagrams (Continued)



1.0 DEVICE OVERVIEW

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com)
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM



3.7 CPU Control Registers

R/W-0) R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
0A ⁽¹⁾	OB ⁽¹⁾	SA ^(1,4)	SB ^(1,4)	OAB ⁽¹⁾	SAB ⁽¹⁾	DA ⁽¹⁾	DC
bit 15							bit 8
R/W-0 ⁽²	R/W-0 ^(2,3)	R/W-0 ^(2,3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2	IPL1	IPL0	RA	N	OV	Z	С
bit 7							bit 0
Legend:		C = Clearable	bit				
R = Reada	able bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value	e at POR	'1'= Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	OA: Accumu	lator A Overflow	v Status bit ⁽¹⁾				
	1 = Accumula	ator A has over	flowed				
	0 = Accumula	ator A has not c	verflowed				
bit 14	OB: Accumu	lator B Overflov	v Status bit ⁽¹⁾				
	1 = Accumula	ator B has over	flowed				
hit 13		lator A Saturatio	n 'Sticky' Sta	tue hit(1,4)			
DIL 15	$1 = \Delta c cumula$	ator A is saturat	ed or has her	n saturated at	some time		
	0 = Accumula	ator A is not sat	urated		Some time		
bit 12	SB: Accumu	lator B Saturatio	on 'Sticky' Sta	tus bit ^(1,4)			
	1 = Accumula	ator B is satura	ed or has bee	en saturated at	some time		
	0 = Accumula	ator B is not sat	urated				
bit 11	OAB: OA (OB Combined A	ccumulator O	verflow Status	bit ⁽¹⁾		
	1 = Accumula	ators A or B have	ve overflowed				
	0 = Neither A	Accumulators A	or B have ove	erflowed	(1)		
bit 10	SAB: SA S	B Combined A	cumulator 'Si	icky Status bit		1	
	1 = Accumula 0 = Neither A	ators A or B are	or B are satur	nave been sat	urated at some	time	
hit 9		Active hit(1)		alou			
bit 0	1 = DO loop is	s in progress					
	0 = DO loop is	s not in progres	S				
bit 8	DC: MCU AL	U Half Carry/Bo	orrow bit				
	1 = A carry-o	out from the 4th	low-order bit (for byte-sized o	data) or 8th low-	order bit (for wo	ord-sized data)
	of the re	sult occurred					
	0 = No carry	-out from the 4	th low-order t	bit (for byte-siz	ed data) or 8th	low-order bit (1	for word-sized
	uala) U						
Note 1:	This bit is availabl	e on dsPIC33E	PXXXMC20X	/50X and dsPl	C33EPXXXGP	50X devices on	ly.
2:	The IPL<2:0> bits	are concatenat	ed with the IF	PL<3> bit (COR	RCON<3>) to fo	rm the CPU Inte	errupt Priority
	Level. The value I IPL< $3 > = 1$.	n parentheses i	naicates the I	PL, IT IPL<3> =	= ⊥. User interru	ipts are disable	a wnen

REGISTER 3-1: SR: CPU STATUS REGISTER

- 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- **4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

TABLE 4-39: PMD REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD	AD1MD	0000
PMD2	0762	_	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	_	_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	CRCMD	_	_	_	_	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	_	_	_	_	_	_	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
PMD7	076C		_			_		_		_	_		DMA0MD DMA1MD DMA2MD DMA3MD	PTGMD	_	_	_	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-40: PMD REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD	AD1MD	0000
PMD2	0762	_	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	—	_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	CRCMD	_	—	_	—	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	_	_	—	_	_	—	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	_	_	PWM3MD	PWM2MD	PWM1MD	_	_	—	_	—	_	_	_	0000
													DMA0MD					
	0760												DMA1MD	DTOMD				
PIVID7	0760	_	_	_	_	_	_	_	_	_	_	_	DMA2MD	PIGMD	_	_	_	0000
													DMA3MD]				

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

		11.0	11.0		11.0		
		0-0	0-0	VREGSE	0-0		VREGS
hit 15		—		VNEGSF	—	Civi	bit 8
bit 10							Dit 0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
bit 7						.1	bit 0
Legend:							
R = Reada	able bit	W = Writable I	oit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	TRAPR: Trap	Reset Flag bit					
	$1 = A \operatorname{Trap} Co$	onflict Reset ha	s occurred	d			
hit 11			s not occurre		ot Elog bit		
DIL 14	1 = An illega	l oncode deter	viinniiaiizeu	v Access Res	et Flay Dit ode or Uninitial	lized W registe	er used as an
	Address	Pointer caused	a Reset			ized w regiote	
	0 = An illegal	l opcode or Uni	nitialized W r	egister Reset h	as not occurred	t	
bit 13-12	Unimplemen	ted: Read as 'o)'				
bit 11	VREGSF: Fla	ish Voltage Reg	ulator Stand	by During Slee	p bit		
	1 = Flash vol	tage regulator i	s active durin	ng Sleep			
bit 10		tage regulator (naby mode dui	ing Sleep		
bit Q	CM: Configur	ation Mismatch	, Elac bit				
bit 5	1 = A Configur	ration Mismatch	h Reset has	occurred			
	0 = A Configu	ration Mismatc	h Reset has	not occurred			
bit 8	VREGS: Volta	age Regulator S	Standby Durii	ng Sleep bit			
	1 = Voltage r	egulator is activ	e during Sle	ер			
	0 = Voltage r	egulator goes in	nto Standby i	mode during SI	еер		
bit 7	EXTR: Extern	nal Reset (MCL	R) Pin bit				
	\perp = A Master 0 = A Master	Clear (pin) Res Clear (pin) Res	et has occur et has not or	rea ccurred			
bit 6	SWR: Softwa	re RESET (Instr	uction) Flag	bit			
	1 = A reset	instruction has	been execut	ed			
	0 = A RESET	instruction has	not been exe	ecuted			
bit 5	SWDTEN: So	oftware Enable/	Disable of W	DT bit ⁽²⁾			
	1 = WDT is er	nabled					
bit 4		ISADIEU hdog Timor Tim	o out Elog b	:+			
DIL 4	1 = WDT time		e-oul Flay D	IL			
	0 = WDT time	e-out has not oc	curred				
Note 1.	All of the Peset sta	itus hits can bo	set or cleare	d in software S	Setting one of th	ese hits in soft	vara does not
	cause a device Re	set.					
2:	If the FWDTEN Co SWDTEN bit settin	onfiguration bit i	s '1' (unprog	rammed), the V	VDT is always e	enabled, regard	less of the

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	_	—	—	PWCOL3	PWCOL2	PWCOL1	PWCOL0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	างพท
bit 15-4	Unimplemen	ted: Read as '	0'				
bit 3	PWCOL3: DN	VA Channel 3 F	Peripheral Wri	te Collision Fla	ag bit		
	1 = Write col	lision is detecte	ed				
	0 = No write	collision is dete	ected				
bit 2	PWCOL2: DN	MA Channel 2 I	Peripheral Wri	te Collision Fla	ag bit		
	1 = Write col	lision is detecte	ed				
	0 = No write	collision is dete	ected				
bit 1	PWCOL1: DN	MA Channel 1 F	Peripheral Wri	te Collision Fla	ag bit		
	1 = Write col	lision is detecte	ed				
h:+ 0					h-14		
DIT U			Peripheral vvri	te Collision Fla	ag dit		
	$\perp = \text{VVrite COI}$	collision is detected	eted				

REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER

10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the powersaving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN[™] module has been configured for 500 kbps, based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC[®] DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding
	module is disabled after a delay of one
	instruction cycle. Similarly, if a PMD bit is
	cleared, the corresponding module is
	enabled after a delay of one instruction
	cycle (assuming the module control regis-
	ters are already configured to enable
	module operation).

10.5 Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.



10.5.1 KEY RESOURCES

- "Watchdog Timer and Power-Saving Modes" (DS70615) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 11-26: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP118	8R<5:0>		
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—		_	_	_	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	RP118R<5:0>: Peripheral Output Function is Assigned to RP118 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-0 Unimplemented: Read as '0'

REGISTER 11-27: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP120)R<5:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 Unimplemented: Read as '0'

bit 5-0 **RP120R<5:0>:** Peripheral Output Function is Assigned to RP120 Output Pin bits (see Table 11-3 for peripheral function numbers)

13.0 TIMER2/3 AND TIMER4/5

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter
- They also support these features:
- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (32-bit timer pairs, and Timer3 and Timer5 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw); Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

Note: For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note: Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture Stop in Idle Control bit
	1 = Input capture will Halt in CPU Idle mode
	0 = Input capture will continue to operate in CPU Idle mode
bit 12-10	ICTSEL<2:0>: Input Capture Timer Select bits
	111 = Peripheral clock (FP) is the clock source of the ICx
	110 = Reserved
	101 = Reserved
	100 - 11 CLR is the clock source of the ICx (only the synchronous clock is supported) 011 = T5CLK is the clock source of the ICx
	010 = T4CLK is the clock source of the ICx
	001 = T2CLK is the clock source of the ICx
	000 = T3CLK is the clock source of the ICx
bit 9-7	Unimplemented: Read as '0'
bit 6-5	ICI<1:0>: Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	01 = Interrupt on every second capture event
hit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
bit 4	1 = Input capture buffer overflow occurred
	0 = No input capture buffer overflow occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	1 = Input capture buffer is not empty, at least one more capture value can be read
	0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture Mode Select bits
	111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
	110 = Unused (module is disabled)
	101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
	100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
	011 = Capture mode, every falling edge (Simple Capture mode)
	001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
	000 = Input capture module is turned off

REGISTER 17-1: QEI1CON: QEI1 CONTROL REGISTER (CONTINUED)

bit 6-4	INTDIV<2:0>: Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select) ⁽³⁾
	<pre>111 = 1:128 prescale value 110 = 1:64 prescale value 101 = 1:32 prescale value 100 = 1:16 prescale value 011 = 1:8 prescale value 010 = 1:4 prescale value 001 = 1:2 prescale value 000 = 1:1 prescale value</pre>
bit 3	CNTPOL: Position and Index Counter/Timer Direction Select bit
	 0 = Counter direction is positive unless modified by external up/down signal
bit 2	GATEN: External Count Gate Enable bit
	 1 = External gate signal controls position counter operation 0 = External gate signal does not affect position counter/timer operation
bit 1-0	CCM<1:0>: Counter Control Mode Selection bits
	 11 = Internal Timer mode with optional external count is selected 10 = External clock count with optional external count is selected 01 = External clock count with external up/down direction is selected 00 = Quadrature Encoder Interface (x4 mode) Count mode is selected
Note 1:	When CCM<1:0> = 10 or 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

- 2: When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.
- 3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
QCAPEN	FLTREN	QFDIV2	QFDIV1	QFDIV0	OUTFNC1	OUTFNC0	SWPAB					
bit 15					• •		bit 8					
R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x					
HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA					
bit 7	bit 7 bi											
Legend:	a hit	\// - \//ritabla	h it	II – Unimploy	monted bit read	4 a.a. (0)						
n - Value at		vv = vvii(able	DIL	$0^{\circ} = 0$	nented bit, read	v – Ritic unkn						
		1 - Dit 13 36t			areu							
bit 15	OCAPEN: OF	-I Position Cou	nter Input Cap	ture Enable bit								
	1 = Index ma	tch event trigge	ers a position c	apture event								
	0 = Index ma	tch event does	not trigger a p	osition capture	event							
bit 14	FLTREN: QE	Ax/QEBx/INDX	x/HOMEx Digi	ital Filter Enabl	e bit							
	1 = Input pin	digital filter is e digital filter is d	nabled isabled (bypas	eed)								
hit 13_11			NDXv/HOMEv	Digital Input Fi	ilter Clock Divid	a Salact hits						
511 15-11	111 = 1:128 (clock divide		Digital Input I								
	110 = 1:64 cl	ock divide										
	101 = 1:32 cl	ock divide										
	100 = 1.16 cm 011 = 1:8 clo	ck divide										
	010 = 1:4 clo	ck divide										
	001 = 1:2 clo	ck divide ck divide										
hit 10₋9			Output Functi	ion Mode Sele	rt hits							
bit 10 5	11 = The CTN	VCMPx pin ace	s high when C	$EI1LEC \ge POS$	$S1CNT \ge QEI10$	GEC						
	10 = The CTM	NCMPx pin goe	s high when P	$OS1CNT \leq QE$	EIILEC							
	01 = The CT	NCMPx pin goe	s high when P	$OS1CNT \ge QE$	EI1GEC							
hit 8	SWPAB: Swa	OFA and OFA	B Innuts hit									
bit 0	1 = QEAx and	d QEBx are swa	apped prior to	quadrature de	coder logic							
	0 = QEAx and	d QEBx are not	swapped	1								
bit 7	HOMPOL: HO	OMEx Input Po	larity Select bit	t								
	1 = Input is in	iverted										
hit 6		ot inverted Vy Input Dolori	ty Soloot bit									
DILO	1 = Input is in	verted	ly Select bit									
	0 = Input is no	ot inverted										
bit 5	QEBPOL: QE	EBx Input Polar	ity Select bit									
	1 = Input is ir	nverted										
L:1 4		ot inverted	:									
DIT 4		EAX Input Polar	ity Select bit									
	1 = 10000000000000000000000000000000000	not inverted										
bit 3	HOME: Statu	s of HOMEx In	out Pin After P	olarity Control								
	1 = Pin is at I	logic '1'		-								
	0 = Pin is at	logic '0'										

REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER



FIGURE 19-1: I2Cx BLOCK DIAGRAM (X = 1 OR 2)

26.3 Programmable CRC Registers

REGISTER 26-1: CRCCON1: CRC CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0				
CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0				
bit 15							bit 8				
R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0				
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	_	—				
bit 7 bit											
Legend:											
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'					
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown				
bit 15	CRCEN: CRC 1 = CRC mod 0 = CRC mod SFRs are	C Enable bit dule is enablec dule is disable not reset	l d; all state ma	ichines, pointe	rs and CRCWD	AT/CRCDAT a	re reset, other				
bit 14	Unimplemen	ted: Read as '	0'								
bit 13	CSIDL: CRC	Stop in Idle Mo	ode bit								
	1 = Discontin 0 = Continue	ues module op s module oper	peration when ation in Idle m	device enters lode	Idle mode						
bit 12-8	VWORD<4:0	>: Pointer Valu	e bits								
	Indicates the or 16 when Pl	number of value $LEN<4:0> \le 7.$	d words in the	FIFO. Has a n	naximum value	of 8 when PLE	N<4:0> > 7				
bit 7	CRCFUL: CR	C FIFO Full bi	t								
	1 = FIFO is fu	ull .									
		ot full									
DIT 6	1 = FIFO is e	C FIFO Empty	/ Bit								
	0 = FIFO is n	ot empty									
bit 5	CRCISEL: CF	RC Interrupt Se	election bit								
	1 = Interrupt 0 = Interrupt	on FIFO is em on shift is com	pty; final word plete and CR(of data is still CWDAT results	shifting through are ready	CRC					
bit 4	CRCGO: Start CRC bit										
	 1 = Starts CRC serial shifter 0 = CRC serial shifter is turned off 										
bit 3	LENDIAN: Da	ata Word Little-	Endian Config	guration bit							
	1 = Data wor 0 = Data wor	d is shifted into d is shifted into	o the CRC star o the CRC star	rting with the L rting with the M	Sb (little endiar ISb (big endian	1))					
bit 2-0	Unimplemented: Read as '0'										



AC CHARACTERISTICS			Standard Ope (unless other) Operating tem	rating Co wise state perature	prditions: 3.0V to 3.6V ed) $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended		
Param No.	Symb	Characteristic	Min.	Тур. ⁽¹⁾	Max.	Units	Conditions
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	_	60	MHz	EC
		Oscillator Crystal Frequency	3.5 10	—	10 25	MHz MHz	XT HS
OS20	Tosc	Tosc = 1/Fosc	8.33	—	DC	ns	+125°C
		Tosc = 1/Fosc	7.14	—	DC	ns	+85°C
OS25	TCY	Instruction Cycle Time ⁽²⁾	16.67	—	DC	ns	+125°C
		Instruction Cycle Time ⁽²⁾	14.28	—	DC	ns	+85°C
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x Tosc	—	0.55 x Tosc	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time ^(3,4)	—	5.2	—	ns	
OS41	TckF	CLKO Fall Time ^(3,4)	—	5.2	—	ns	
OS42	Gм	External Oscillator Transconductance ⁽⁴⁾	—	12	—	mA/V	HS, VDD = 3.3V, TA = +25°C
			—	6	—	mA/V	XT, VDD = 3.3V, TA = +25°C

TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- 2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.
- 3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
- 4: This parameter is characterized, but not tested in manufacturing.

FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



TABLE 30-36:SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard (unless of Operating	Operatin otherwise temperat	g Conditie stated) ture -40°	ons: 3.0V $^{\circ}C \leq TA \leq$	/ to 3.6V +85°C for Industrial
	i	<i>"</i>		(0)	-40°	$^{\circ}C \leq TA \leq$	+125°C for Extended
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	-40°C to +125°C (Note 3)
SP20	TscF	SCK2 Output Fall Time	_	_		ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK2 Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30			ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30			ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPI2 pins.



FIGURE 30-28: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

DC CHARACT	Standard C (unless off Operating t	Operating Co nerwise state emperature	onditions: 3 ed) -40°C ≤ TA	0V to 3.6V ≤ +150°C			
Parameter No.	Typical	Max	Units	Conditions			
Power-Down	Current (IPD)						
HDC60e	1400	2500	μA	+150°C	3.3V	Base Power-Down Current (Notes 1, 3)	
HDC61c	15	—	μA	+150°C	3.3V	Watchdog Timer Current: ∆IWDT (Notes 2, 4)	

TABLE 31-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

Note 1: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to Vss. WDT, etc., are all switched off and VREGS (RCON<8>) = 1.

2: The ∆ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

3: These currents are measured on the device containing the most memory in this family.

4: These parameters are characterized, but are not tested in manufacturing.

TABLE 31-5: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Parameter No.	Typical	Max	Units	Conditions			
HDC44e	12	30	mA	+150°C 3.3V 40 MIPS			

TABLE 31-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Parameter No.	Typical	Мах	Units	Conditions			
HDC20	9	15	mA	+150°C	3.3V	10 MIPS	
HDC22	16	25	mA	+150°C	3.3V	20 MIPS	
HDC23	30	50	mA	+150°C	3.3V	40 MIPS	

TABLE 31-7: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$					
Parameter No.	Typical	Мах	Doze Ratio	Units	Conditions			
HDC72a	24	35	1:2	mA				
HDC72f ⁽¹⁾	14	—	1:64	mA	+150°C	3.3V	40 MIPS	
HDC72g ⁽¹⁾	12	_	1:128	mA				

Note 1: Parameters with Doze ratios of 1:64 and 1:128 are characterized, but are not tested in manufacturing.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS				
Dimension	Dimension Limits		NOM	MAX		
Number of Pins		28				
Pitch	е	0.65 BSC				
Overall Height	Α	-	-	2.00		
Molded Package Thickness	A2	1.65	1.75	1.85		
Standoff	A1	0.05	-	-		
Overall Width	E	7.40	7.80	8.20		
Molded Package Width	E1	5.00	5.30	5.60		
Overall Length	D	9.90	10.20	10.50		
Foot Length	L	0.55	0.75	0.95		
Footprint	L1	1.25 REF				
Lead Thickness	с	0.09	-	0.25		
Foot Angle	¢	0°	4°	8°		
Lead Width	b	0.22	_	0.38		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.

- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B