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Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc202-i-mm

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FIGURE 2-5: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER









FIGURE 4-9: DATA MEMORY MAP FOR dsPIC33EP128MC20X/50X AND dsPIC33EP128GP50X DEVICES





TADLL 4-2																		
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	_	—	CSIDL	ABAT	CANCKS	R	EQOP<2:0)>	OPN	NODE<2:0	>	_	CANCAP	_	_	WIN	0480
C1CTRL2	0402	_	—	_	—	—	—	_	_	_	—	_		D	NCNT<4:0	>		0000
C1VEC	0404	_	_	_		F	ILHIT<4:0>			_				ICODE<6:0	>			0040
C1FCTRL	0406	[DMABS<2:0	>	—	—		—	_	_	—	—			FSA<4:0>			0000
C1FIFO	0408	_	_			FBP<	5:0>			_	_			FNRB	<5:0>			0000
C1INTF	040A	_	_	ТХВО	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	_	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	_	_	_	—	—	_	_	_	IVRIE	WAKIE	ERRIE	_	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E				TERRCN	T<7:0>							RERRCM	NT<7:0>				0000
C1CFG1	0410	_	_	_	—	—	_	_	_	SJW<	1:0>			BRP	<5:0>			0000
C1CFG2	0412	_	WAKFIL	_	SEG2PH<2:0> SEG2PHTS SAM SEG1PH<2:0> PRSEG				RSEG<2:0	>	0000							
C1FEN1	0414	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C1FMSKSEL1	0418	F7MS	K<1:0>	F6MS	K<1:0>	<1:0> F5MSK<1:0> F4MSK<1:0>			F3MSK<1:0> F2MSK<1:0>			K<1:0>	:0> F1MSK<1:0> F0MSK<1:0>		0000			
C1FMSKSEL2	041A	F15MS	SK<1:0>	F14MS	K<1:0>	<pre><<1:0> F13MSK<1:0> F12MSK<1:0></pre>			F11MSK<1:0> F10MSK<1:0> F9MSK<1:0>			<<1:0>	F8MSK<1:0> 00		0000			

TABLE 4-21: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 0 OR 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 0 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400- 041E							S	ee definition	when WIN	= x							
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	11 RXOVF10 RXOVF9 RXOVF8 RXOVF7 RXOVF6 RXOVF5 RXOVF4 RXOVF3 RXOVF2 RXOVF1 RXOVF0								0000			
C1RXOVF2	042A	RXOVF31	RXOVF30	0 RXOVF29 RXOVF28 RXOVF27 RXOVF26 RXOVF25 RXOVF24 RXOVF23 RXOVF22 RXOVF22 RXOVF21 RXOVF20 RXOVF19 RXOVF18 RXOVF18 RXOVF17 RXOVF16 000												0000		
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PF	RI<1:0>	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PF	RI<1:0>	0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PF	RI<1:0>	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PF	RI<1:0>	0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PF	RI<1:0>	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PF	RI<1:0>	0000
C1TR67CON	0436	TXEN7 TXABT7 TXLARB7 TXERR7 TXREQ7 RTREN7 TX7PRI<1:0> TXEN6 TXABAT6 TXLARB6 TXER6 TXREQ6 RTREN6 TX6PRI<1:0> xx											xxxx					
C1RXD	0440	ECAN1 Receive Data Word xxx												xxxx				
C1TXD	0442							E	CAN1 Trans	smit Data W	ord							xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: CRC REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON1	0640	CRCEN	—	CSIDL		V	WORD<4:()>		CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	-	—	0000
CRCCON2	0642	_	_	_		D	WIDTH<4:0)>		_	_	_		F	PLEN<4:0>			0000
CRCXORL	0644		X<15:1> 000													0000		
CRCXORH	0646		X<31:16> 000												0000			
CRCDATL	0648								CRC Data	Input Low V	Vord							0000
CRCDATH	064A								CRC Data	Input High \	Nord							0000
CRCWDATL	064C		CRC Result Low Word 0000											0000				
CRCWDATH	064E		CRC Result High Word 0000															

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

TABLE 4-25: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC202/502 AND PIC24EPXXXGP/MC202 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
RPOR0	0680	_	—		RP35R<5:0>						—	RP20R<5:0> 00							
RPOR1	0682	_	_		RP37R<5:0>						_	RP36R<5:0> 01							
RPOR2	0684	_	_			RP39F	२<5:0>			—	_	RP38R<5:0>						0000	
RPOR3	0686	_	_		RP41R<5:0>					—	_	RP40R<5:0> 0					0000		
RPOR4	0688	_	—		RP43R<5:0>						_			RP42F	२<5:0>			0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC203/503 AND PIC24EPXXXGP/MC203 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
RPOR0	0680	—	_		RP35R<5:0>						_			RP20	R<5:0>			0000	
RPOR1	0682	_	_			RP37	२<5:0>			_	_			RP36	२<5:0>			0000	
RPOR2	0684	_	_		RP39R<5:0>						_		RP38R<5:0>						
RPOR3	0686	_	_			RP41	२<5:0>			_	_		RP40R<5:0>						
RPOR4	0688	_	_			RP43	२<5:0>			_	_			RP42	२<5:0>			0000	
RPOR5	068A	_	_	_							_							0000	
RPOR6	068C			-	—	_		—			_			RP56	R<5:0>			0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
GIE	DISI	SWTRAP		_	_	_	—
bit 15				·			bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
		_	_	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0
Legend:	L:1		L:1			(0)	
R = Readable	DIT	vv = vvritable	DIT		mented bit, read	as '0'	
-n = value at I	POR	"1" = Bit is set		$0^{\circ} = Bit is cle$	eared	x = Bit is unkr	nown
hit 15		ntorrunt Enable	, hit				
DIL 15		and associate	d IF hits are e	nahled			
	0 = Interrupts	are disabled,	but traps are s	still enabled			
bit 14	DISI: DISI Ir	nstruction Statu	s bit				
	1 = DISI ins	truction is activ	e				
	0 = DISI ins i	truction is not a	ictive				
bit 13	SWTRAP: So	oftware Trap St	atus bit				
	1 = Software	trap is enabled	4				
hit 12-3		ted. Read as '	 				
bit 2	INT2FP: Exte	ernal Interrupt 2	∘ PEdge Detect	Polarity Selec	et bit		
	1 = Interrupt	on negative ed	ae				
	0 = Interrupt	on positive edg	le				
bit 1	INT1EP: Exte	ernal Interrupt ?	Edge Detect	Polarity Selec	ct bit		
	1 = Interrupt	on negative ed	ge				
	0 = Interrupt	on positive edg	e				
bit 0	INTOEP: Exte	ernal Interrupt () Edge Detect	Polarity Selec	ct bit		
	\perp = interrupt	on negative ed	ye Ie				

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CHEN	SIZE	DIR	HALF	NULLW	_	—	—
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
		AMODE1	AMODE0			MODE1	MODE0
bit 7							bit 0
Legend:			,			(0)	
R = Readable	bit	W = Writable	bit		mented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		0^{\prime} = Bit is cle	eared	x = Bit is unkn	IOWN
bit 15		Channel Enabl	o hit				
bit 15	1 = Channel	is enabled					
	0 = Channel	is disabled					
bit 14	SIZE: DMA D	ata Transfer Si	ze bit				
	1 = Byte						
	0 = Word						
bit 13	DIR: DMA Tra	ansfer Direction) bit (source/d	estination bus	select)		
	1 = Reads from 0 = Reads from 1	om RAM addre	ddress. writes to p	s to RAM addr	ess ess		
bit 12	HALF: DMA	Block Transfer	Interrupt Sele	ct bit			
	1 = Initiates i	nterrupt when I	nalf of the dat	a has been mo	oved		
	0 = Initiates i	nterrupt when a	all of the data	has been mov	ved		
bit 11	NULLW: Null	Data Periphera	al Write Mode	Select bit			
	1 = Null data	write to periph	eral in additio	n to RAM write	e (DIR bit must a	also be clear)	
bit 10-6	Unimplemen	ted: Read as '	ר'				
bit 5-4	AMODE<1:0	: DMA Channe	el Addressina	Mode Select	bits		
	11 = Reserve	ed					
	10 = Peripher	ral Indirect Add	ressing mode				
	01 = Register	Indirect withou	ut Post-Increm	nent mode			
hit 3 2		tod: Pood as '	ost-incremen	tmode			
bit 1_0		DMA Channel	Operating Mc	nda Salact hits			
bit 1-0	11 = One-Sh	ot. Pina-Pona r	nodes are en	abled (one blo	ck transfer from	/to each DMA b	ouffer)
	10 = Continue	ous, Ping-Pong	modes are e	nabled			
	01 = One-Sho	ot, Ping-Pong r	nodes are dis	abled			
		ous, Ping-Pong	modes are d	ISADIEO			

REGISTER 8-1: DMAXCON: DMA CHANNEL X CONTROL REGISTER

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_		—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
			DMA0MD ⁽¹⁾				
_	_	_	DMA1MD ⁽¹⁾	PTGMD	_	_	_
			DMA2MD ⁽¹⁾	1 TOME			
			DMA3MD ⁽¹⁾				
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown
bit 15-5	Unimplement	ted: Read as '	D'				
bit 4	DMA0MD: DN	/A0 Module Di	sable bit ⁽¹⁾				
	1 = DMA0 mo	dule is disable	d				
	0 = DMA0 mo	dule is enable	d 				
	DMA1MD: DN	/A1 Module Di	sable bit(")				
	1 = DMA1 mo 0 = DMA1 mo	dule is disable	d d				
			sable bit(1)				
	1 = DMA2 mo	dule is disable	d				
	0 = DMA2 mo	dule is enable	d				
	DMA3MD: DN	/A3 Module Di	sable bit ⁽¹⁾				
	1 = DMA3 mo	dule is disable	d				
	0 = DMA3 mo	dule is enable	b				
bit 3	PTGMD: PTG	Module Disab	le bit				
	1 = PTG mod	ule is disabled					
	$0 = PIG \mod 1$	uie is enabled	-1				
DIT 2-0	Unimplement	tea: Read as '	J.				
Note 1: Th	nis single bit ena	ables and disat	oles all four DM	A channels.			

REGISTER 10-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

15.2 Output Compare Control Registers

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
		OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	_	ENFLTB
bit 15							bit 8
R/W-0	U-0	R/W-0, HSC	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0
ENFLTA		OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0
bit 7							bit 0
Legend:		HSC = Hardw	are Settable/Cl	earable bit			
R = Reada	ible bit	W = Writable I	bit	U = Unimplem	nented bit, read	as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-14	Unimplemen	ted: Read as '0)'				
bit 13	OCSIDL: Out	tput Compare x	Stop in Idle Mo	de Control bit			
	1 = Output C	compare x Halts	in CPU Idle me	ode via CDU Idia m	odo		
bit 12 10			nues lo operale		oue		
DIL 12-10	111 = Perinh	eral clock (Ep)	pare x Clock S				
	110 = Reserv	/ed					
	101 = PTGO	x clock ⁽²⁾					
	100 = T1CLK	is the clock so	urce of the OC	k (only the sync	hronous clock	is supported)	
	011 = 15CLK	is the clock sou	urce of the OC	х ~			
	001 = T3CLK	is the clock so	urce of the OC	x X			
	000 = T2CLK	is the clock so	urce of the OC	ĸ			
bit 9	Unimplemen	ted: Read as '0)'				
bit 8	ENFLTB: Fau	ult B Input Enab	le bit				
	1 = Output C 0 = Output C	ompare Fault B compare Fault B	input (OCFB) input (OCFB)	is enabled is disabled			
bit 7	ENFLTA: Fau	ult A Input Enabl	le bit				
	1 = Output C	ompare Fault A	input (OCFA)	is enabled			
	0 = Output C	ompare Fault A	input (OCFA)	is disabled			
bit 6	Unimplemen	ted: Read as '0)'				
bit 5	OCFLTB: PW	M Fault B Cond	dition Status bit				
	1 = PWM Fa 0 = No PWM	ult B condition of Fault B condition	on OCFB pin ha on on OCFB pi	as occurred n has occurred			
bit 4	OCFLTA: PW	/M Fault A Cond	dition Status bit				
	1 = PWM Fa	ult A condition of	on OCFA pin ha	as occurred			
	0 = No PWM	I Fault A condition	on on OCFA pi	n has occurred			
Note 1:	OCxR and OCxF	RS are double-b	ouffered in PWN	A mode only.			
2:	Each Output Cor	mpare x module	(OCx) has one	PTG clock sou	urce. See Secti	on 24.0 "Perip	oheral Trigger
	Generator (PTG PTGO4 = OC1) wodule" for r	nore informatio	n.			
	PTGO5 = OC2						
	PTGO6 = OC3						
	PTGO7 = OC4						

16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support a dedicated Pulse-Width Modulation (PWM) module with up to 6 outputs.

The high-speed PWMx module consists of the following major features:

- Three PWM generators
- Two PWM outputs per PWM generator
- Individual period and duty cycle for each PWM pair
- Duty cycle, dead time, phase shift and frequency resolution of Tcy/2 (7.14 ns at Fcy = 70MHz)
- Independent Fault and current-limit inputs for six PWM outputs
- · Redundant output
- Center-Aligned PWM mode
- Output override control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Prescaler for input clock
- PWMxL and PWMxH output pin swapping
- Independent PWM frequency, duty cycle and phase-shift changes for each PWM generator
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB) functionality
- Frequency resolution enhancement
- PWM capture functionality

Note: In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 8.32 ns.

The high-speed PWMx module contains up to three PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWMx can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADC module based on either of the two master time bases.

The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 input pin that utilizes PPS, can synchronize the high-speed PWMx module with an external signal. The SYNCO1 pin is an output pin that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

16.1 PWM Faults

The PWMx module incorporates multiple external Fault inputs to include FLT1 and FLT2 which are remappable using the PPS feature, FLT3 and FLT4 which are available only on the larger 44-pin and 64-pin packages, and FLT32 which has been implemented with Class B safety features, and is available on a fixed pin on all dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

16.1.1 PWM FAULTS AT RESET

During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the highspeed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled low externally or the internal pull-down resistor in the CNPDx register can be enabled.

Note: The Fault mode may be changed using the FLTMOD<1:0> bits (FCLCON<1:0>), regardless of the state of FLT32.

16.2 PWM Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

16.2.1 KEY RESOURCES

- "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | | | | bit 0 |

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-0 EID<15:0>: Extended Identifier bits

1 = Message address bit, EIDx, must be '1' to match filter

0 = Message address bit, EIDx, must be '0' to match filter

REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F7M	SK<1:0>	F6MSI	K<1:0>	F5MS	K<1:0>	F4MSK<1:0>		
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F3M	SK<1:0>	F2MSI	K<1:0>	F1MS	K<1:0>	F0MS	K<1:0>	
bit 7							bit 0	
Legend:								
R = Readabl	le bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'		
-n = Value at	t POR	'1' = Bit is set	:	'0' = Bit is clea	ared	x = Bit is unkr	nown	
bit 15-14	F7MSK<1:0: 11 = Reserve 10 = Accepta 01 = Accepta 00 = Accepta	>: Mask Source ed ance Mask 2 re ance Mask 1 re ance Mask 0 re	for Filter 7 bi gisters contair gisters contair gisters contair	ts n mask n mask n mask				
bit 13-12	F6MSK<1:0	>: Mask Source	for Filter 6 bi	ts (same values	as bits<15:14	! >)		
bit 11-10	F5MSK<1:0	>: Mask Source	for Filter 5 bi	ts (same values	as bits<15:14	! >)		
bit 9-8	F4MSK<1:0	>: Mask Source	for Filter 4 bi	ts (same values	as bits<15:14	! >)		
bit 7-6	F3MSK<1:0:	>: Mask Source	for Filter 3 bi	ts (same values	s as bits<15:14	l>)		
bit 5-4	F2MSK<1:0	>: Mask Source	for Filter 2 bi	ts (same values	s as bits<15:14	! >)		
bit 3-2	F1MSK<1:0	>: Mask Source	for Filter 1 bi	ts (same values	s as bits<15:14	ł>)		
bit 1-0	F0MSK<1:0	Hask Source	for Filter 0 bi	ts (same values	s as bits<15:14	! >)		

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

RXOVF4

bit 7			bit 0
Legend:	C = Writable bit, but or	nly '0' can be written to clear the bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	

RXOVF3

RXOVF2

R = Readable bit	vv = vvritable bit	U = Unimplemented bit, read	as 0
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 RXOVF<15:0>: Receive Buffer n Overflow bits

RXOVF6

RXOVF7

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

RXOVF5

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0	' can be written to clear the bi	t
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 RXOVF<31:16>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

RXOVF0

RXOVF1

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0
bit 15							bit 8

| R/W-0 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 Unimplemented: Read as '0'

bit 11-8	SELSRCC<3:0>: Mask C Input Select bits
	1111 = FLT4
	1110 = FLT2
	1101 = PTGO19
	1100 = PTGO18
	1011 = Reserved
	1010 = Reserved
	1001 = Reserved
	1000 = Reserved
	0111 = Reserved
	0110 = Reserved
	0101 = PWM3H
	0100 = PWM3L
	0011 = PWM2H
	0010 = PWM2L
	0001 = PWM1H
	0000 = PWM1L
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1001 = Reserved 1000 = Reserved 0011 = Reserved 0111 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved 0110 = Reserved 0110 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3I
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2I
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H 0000 = PWM1I



FIGURE 30-3: I/O TIMING CHARACTERISTICS

TABLE 30-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature } -40^\circ C \leq T_A \leq +85^\circ C \mbox{ for Industrial} \\ -40^\circ C \leq T_A \leq +125^\circ C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic	Min.	Тур. ⁽¹⁾	Max.	Units	Conditions
DO31	TIOR	Port Output Rise Time	_	5	10	ns	
DO32	TIOF	Port Output Fall Time	—	5	10	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	_		ns	
DI40	TRBP	CNx High or Low Time (input)	2		_	TCY	

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

FIGURE 30-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS









AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)(1)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
ADC Accuracy (10-Bit Mode)							
AD20b	Nr	Resolution	10 Data Bits		bits		
AD21b	INL	Integral Nonlinearity	-0.625		0.625	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-1.5	_	1.5	LSb	+85°C < TA ≤ +125°C (Note 2)
AD22b	DNL	Differential Nonlinearity	-0.25	_	0.25	LSb	-40°C \leq TA \leq +85°C (Note 2)
			-0.25		0.25	LSb	+85°C < TA \leq +125°C (Note 2)
AD23b	Gerr	Gain Error	-2.5		2.5	LSb	-40°C \leq TA \leq +85°C (Note 2)
			-2.5	_	2.5	LSb	+85°C < TA \leq +125°C (Note 2)
AD24b	EOFF	Offset Error	-1.25		1.25	LSb	$-40^{\circ}C \le TA \le +85^{\circ}C \text{ (Note 2)}$
			-1.25	_	1.25	LSb	+85°C < TA \leq +125°C (Note 2)
AD25b	—	Monotonicity	_	_	_		Guaranteed
Dynamic Performance (10-Bit Mode)							
AD30b	THD	Total Harmonic Distortion ⁽³⁾		64	—	dB	
AD31b	SINAD	Signal to Noise and Distortion ⁽³⁾	-	57	_	dB	
AD32b	SFDR	Spurious Free Dynamic Range ⁽³⁾	—	72	—	dB	
AD33b	Fnyq	Input Signal Bandwidth ⁽³⁾	_	550		kHz	
AD34b	ENOB	Effective Number of Bits ⁽³⁾	—	9.4	—	bits	

TABLE 30-59: ADC MODULE SPECIFICATIONS (10-BIT MODE)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

Revision C (December 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see Section 20.1 "UART Helpful Tips" and Section 3.6 "CPU Resources". All occurrences of TLA were updated to VTLA throughout the document, with the exception of the pin diagrams (updated diagrams were not available at time of publication).

A new chapter, Section 31.0 "DC and AC Device Characteristics Graphs", was added.

All other major changes are referenced by their respective section in Table A-2.

Section Name	Update Description
"16-bit Microcontrollers and Digital Signal Controllers (up to 256-Kbyte Flash and 32-Kbyte SRAM) with High- Speed PWM, Op amps, and Advanced Analog"	The content on the first page of this section was extensively reworked to provide the reader with the key features and functionality of this device family in an "at-a-glance" format.
Section 1.0 "Device Overview"	Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X Block Diagram (see Figure 1-1), which now contains a CPU block and a reference to the CPU diagram. Updated the description and Note references in the Pinout I/O Descriptions for these pins: C1IN2- C2IN2- C3IN2- OA1OUT OA2OUT and OA3OUT (see Table 1-1)
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"	Updated the Recommended Minimum Connection diagram (see Figure 2-1).
Section 3.0 "CPU"	Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X CPU Block Diagram (see Figure 3-1). Updated the Status register definition in the Programmer's Model (see Figure 3-2).
Section 4.0 "Memory Organization"	Updated the Data Memory Maps (see Figure 4-6 and Figure 4-11). Removed the DCB<1:0> bits from the OC1CON2, OC2CON2, OC3CON2, and OC4CON2 registers in the Output Compare 1 Through Output Compare 4 Register Map (see Table 4-10). Added the TRIG1 and TRGCON1 registers to the PWM Generator 1 Register Map (see Table 4-13). Added the TRIG2 and TRGCON2 registers to the PWM Generator 2 Register Map (see Table 4-14). Added the TRIG3 and TRGCON3 registers to the PWM Generator 3 Register Map (see Table 4-15). Updated the second note in Section 4.7.1 "Bit-Reversed Addressing Implementation".
Section 8.0 "Direct Memory Access (DMA)"	Updated the DMA Controller diagram (see Figure 8-1).
Section 14.0 "Input Capture"	Updated the bit values for the ICx clock source of the ICTSEL<12:10> bits in the ICxCON1 register (see Register 14-1).
Section 15.0 "Output Compare"	Updated the bit values for the OCx clock source of the OCTSEL<2:0> bits in the OCxCON1 register (see Register 15-1). Removed the DCB<1:0> bits from the Output Compare x Control Register 2 (see Register 15-2).

TABLE A-2: MAJOR SECTION UPDATES