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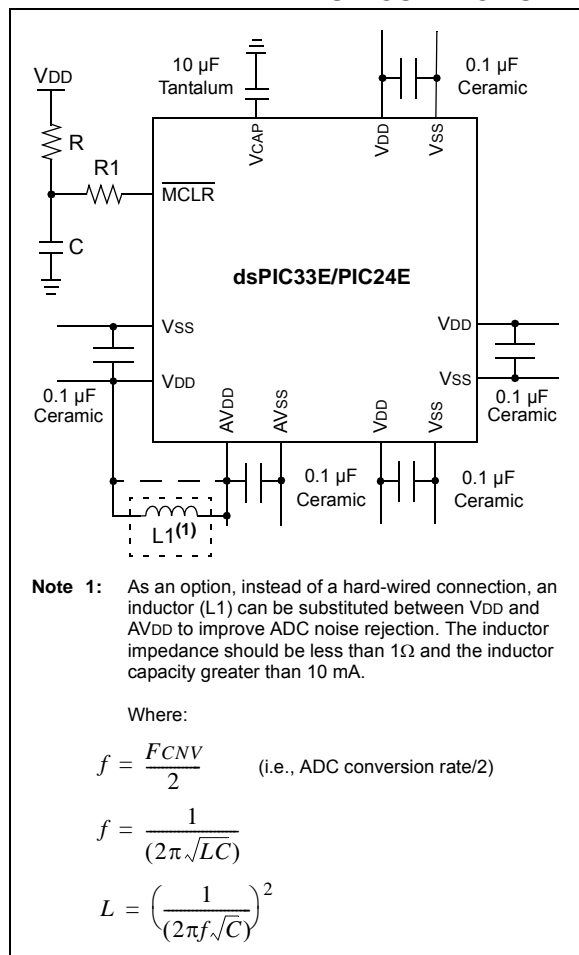
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc202-i-so

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohm) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor greater than 4.7 µF (10 µF is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 30.0 “Electrical Characteristics”** for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 27.3 “On-Chip Voltage Regulator”** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

- Device Reset
- Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS

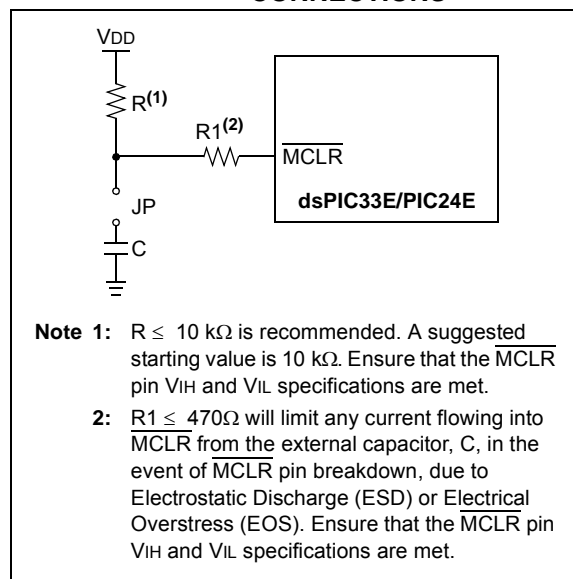


FIGURE 2-7: INTERLEAVED PFC

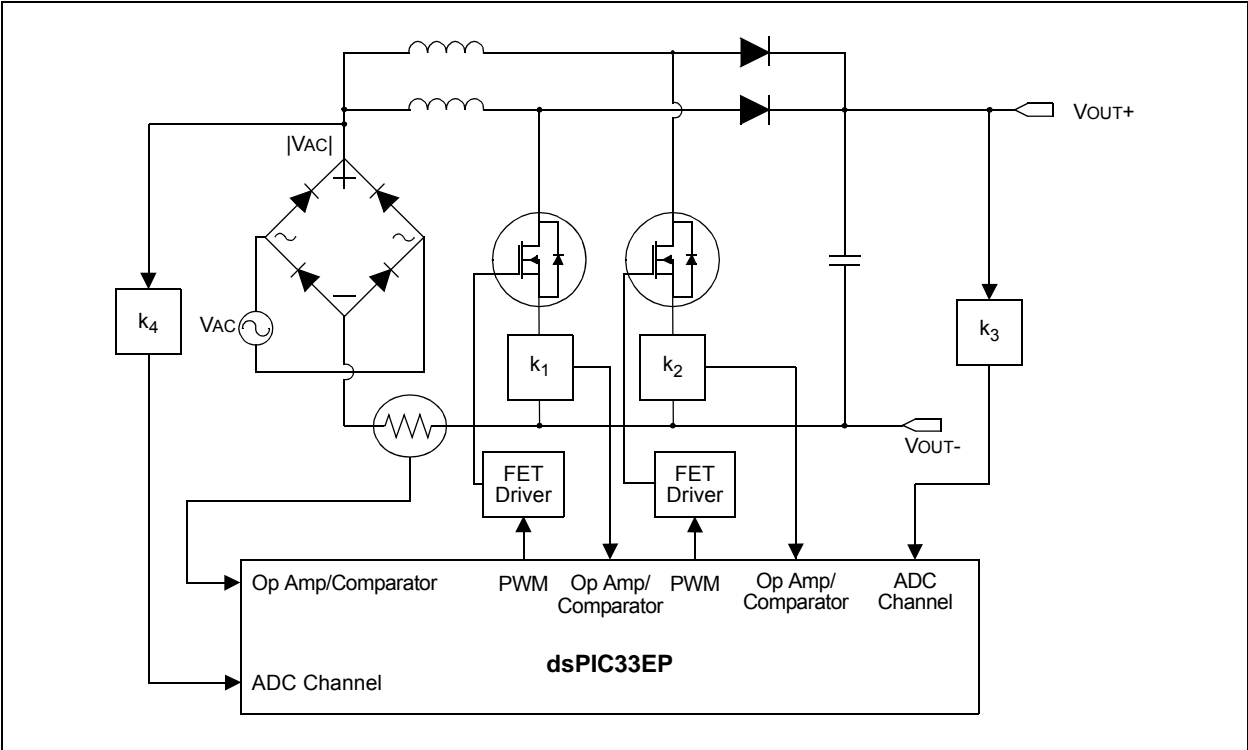
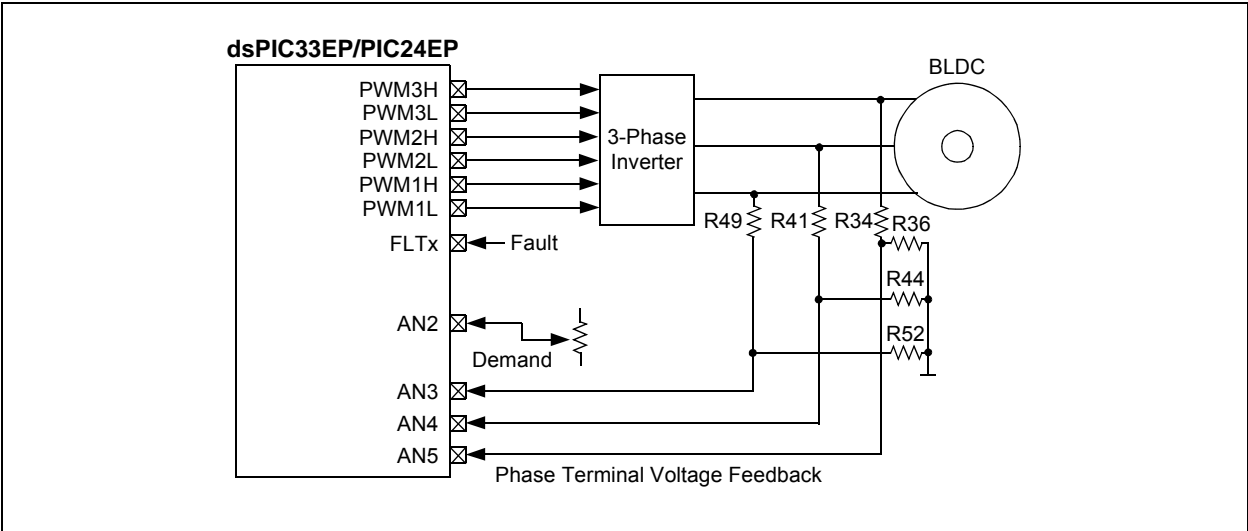


FIGURE 2-8: BEMF VOLTAGE MEASURED USING THE ADC MODULE



REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

- bit 2 **SFA:** Stack Frame Active Status bit
1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space
- bit 1 **RND:** Rounding Mode Select bit⁽¹⁾
1 = Biased (conventional) rounding is enabled
0 = Unbiased (convergent) rounding is enabled
- bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit⁽¹⁾
1 = Integer mode is enabled for DSP multiply
0 = Fractional mode is enabled for DSP multiply

- Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
2: This bit is always read as '0'.
3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000	
CORCON	0044	VAR	—	US<1:0>		EDT	DL<2:0>			SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF	0020	
MODCON	0046	XMODEN	YMODEN	—	—	BWM<3:0>				YWM<3:0>				XWM<3:0>				0000	
XMODSRT	0048	XMODSRT<15:0>																—	0000
XMODEND	004A	XMODEND<15:0>																—	0001
YMODSRT	004C	YMODSRT<15:0>																—	0000
YMODEND	004E	YMODEND<15:0>																—	0001
XBREV	0050	BREN	XBREV<14:0>																0000
DISCNT	0052	—	—	DISCNT<13:0>															0000
TBLPAG	0054	—	—	—	—	—	—	—	—	TBLPAG<7:0>									0000
MSTRPR	0058	MSTRPR<15:0>																0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-2: CPU CORE REGISTER MAP FOR PIC24EPXXXGP/MC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
W0	0000	W0 (WREG)																xxxx	
W1	0002	W1																xxxx	
W2	0004	W2																xxxx	
W3	0006	W3																xxxx	
W4	0008	W4																xxxx	
W5	000A	W5																xxxx	
W6	000C	W6																xxxx	
W7	000E	W7																xxxx	
W8	0010	W8																xxxx	
W9	0012	W9																xxxx	
W10	0014	W10																xxxx	
W11	0016	W11																xxxx	
W12	0018	W12																xxxx	
W13	001A	W13																xxxx	
W14	001C	W14																xxxx	
W15	001E	W15																xxxx	
SPLIM	0020	SPLIM<15:0>																0000	
PCL	002E	PCL<15:1>																—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH<6:0>							0000	
DSRPAG	0032	—	—	—	—	—	—	DSRPAG<9:0>										0001	
DSWPAG	0034	—	—	—	—	—	—	—	DSWPAG<8:0>										0001
RCOUNT	0036	RCOUNT<15:0>																0000	
SR	0042	—	—	—	—	—	—	—	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000	
CORCON	0044	VAR	—	—	—	—	—	—	—	—	—	—	—	IPL3	SFA	—	—	0020	
DISICNT	0052	—	—	DISICNT<13:0>														0000	
TBLPAG	0054	—	—	—	—	—	—	—	—	TBLPAG<7:0>									0000
MSTRPR	0058	MSTRPR<15:0>																0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBT	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR<3:0>				VECNUM<7:0>								0000

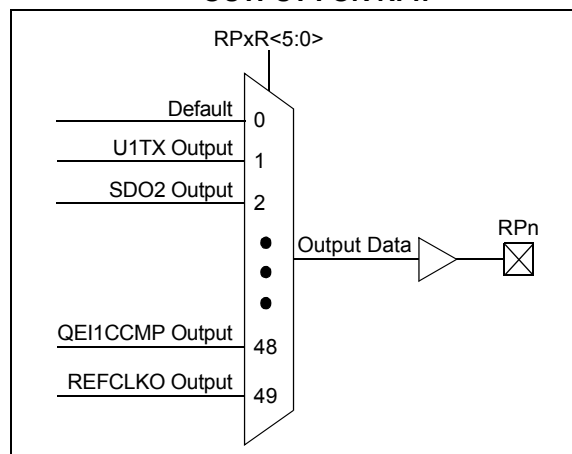
Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

11.4.4.2 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 11-18 through Register 11-27). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 11-3: MULTIPLEXING REMAPPABLE OUTPUT FOR RPn



11.4.4.3 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPnR<5:0>	Output Name
Default PORT	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
U2TX	000011	RPn tied to UART2 Transmit
SDO2	001000	RPn tied to SPI2 Data Output
SCK2	001001	RPn tied to SPI2 Clock Output
SS2	001010	RPn tied to SPI2 Slave Select
C1TX ⁽²⁾	001110	RPn tied to CAN1 Transmit
OC1	010000	RPn tied to Output Compare 1 Output
OC2	010001	RPn tied to Output Compare 2 Output
OC3	010010	RPn tied to Output Compare 3 Output
OC4	010011	RPn tied to Output Compare 4 Output
C1OUT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
SYNCO1 ⁽¹⁾	101101	RPn tied to PWM Primary Time Base Sync Output
QE1CCMP ⁽¹⁾	101111	RPn tied to QE1 Counter Comparator Output
REFCLKO	110001	RPn tied to Reference Clock Output
C4OUT	110010	RPn tied to Comparator Output 4

Note 1: This function is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This function is available in dsPIC33EPXXXGP/MC50X devices only.

REGISTER 11-10: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	U1RXR<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **U1RXR<6:0>:** Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-11: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	U2RXR<6:0>							
bit 7								bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **U2RXR<6:0>:** Assign UART2 Receive (U2RX) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER⁽²⁾

R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD1 ⁽¹⁾	PMOD0 ⁽¹⁾	OVRENH	OVRENL
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

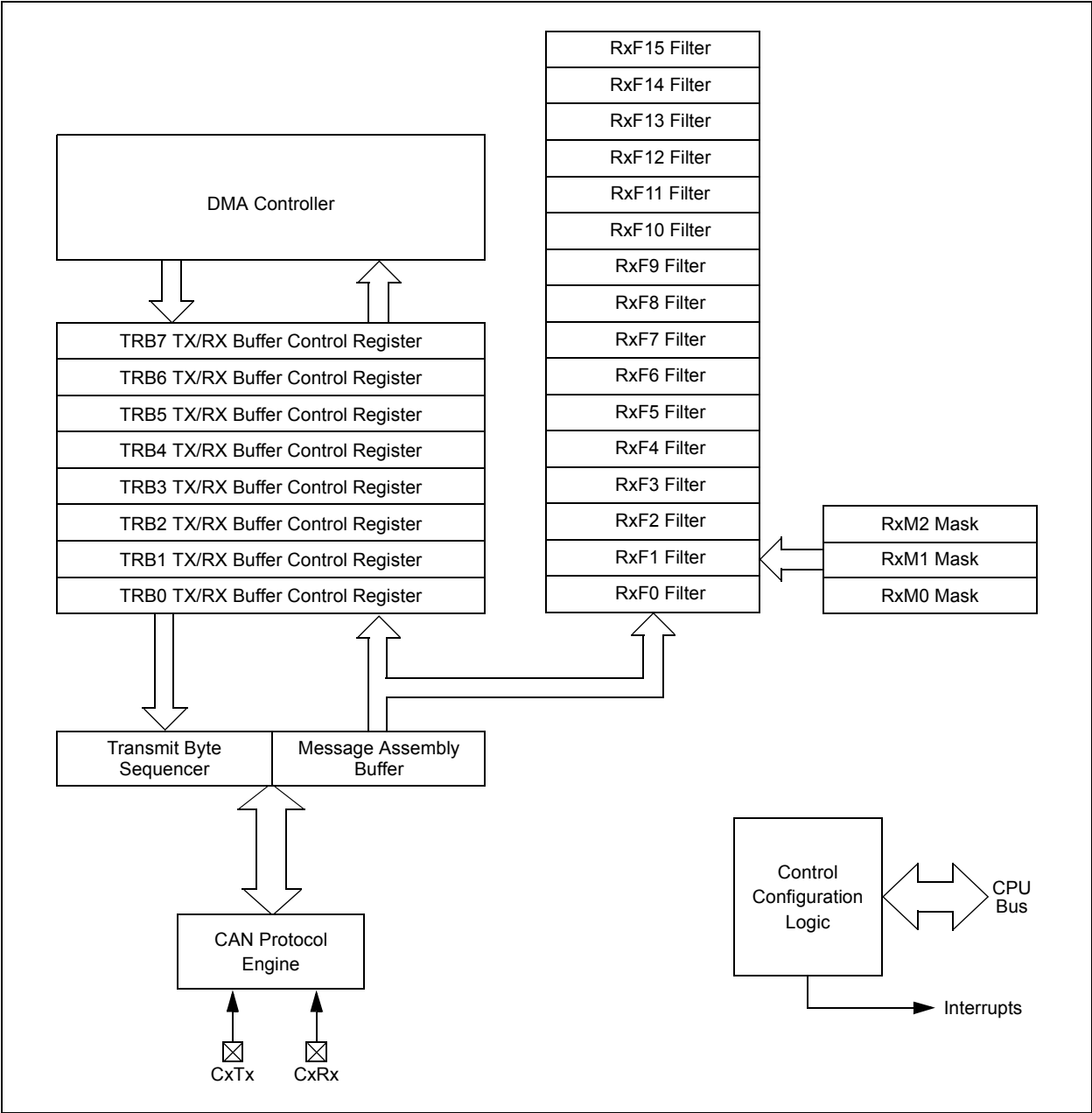
x = Bit is unknown

- bit 15 **PENH:** PWMxH Output Pin Ownership bit
1 = PWMx module controls PWMxH pin
0 = GPIO module controls PWMxH pin
- bit 14 **PENL:** PWMxL Output Pin Ownership bit
1 = PWMx module controls PWMxL pin
0 = GPIO module controls PWMxL pin
- bit 13 **POLH:** PWMxH Output Pin Polarity bit
1 = PWMxH pin is active-low
0 = PWMxH pin is active-high
- bit 12 **POLL:** PWMxL Output Pin Polarity bit
1 = PWMxL pin is active-low
0 = PWMxL pin is active-high
- bit 11-10 **PMOD<1:0>:** PWMx # I/O Pin Mode bits⁽¹⁾
11 = Reserved; do not use
10 = PWMx I/O pin pair is in the Push-Pull Output mode
01 = PWMx I/O pin pair is in the Redundant Output mode
00 = PWMx I/O pin pair is in the Complementary Output mode
- bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
1 = OVRDAT<1> controls output on PWMxH pin
0 = PWMx generator controls PWMxH pin
- bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
1 = OVRDAT<0> controls output on PWMxL pin
0 = PWMx generator controls PWMxL pin
- bit 7-6 **OVRDAT<1:0>:** Data for PWMxH, PWMxL Pins if Override is Enabled bits
If OVRRENH = 1, PWMxH is driven to the state specified by OVRDAT<1>.
If OVRRENL = 1, PWMxL is driven to the state specified by OVRDAT<0>.
- bit 5-4 **FLTDAT<1:0>:** Data for PWMxH and PWMxL Pins if FLTMOD is Enabled bits
If Fault is active, PWMxH is driven to the state specified by FLTDAT<1>.
If Fault is active, PWMxL is driven to the state specified by FLTDAT<0>.
- bit 3-2 **CLDAT<1:0>:** Data for PWMxH and PWMxL Pins if CLMOD is Enabled bits
If current-limit is active, PWMxH is driven to the state specified by CLDAT<1>.
If current-limit is active, PWMxL is driven to the state specified by CLDAT<0>.

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).

Note 2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

FIGURE 21-1: ECAN™ MODULE BLOCK DIAGRAM



REGISTER 21-16: CxRXFnSID: ECANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15						bit 8	

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	EXIDE	—	EID17	EID16
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5

SID<10:0>: Standard Identifier bits

1 = Message address bit, SIDx, must be '1' to match filter

0 = Message address bit, SIDx, must be '0' to match filter

bit 4

Unimplemented: Read as '0'

bit 3

EXIDE: Extended Identifier Enable bit

If MIDE = 1:

1 = Matches only messages with Extended Identifier addresses

0 = Matches only messages with Standard Identifier addresses

If MIDE = 0:

Ignores EXIDE bit.

bit 2

Unimplemented: Read as '0'

bit 1-0

EID<17:16>: Extended Identifier bits

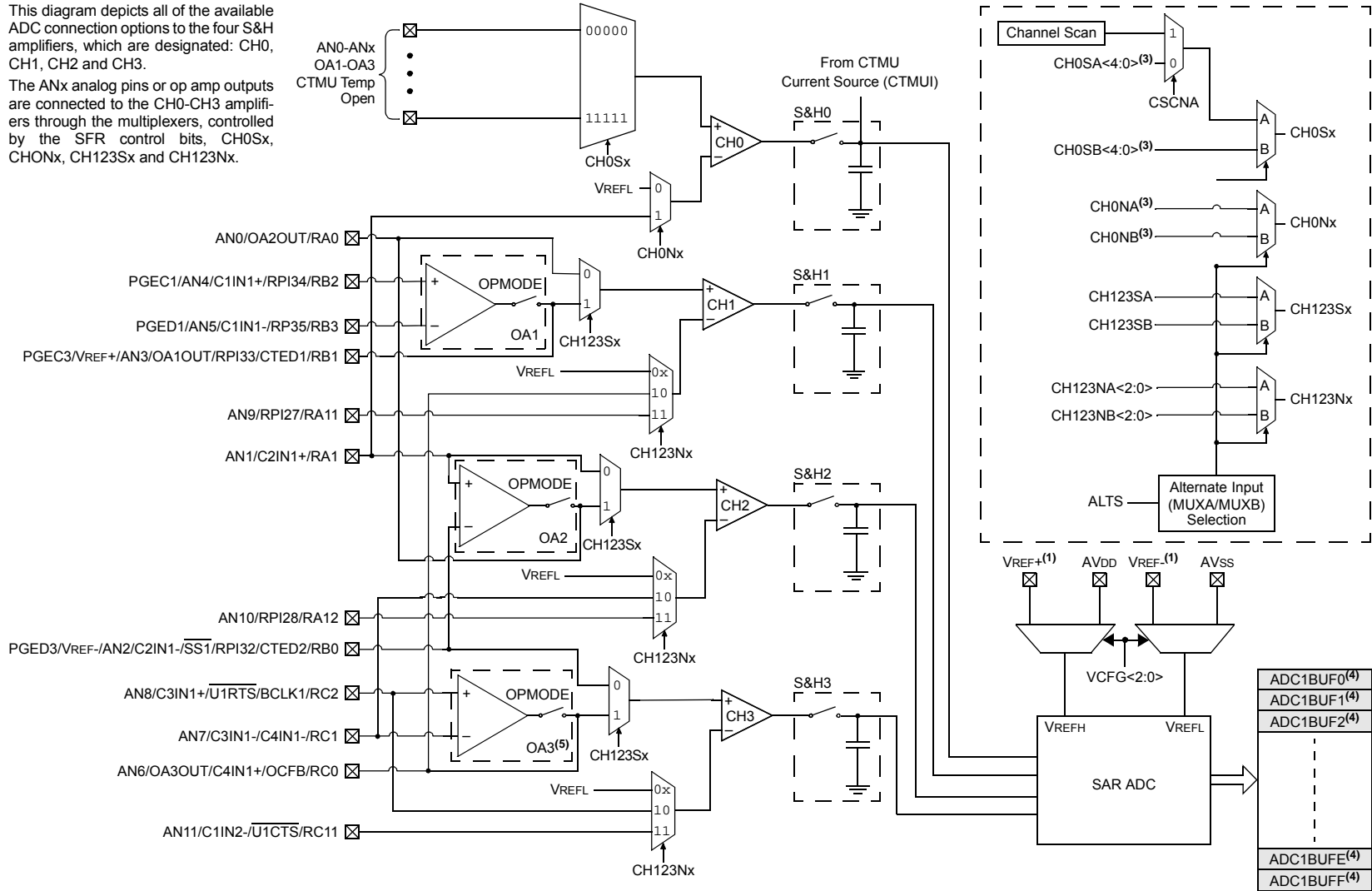
1 = Message address bit, EIDx, must be '1' to match filter

0 = Message address bit, EIDx, must be '0' to match filter

FIGURE 23-1: ADC MODULE BLOCK DIAGRAM WITH CONNECTION OPTIONS FOR ANx PINS AND OP AMPS

This diagram depicts all of the available ADC connection options to the four S&H amplifiers, which are designated: CH0, CH1, CH2 and CH3.

The ANx analog pins or op amp outputs are connected to the CH0-CH3 amplifiers through the multiplexers, controlled by the SFR control bits, CH0Sx, CH0Nx, CH123Sx and CH123Nx.



- Note**
- 1: VREF+, VREF- inputs can be multiplexed with other analog inputs.
 - 2: Channels 1, 2 and 3 are not applicable for the 12-bit mode of operation.
 - 3: These bits can be updated with Step commands from the PTG module. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.
 - 4: When ADDMAEN (AD1CON4<8>) = 1, enabling DMA, only ADC1BUF0 is used.
 - 5: OA3 is not available for 28-pin devices.

NOTES:

27.5 Watchdog Timer (WDT)

For dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

27.5.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT Time-out period (TWDT), as shown in Parameter SY12 in Table 30-22.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

27.5.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3,2>) needs to be cleared in software after the device wakes up.

27.5.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

27.5.4 WDT WINDOW

The Watchdog Timer has an optional Windowed mode, enabled by programming the WINDIS bit in the WDT Configuration register (FWDT<6>). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window select bits (WDTWIN<1:0>).

FIGURE 27-2: WDT BLOCK DIAGRAM

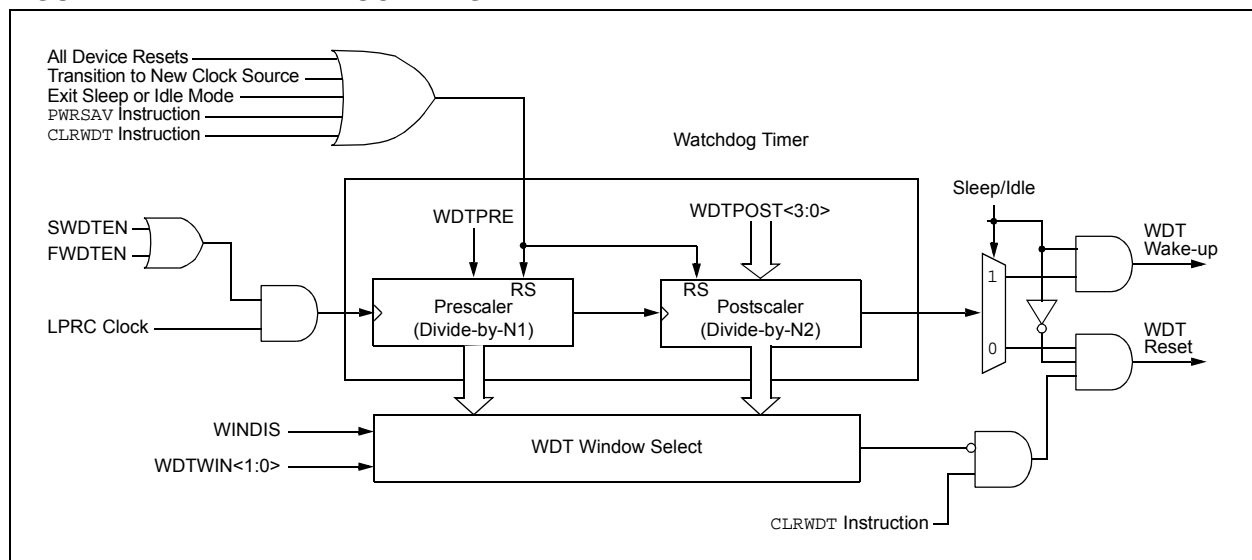


TABLE 28-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
1	ADD	ADD Acc ⁽¹⁾	Add Accumulators	1	1	OA,OB,SA,SB
		ADD f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD f, WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD #lit10, Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD Wb, Ws, Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD Wb, #lit5, Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD Wso, #Slit4, Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC f, WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC #lit10, Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC Wb, Ws, Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC Wb, #lit5, Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND f	f = f .AND. WREG	1	1	N,Z
		AND f, WREG	WREG = f .AND. WREG	1	1	N,Z
		AND #lit10, Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND Wb, Ws, Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND Wb, #lit5, Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR f, WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR Ws, Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR Wb, Wns, Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR Wb, #lit5, Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR f, #bit4	Bit Clear f	1	1	None
		BCLR Ws, #bit4	Bit Clear Ws	1	1	None
6	BRA	BRA C, Expr	Branch if Carry	1	1 (4)	None
		BRA GE, Expr	Branch if greater than or equal	1	1 (4)	None
		BRA GEU, Expr	Branch if unsigned greater than or equal	1	1 (4)	None
		BRA GT, Expr	Branch if greater than	1	1 (4)	None
		BRA GTU, Expr	Branch if unsigned greater than	1	1 (4)	None
		BRA LE, Expr	Branch if less than or equal	1	1 (4)	None
		BRA LEU, Expr	Branch if unsigned less than or equal	1	1 (4)	None
		BRA LT, Expr	Branch if less than	1	1 (4)	None
		BRA LTU, Expr	Branch if unsigned less than	1	1 (4)	None
		BRA N, Expr	Branch if Negative	1	1 (4)	None
		BRA NC, Expr	Branch if Not Carry	1	1 (4)	None
		BRA NN, Expr	Branch if Not Negative	1	1 (4)	None
		BRA NOV, Expr	Branch if Not Overflow	1	1 (4)	None
		BRA NZ, Expr	Branch if Not Zero	1	1 (4)	None
		BRA OA, Expr ⁽¹⁾	Branch if Accumulator A overflow	1	1 (4)	None
		BRA OB, Expr ⁽¹⁾	Branch if Accumulator B overflow	1	1 (4)	None
		BRA OV, Expr ⁽¹⁾	Branch if Overflow	1	1 (4)	None
		BRA SA, Expr ⁽¹⁾	Branch if Accumulator A saturated	1	1 (4)	None
		BRA SB, Expr ⁽¹⁾	Branch if Accumulator B saturated	1	1 (4)	None
		BRA Expr	Branch Unconditionally	1	4	None
		BRA Z, Expr	Branch if Zero	1	1 (4)	None
		BRA Wn	Computed Branch	1	4	None
7	BSET	BSET f, #bit4	Bit Set f	1	1	None
		BSET Ws, #bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C Ws, Wb	Write C bit to Ws<Wb>	1	1	None
		BSW.Z Ws, Wb	Write Z bit to Ws<Wb>	1	1	None

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
46	MOV	MOV <i>f</i> , <i>Wn</i>	Move <i>f</i> to <i>Wn</i>	1	1	None
		MOV <i>f</i>	Move <i>f</i> to <i>f</i>	1	1	None
		MOV <i>f</i> , WREG	Move <i>f</i> to WREG	1	1	None
		MOV #lit16, <i>Wn</i>	Move 16-bit literal to <i>Wn</i>	1	1	None
		MOV.b #lit8, <i>Wn</i>	Move 8-bit literal to <i>Wn</i>	1	1	None
		MOV <i>Wn</i> , <i>f</i>	Move <i>Wn</i> to <i>f</i>	1	1	None
		MOV <i>Wso</i> , <i>Wdo</i>	Move <i>Ws</i> to <i>Wd</i>	1	1	None
		MOV WREG, <i>f</i>	Move WREG to <i>f</i>	1	1	None
		MOV.D <i>Wns</i> , <i>Wd</i>	Move Double from <i>W(ns):W(ns + 1)</i> to <i>Wd</i>	1	2	None
		MOV.D <i>Ws</i> , <i>Wnd</i>	Move Double from <i>Ws</i> to <i>W(nd + 1):W(nd)</i>	1	2	None
47	MOVPAG	MOVPAG #lit10, DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPAG #lit9, DSWPAG	Move 9-bit literal to DSWPAG	1	1	None
		MOVPAG #lit8, TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPAG <i>Ws</i> , DSRPAG	Move <i>Ws</i> <9:0> to DSRPAG	1	1	None
		MOVPAG <i>Ws</i> , DSWPAG	Move <i>Ws</i> <8:0> to DSWPAG	1	1	None
		MOVPAG <i>Ws</i> , TBLPAG	Move <i>Ws</i> <7:0> to TBLPAG	1	1	None
48	MOVSAC	MOVSAC <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> , AWB ⁽¹⁾	Prefetch and store accumulator	1	1	None
49	MPY	MPY <i>Wm</i> * <i>Wn</i> , <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> ⁽¹⁾	Multiply <i>Wm</i> by <i>Wn</i> to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
		MPY <i>Wm</i> * <i>Wm</i> , <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> ⁽¹⁾	Square <i>Wm</i> to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
50	MPY.N	MPY.N <i>Wm</i> * <i>Wn</i> , <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> ⁽¹⁾	-(Multiply <i>Wm</i> by <i>Wn</i>) to Accumulator	1	1	None
51	MSC	MSC <i>Wm</i> * <i>Wm</i> , <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> , AWB ⁽¹⁾	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB,SA,SB,SAB

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 30-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended	
Parameter No.	Typ.	Max.	Units	Conditions
Power-Down Current (IPD)⁽¹⁾ – dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X and PIC24EP32GP/MC20X				
DC60d	30	100	μA	-40°C
DC60a	35	100	μA	+25°C
DC60b	150	200	μA	+85°C
DC60c	250	500	μA	+125°C
Power-Down Current (IPD)⁽¹⁾ – dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X and PIC24EP64GP/MC20X				
DC60d	25	100	μA	-40°C
DC60a	30	100	μA	+25°C
DC60b	150	350	μA	+85°C
DC60c	350	800	μA	+125°C
Power-Down Current (IPD)⁽¹⁾ – dsPIC33EP128GP50X, dsPIC33EP128MC20X/50X and PIC24EP128GP/MC20X				
DC60d	30	100	μA	-40°C
DC60a	35	100	μA	+25°C
DC60b	150	350	μA	+85°C
DC60c	550	1000	μA	+125°C
Power-Down Current (IPD)⁽¹⁾ – dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X and PIC24EP256GP/MC20X				
DC60d	35	100	μA	-40°C
DC60a	40	100	μA	+25°C
DC60b	250	450	μA	+85°C
DC60c	1000	1200	μA	+125°C
Power-Down Current (IPD)⁽¹⁾ – dsPIC33EP512GP50X, dsPIC33EP512MC20X/50X and PIC24EP512GP/MC20X				
DC60d	40	100	μA	-40°C
DC60a	45	100	μA	+25°C
DC60b	350	800	μA	+85°C
DC60c	1100	1500	μA	+125°C

Note 1: IPD (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- MCLR = VDD, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all set)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

32.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 32-1: V_{OH} – 4x DRIVER PINS

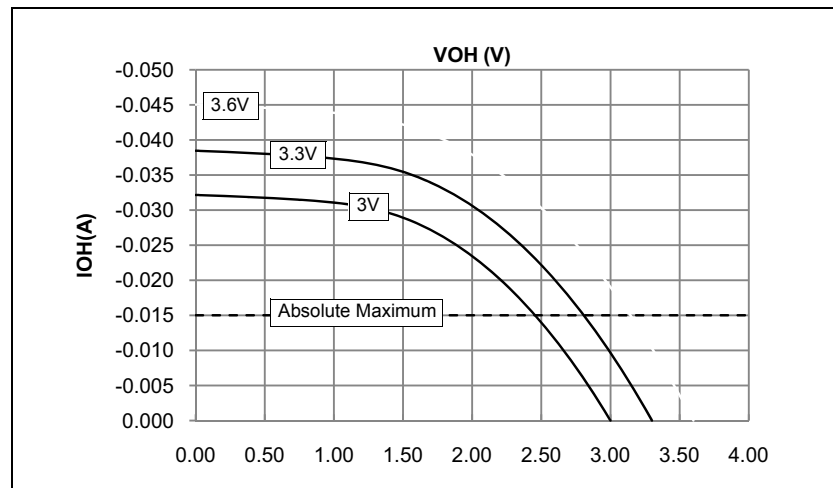


FIGURE 32-3: V_{OL} – 4x DRIVER PINS

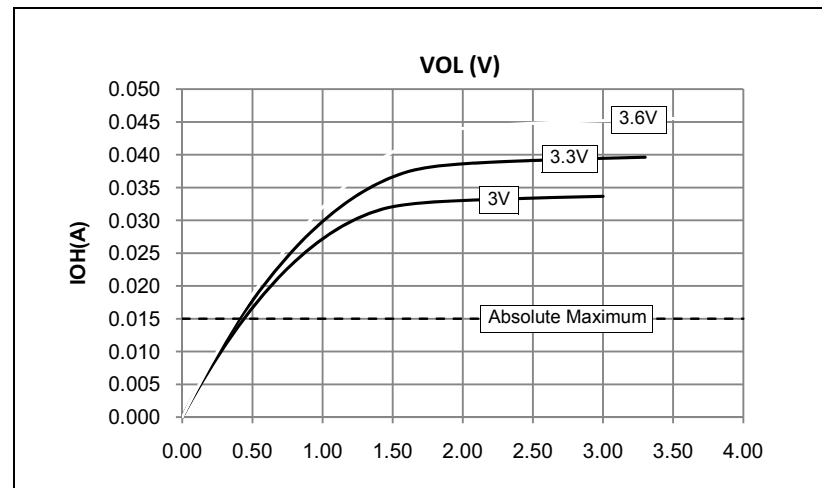


FIGURE 32-2: V_{OH} – 8x DRIVER PINS

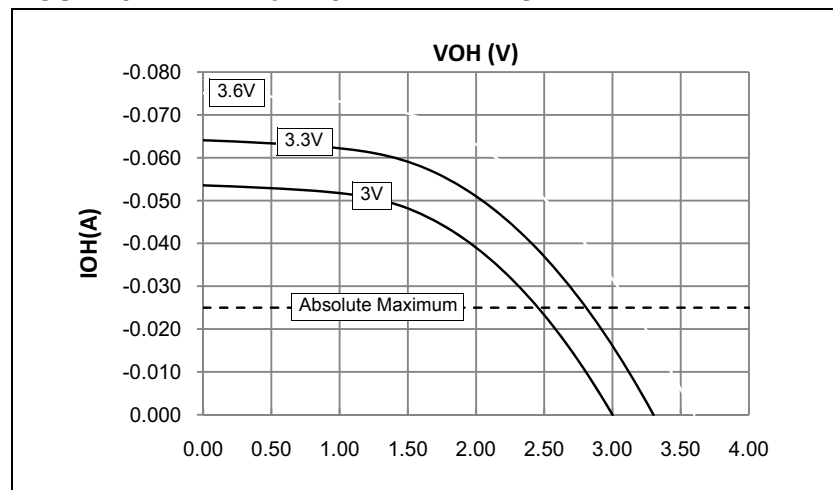
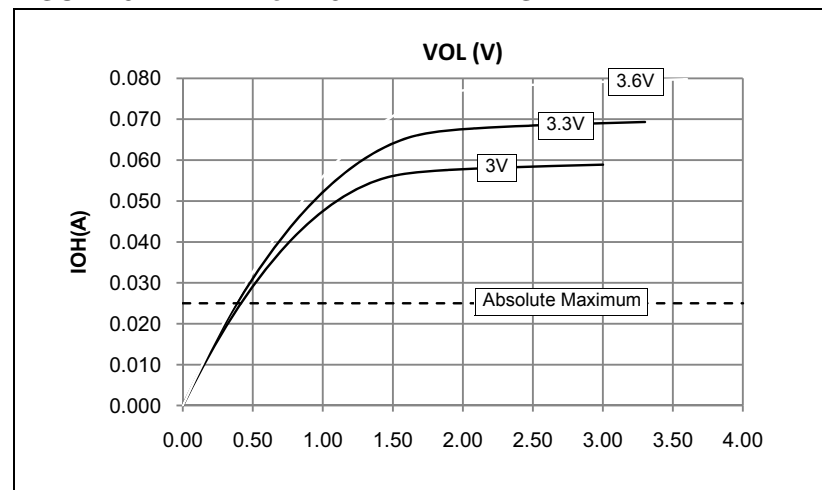


FIGURE 32-4: V_{OL} – 8x DRIVER PINS



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Printed on recycled paper.

ISBN: 9781620773949

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