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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc202t-i-ss

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2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μ F to 47 μ F.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohm) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor greater than 4.7 μ F (10 μ F is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 30.0** "**Electrical Characteristics**" for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 27.3 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

- Device Reset
- Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.





2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (VIH) and Voltage Input Low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB[®] PICkit[™] 3, MPLAB ICD 3, or MPLAB REAL ICE[™].

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- "Using MPLAB[®] ICD 3" (poster) DS51765
- "MPLAB[®] ICD 3 Design Advisory" DS51764
- "MPLAB[®] REAL ICE[™] In-Circuit Emulator User's Guide" DS51616
- "Using MPLAB[®] REAL ICE™ In-Circuit Emulator" (poster) DS51749

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator. For details, see **Section 9.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.



SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



FIGURE 2-5: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER









FIGURE 4-10: DATA MEMORY MAP FOR dsPIC33EP256MC20X/50X AND dsPIC33EP256GP50X DEVICES

TABLE	4-Z:	CPU		EGISTEI	RIMAP		Z4EPX		C20X D	EVICES	ONLT							
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000		W0 (WREG) xxxx															
W1	0002		W1 xxxx															
W2	0004								W2									xxxx
W3	0006								W3									xxxx
W4	8000		W4 xxxx											xxxx				
W5	000A		W5 xxxx															
W6	000C								W6									xxxx
W7	000E								W7									xxxx
W8	0010		W8 xxxx															
W9	0012		W9 xxxx															
W10	0014		W10 xxxx									xxxx						
W11	0016		W11 xxxx									xxxx						
W12	0018								W12									xxxx
W13	001A								W13									xxxx
W14	001C								W14									xxxx
W15	001E								W15									xxxx
SPLIM	0020								SPLIM<1	5:0>								0000
PCL	002E			•			•	P	CL<15:1>								—	0000
PCH	0030	—	—	—	—	—	—		—	—				PCH<6:0>				0000
DSRPAG	0032	—	—	—	—	—	—					DSRPA	G<9:0>					0001
DSWPAG	0034	—	—	—	—	—	—	—				DS	SWPAG<8:0)>				0001
RCOUNT	0036			•			•		RCOUNT<	15:0>								0000
SR	0042	—	—		—	_	—	_	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	С	0000
CORCON	0044	VAR	_	—	—	—	—	_	—	—	—	—	—	IPL3	SFA	—	—	0020
DISICNT	0052	—	-							DISICNT	<13:0>							0000
TBLPAG	0054	—	—	—	—	—	—	—	—				TBLPA	G<7:0>				0000
MSTRPR	0058	MSTRPR<15:0> 0000																

D I -4.0 - -

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC35	0886	—		JTAGIP<2:0)>	—		ICDIP<2:0	>	—	_	—	—	_	_	—	-	4400
IPC36	0888	_		PTG0IP<2:0)>	_	PT	GWDTIP<	2:0>	_	PT	GSTEPIP<2	::0>	_	_	_	_	4440
IPC37	088A	_	_	_	_	_	F	PTG3IP<2:	0>	_		PTG2IP<2:0	>	- PTG1IP<2:0>			0444	
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	_	_	_	_	_	_	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	_	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	_	—	_	—	—	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	_	_	_	—	_	—	_	DAE	DOOVR	—	—	—		0000
INTCON4	08C6	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	SGHT	0000
INTTREG	08C8	_	_	_	_		ILR<	3:0>					VECN	IUM<7:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- · Register Indirect
- · Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal
- Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

11.7 **Peripheral Pin Select Registers**

REGISTER 11-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				INT1R<6:0>			
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	-	—	—	_	—	—
bit 7	•		•	•			bit 0

Legend:

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 14-8 INT1R<6:0>: Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121 0000001 = Input tied to CMP1 0000000 = Input tied to Vss bit 7-0 Unimplemented: Read as '0'

NOTES:

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

bit 6-4	SYNCSRC<2:0>: Synchronous Source Selection bits ⁽¹⁾ 111 = Reserved
	•
	• 100 = Reserved 011 = PTGO17 ⁽²⁾ 010 = PTGO16 ⁽²⁾ 001 = Reserved 000 = SYNCI1 input from PPS
bit 3-0	<pre>SEVTPS<3:0>: PWMx Special Event Trigger Output Postscaler Select bits⁽¹⁾ 1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event</pre>
	0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event 0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

- **Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.
 - 2: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-22: CxRXFUL1: ECANx RECEIVE BUFFER FULL REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8
bit 15							bit 8

| R/C-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| RXFUL7 | RXFUL6 | RXFUL5 | RXFUL4 | RXFUL3 | RXFUL2 | RXFUL1 | RXFUL0 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-0 **RXFUL<15:0>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

REGISTER 21-23: CxRXFUL2: ECANx RECEIVE BUFFER FULL REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL31 | RXFUL30 | RXFUL29 | RXFUL28 | RXFUL27 | RXFUL26 | RXFUL25 | RXFUL24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL23 | RXFUL22 | RXFUL21 | RXFUL20 | RXFUL19 | RXFUL18 | RXFUL17 | RXFUL16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-0 **RXFUL<31:16>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

24.3 PTG Control Registers

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT ⁽²⁾	PTGSSEN ⁽³⁾	PTGIVIS
bit 15							bit 8
R/W-0	HS-0	U-0	U-0	U-0	U-0	R/V	V-0
PTGSTRT	PTGWDTO	_	_	_	_	PTGITM1 ⁽¹⁾	PTGITM0 ⁽¹⁾

h	it	7
υ	π.	1

Legend:	HS = Hardware Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15		PTGEN: Module Enable bit
		1 = PTG module is enabled
		0 = PTG module is disabled
bit 14		Unimplemented: Read as '0'
bit 13		PTGSIDL: PTG Stop in Idle Mode bit
		 1 = Discontinues module operation when device enters Idle mode 0 = Continues module operation in Idle mode
bit 12		PTGTOGL: PTG TRIG Output Toggle Mode bit
		 1 = Toggle state of the PTGOx for each execution of the PTGTRIG command 0 = Each execution of the PTGTRIG command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits
bit 11		Unimplemented: Read as '0'
bit 10		PTGSWT: PTG Software Trigger bit ⁽²⁾
		1 = Triggers the PTG module
		0 = No action (clearing this bit will have no effect)
bit 9		PTGSSEN: PTG Enable Single-Step bit ⁽³⁾
		1 = Enables Single-Step mode
		0 = Disables Single-Step mode
bit 8		PTGIVIS: PTG Counter/Timer Visibility Control bit
		1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)
		 Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those limit registers
bit 7		PTGSTRT: PTG Start Sequencer bit
		1 = Starts to sequentially execute commands (Continuous mode)0 = Stops executing commands
bit 6		PTGWDTO: PTG Watchdog Timer Time-out Status bit
		1 = PTG Watchdog Timer has timed out
		0 = PTG watchdog Timer has not timed out.
bit 5-2		Unimplemented: Read as '0'
Note	1: Th	nese bits apply to the PTGWHI and PTGWLO commands only.
	2: Th	is bit is only used with the PTGCTRL step command software trigger option.

3: Use of the PTG Single-Step mode is reserved for debugging tools only.

bit 0

27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3:USER ID WORDS REGISTER
MAP

File Name	Address	Bits 23-16	Bits 15-0
FUID0	0x800FF8	—	UID0
FUID1	0x800FFA	—	UID1
FUID2	0x800FFC	—	UID2
FUID3	0x800FFE	—	UID3

Legend: — = unimplemented, read as '1'.

27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an onchip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE

REGULATOR^(1,2,3)



27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

28.0 INSTRUCTION SET SUMMARY

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. То complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Familv Reference Manual', which is available from the Microchip web site (www.microchip.com).

The dsPIC33EP instruction set is almost identical to that of the dsPIC30F and dsPIC33F. The PIC24EP instruction set is almost identical to that of the PIC24F and PIC24H.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- · Word or byte-oriented operations
- · Bit-oriented operations
- · Literal operations
- DSP operations
- · Control operations

Table 28-1 lists the general symbols used in describing the instructions.

The dsPIC33E instruction set summary in Table 28-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register 'Wb' without any address modifier
- The second source operand, which is typically a register 'Ws' with or without an address modifier
- The destination of the result, which is typically a register 'Wd' with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- · The file register specified by the value 'f'
- The destination, which could be either the file register 'f' or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/ shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register 'Wb')

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register 'Wb' without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register 'Wd' with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- · The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register 'Wn' or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

TABLE 30-46:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)TIMING REQUIREMENTS

АС СНА				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	FscP	Maximum SCK1 Input Frequency	—	—	Lesserof FP or 11	MHz	(Note 3)	
SP72	TscF	SCK1 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK1 Input Rise Time	—	-	—	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO1 Data Output Rise Time	—	-	—	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	-	—	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	-	—	ns		
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns		
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)	
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	—	ns	(Note 4)	
SP60	TssL2doV	SDO1 Data Output Valid after SS1 Edge	—	_	50	ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

33.0 PACKAGING INFORMATION

33.1 Package Marking Information

28-Lead SPDIP



28-Lead SOIC (.300")



28-Lead SSOP



Example dsPIC33EP64GP 502-I/SP@3 1310017

Example



Example



28-Lead QFN-S (6x6x0.9 mm)



Example



Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the even be carried characters	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available s for customer-specific information.

44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-157C Sheet 1 of 2

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
	Dimension Limits	MIN	NOM	MAX	
Number of Leads	N	44			
Lead Pitch	e		0.80 BSC		
Overall Height	A	-	-	1.20	
Molded Package Thickness	A2	0.95	1.00	1.05	
Standoff	A1	0.05	-	0.15	
Foot Length	L	0.45	0.60	0.75	
Footprint	L1		1.00 REF		
Foot Angle	ф	0°	3.5°	7°	
Overall Width	E		12.00 BSC		
Overall Length	D		12.00 BSC		
Molded Package Width	E1		10.00 BSC		
Molded Package Length	D1	10.00 BSC			
Lead Thickness	С	0.09 – 0.20			
Lead Width	b	0.30	0.37	0.45	
Mold Draft Angle Top	α	11°	12°	13°	
Mold Draft Angle Bottom	β	11°	12°	13°	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	
Number of Pins	N	48			
Pitch	е	0.40 BSC			
Overall Height	Α	0.45	0.50	0.55	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3	0.127 REF			
Overall Width	E	6.00 BSC			
Exposed Pad Width	E2	4.45	4.60	4.75	
Overall Length	D	6.00 BSC			
Exposed Pad Length	D2	4.45	4.60	4.75	
Contact Width	b	0.15	0.20	0.25	
Contact Length	L	0.30	0.40	0.50	
Contact-to-Exposed Pad	K	0.20	-	_	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-153A Sheet 2 of 2