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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc203-e-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### Pin Diagrams (Continued)



# 3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

# 3.1 Registers

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls.

# 3.2 Instruction Set

The instruction set for dsPIC33EPXXXGP50X and dsPIC33EPXXXMC20X/50X devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The instruction set for PIC24EPXXXGP/MC20X devices has the MCU class of instructions only and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

# 3.3 Data Space Addressing

The base Data Space can be addressed as 64 Kbytes (32K words).

The Data Space includes two ranges of memory, referred to as X and Y data memory. Each memory range is accessible through its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Spaces have memory locations that are device-specific, and are described further in the data memory maps in **Section 4.2 "Data Address Space"**.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 32-Kbyte aligned program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to the "**Data Memory**" (DS70595) and "**Program Memory**" (DS70613) sections in the "*dsPIC33/PIC24 Family Reference Manual*" for more details on EDS, PSV and table accesses.

On the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms. PIC24EPXXXGP/MC20X devices do not support Modulo and Bit-Reversed Addressing.

# 3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- · Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

# 3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

#### 3.6.1 KEY RESOURCES

- "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

TABLE 4	4-31:	PER	IPHERA	L PIN S	ELECT	INPUT F	REGISTI	ER MAP	FOR ds	sPIC33E	PXXXG	P50X D	EVICES	3 ONLY	

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—				INT1R<6:0>					—	—	—	—	_			0000
RPINR1	06A2		_								INT2R<6:0>							0000
RPINR3	06A6		_									0000						
RPINR7	06AE			IC2R<6:0>							IC1R<6:0>							0000
RPINR8	06B0	_		IC4R<6:0>						_				IC3R<6:0>				0000
RPINR11	06B6	_	_	_	_	_	-	_	_	_			(	DCFAR<6:0	>			0000
RPINR18	06C4	_	_	_	_	_	-	_	_	_	U1RXR<6:0>						0000	
RPINR19	06C6	_	_	_	_	_	-	_	_	_			l	J2RXR<6:0	>			0000
RPINR22	06CC	_			S	CK2INR<6:0	)>			_				SDI2R<6:0>				0000
RPINR23	06CE	_	_	_	_	_	-	_	_	— SS2R<6:0>							0000	
RPINR26	06D4	_	_	_		_	—		_		- C1RXR<6:0>						0000	

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### **TABLE 4-32:** PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	PINR0 06A0 — INT1R<6:0>							_	—	—	—			_	_	0000		
RPINR1	06A2	_	_						_	_				INT2R<6:0>				0000
RPINR3	06A6	_	_							_	T2CKR<6:0>							0000
RPINR7	06AE	_		IC2R<6:0>						_	IC1R<6:0>						0000	
RPINR8	06B0	_				IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6	_	_	_	_	_	_	_	_	_			(	DCFAR<6:0	>			0000
RPINR12	06B8	_		FLT2R<6:0>						_				FLT1R<6:0>	•			0000
RPINR14	06BC	_			(	QEB1R<6:0	>			_			(	QEA1R<6:0	>			0000
RPINR15	06BE	_			Н	OME1R<6:(	)>			_			I	NDX1R<6:0	>			0000
RPINR18	06C4	_	_	_	_	_	_	_	_	_	U1RXR<6:0>						0000	
RPINR19	06C6	_	_	_	_	_	_	_	_	_			ι	J2RXR<6:0	>			0000
RPINR22	06CC	_			S	CK2INR<6:	0>			_				SDI2R<6:0>				0000
RPINR23	06CE	_	_	_	_	_	-	_	_	_				SS2R<6:0>				0000
RPINR26	06D4	_	_	— — — — — — — C1RXR<6:0>							0000							
RPINR37	06EA	_		SYNCI1R<6:0>						_	_	—			—	_	_	0000
RPINR38	06EC	—		DTCMP1R<6:0>						—						—	0000	
RPINR39	06EE	_		DTCMP3R<6:0>						_			D	CMP2R<6:	0>			0000

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

# REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 4	MATHERR: Math Error Status bit
	1 = Math error trap has occurred
	0 = Math error trap has not occurred
bit 3	ADDRERR: Address Error Trap Status bit
	<ul><li>1 = Address error trap has occurred</li><li>0 = Address error trap has not occurred</li></ul>
bit 2	STKERR: Stack Error Trap Status bit
	1 = Stack error trap has occurred
	0 = Stack error trap has not occurred
bit 1	<b>OSCFAIL:</b> Oscillator Failure Trap Status bit
	1 = Oscillator failure trap has occurred
	0 = Oscillator failure trap has not occurred
bit 0	Unimplemented: Read as '0'

Note 1: These bits are available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

# 8.0 DIRECT MEMORY ACCESS (DMA)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Direct Memory Access (DMA)" (DS70348) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The DMA Controller transfers data between Peripheral Data registers and Data Space SRAM

In addition, DMA can access the entire data memory space. The Data Memory Bus Arbiter is utilized when either the CPU or DMA attempts to access SRAM, resulting in potential DMA or CPU stalls.

The DMA Controller supports 4 independent channels. Each channel can be configured for transfers to or from selected peripherals. Some of the peripherals supported by the DMA Controller include:

- ECAN<sup>™</sup>
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI)
- UART
- Input Capture
- Output Compare

Refer to Table 8-1 for a complete list of supported peripherals.

# FIGURE 8-1: DMA CONTROLLER MODULE



#### REGISTER 11-7: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				FLT2R<6:0>			
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				FLT1R<6:0>			
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown
bit 15	Unimpleme	ented: Read as '	0'				
bit 14-8	FLT2R<6:0: (see Table 1	Assign PWM   1-2 for input pin	Fault 2 (FLT2 selection nur	) to the Corresp mbers)	onding RPn F	Pin bits	
	1111001 =	Input tied to RPI	121				
	•						
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss	5				
bit 7	Unimpleme	ented: Read as '	0'				
bit 6-0	FLT1R<6:0: (see Table 1	Second States	Fault 1 (FLT1 selection nur	) to the Corresp nbers)	onding RPn F	Pin bits	
	1111001 =	Input tied to RPI	121				
	•						
	-						
		Input tied to CM	P1				
	0000000 =	Input tied to Vss	;				

# 12.0 TIMER1

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated in Asynchronous Counter mode from an external clock source
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and the clock synchronization is performed after the prescaler
- A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- · Gated Timer mode
- Synchronous Counter mode
- · Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit setting for different operating modes are given in the Table 12-1.

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated Timer	0	1	х
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

#### TABLE 12-1: TIMER MODE SETTINGS

#### FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	_			DTR)	<13:8>		
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			DTR	2x<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

# REGISTER 16-10: DTRx: PWMx DEAD-TIME REGISTER

bit 15-14 Unimplemented: Read as '0'

bit 13-0 DTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

#### REGISTER 16-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			ALTDT	Rx<13:8>		
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			ALTDT	Rx<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	d as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-14 Unimplemented: Read as '0'

bit 13-0 ALTDTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	FRMPOL	_	_		_	
bit 15	·						bit 8
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
_	—	—	—	_	—	FRMDLY	SPIBEN
bit 7							bit 0
Legend:							
R = Readabl	le bit	W = Writable b	oit	U = Unimple	mented bit, rea	d as '0'	
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	FRMEN: Frai	med SPIx Supp	ort bit				
	1 = Framed S	SPIx support is e	enabled ( <mark>SSx</mark> disabled	pin is used as	Frame Sync p	ulse input/outpu	t)
bit 14	SPIFSD: Fra	me Svnc Pulse	Direction Cor	ntrol bit			
	1 = Frame Sy	ync pulse input (	(slave)				
hit 12	EPMPOL · Er	amo Syno Bulse	Dolority bit				
DIL 13	1 = Frame Sv	anne Sync Fuise					
	0 = Frame S	vnc pulse is acti	ve-low				
bit 12-2	Unimplemen	nted: Read as '0	)'				
bit 1	FRMDLY: Fra	ame Sync Pulse	Edge Select	bit			
	1 = Frame Sy 0 = Frame Sy	ync pulse coinci ync pulse prece	des with first des first bit cl	bit clock ock			
bit 0	SPIBEN: Enh	nanced Buffer E	nable bit				
	1 = Enhance	d buffer is enabl	led				
	0 = Enhance	d buffer is disab	led (Standard	l mode)			

#### REGISTER 18-3: SPIXCON2: SPIX CONTROL REGISTER 2

# 19.1 I<sup>2</sup>C Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

#### 19.1.1 KEY RESOURCES

- "Inter-Integrated Circuit (I<sup>2</sup>C)" (DS70330) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—		—	AMSK9	AMSK8
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0
bit 7							bit 0

#### REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 Unimplemented: Read as '0'

bit 9-0

AMSK<9:0>: Address Mask Select bits

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax + 1; bit match is required in this position

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	_	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0
bit 15							bit 8
U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	_	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 15-14	Unimplemen	ted: Read as '	0'				
bit 13-8	<b>FBP&lt;5:0&gt;:</b> F	IFO Buffer Poir	nter bits				
	011111 = RE	331 buffer					
	•	50 builer					
	•						
	•						
	000001 <b>= TR</b>	B1 buffer					
	000000 = TR	RB0 buffer					
bit 7-6	Unimplemen	ted: Read as '	0'				
bit 5-0	FNRB<5:0>:	FIFO Next Rea	ad Buffer Poin	ter bits			
	011111 <b>= RE</b>	331 buffer					
	011110 <b>= RE</b>	330 buffer					
	•						
	•						
	•						
	000001 = TR	(B1 buffer					
	000000 = TR						

#### REGISTER 21-5: CxFIFO: ECANx FIFO STATUS REGISTER

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

#### REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID7  | EID6  | EID5  | EID4  | EID3  | EID2  | EID1  | EID0  |
| bit 7 |       |       |       |       |       |       | bit 0 |

# Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-0 EID<15:0>: Extended Identifier bits

1 = Message address bit, EIDx, must be '1' to match filter

0 = Message address bit, EIDx, must be '0' to match filter

#### REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MSK<1:0>		F6MSI	K<1:0>	F5MSK<1:0>		F4MS	K<1:0>
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3M	SK<1:0>	F2MSI	K<1:0>	F1MS	K<1:0>	F0MS	K<1:0>
bit 7							bit 0
Legend:							
R = Readabl	le bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'	
-n = Value at	t POR	'1' = Bit is set	:	'0' = Bit is cleared		x = Bit is unknown	
bit 15-14	<b>F7MSK&lt;1:0:</b> 11 = Reserve 10 = Accepta 01 = Accepta 00 = Accepta	>: Mask Source ed ance Mask 2 re ance Mask 1 re ance Mask 0 re	for Filter 7 bi gisters contair gisters contair gisters contair	ts n mask n mask n mask			
bit 13-12	F6MSK<1:0	>: Mask Source	for Filter 6 bi	ts (same values	as bits<15:14	<b>!</b> >)	
bit 11-10	F5MSK<1:0	>: Mask Source	for Filter 5 bi	ts (same values	as bits<15:14	<b>!</b> >)	
bit 9-8	F4MSK<1:0	>: Mask Source	for Filter 4 bi	ts (same values	as bits<15:14	<b>!</b> >)	
bit 7-6	F3MSK<1:0:	>: Mask Source	for Filter 3 bi	ts (same values	s as bits<15:14	l>)	
bit 5-4	F2MSK<1:0	>: Mask Source	for Filter 2 bi	ts (same values	s as bits<15:14	<b>!</b> >)	
bit 3-2	F1MSK<1:0	>: Mask Source	for Filter 1 bi	ts (same values	s as bits<15:14	ł>)	
bit 1-0	F0MSK<1:0	Hask Source	for Filter 0 bi	ts (same values	s as bits<15:14	<b>!</b> >)	





#### 24.4 Step Commands and Format

#### TABLE 24-1: PTG STEP COMMAND FORMAT

Step Command Byte:	
STE	Px<7:0>
CMD<3:0>	OPTION<3:0>
bit 7 bit	4 bit 3 bit 0

bit 7-4	CMD<3:0>	Step Command	Command Description
	0000	PTGCTRL	Execute control command as described by OPTION<3:0>.
	0001	PTGADD	Add contents of PTGADJ register to target register as described by OPTION<3:0>.
		PTGCOPY	Copy contents of PTGHOLD register to target register as described by OPTION<3:0>.
	001x	PTGSTRB	Copy the value contained in CMD<0>:OPTION<3:0> to the CH0SA<4:0> bits (AD1CHS0<4:0>).
	0100	PTGWHI	Wait for a low-to-high edge input from the selected PTG trigger input as described by OPTION<3:0>.
	0101	PTGWLO	Wait for a high-to-low edge input from the selected PTG trigger input as described by OPTION<3:0>.
	0110	Reserved	Reserved.
	0111	PTGIRQ	Generate individual interrupt request as described by OPTION3<:0>.
	100x	PTGTRIG	Generate individual trigger output as described by < <cmd<0>:OPTION&lt;3:0&gt;&gt;.</cmd<0>
	101x	PTGJMP	Copy the value indicated in < <cmd<0>:OPTION&lt;3:0&gt;&gt; to the Queue Pointer (PTGQPTR) and jump to that Step queue.</cmd<0>
	110x	PTGJMPC0	PTGC0 = PTGC0LIM: Increment the Queue Pointer (PTGQPTR).
			$PTGC0 \neq PTGC0LIM$ : Increment Counter 0 (PTGC0) and copy the value indicated in < <cmd<0>:OPTION&lt;3:0&gt;&gt; to the Queue Pointer (PTGQPTR), and jump to that Step queue</cmd<0>
	111x	PTGJMPC1	PTGC1 = PTGC1LIM: Increment the Queue Pointer (PTGQPTR).
			$PTGC1 \neq PTGC1LIM$ : Increment Counter 1 (PTGC1) and copy the value indicated in < <cmd<0>:OPTION&lt;3:0&gt;&gt; to the Queue Pointer (PTGQPTR), and jump to that Step queue.</cmd<0>

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.



#### FIGURE 30-13: QEI MODULE INDEX PULSE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

# TABLE 30-32: QEI INDEX PULSE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min. Max. Units Conditions				
TQ50	TqiL	Filter Time to Recognize Low, with Digital Filter	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 <b>(Note 2)</b>	
TQ51	TqiH	Filter Time to Recognize High, with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 <b>(Note 2)</b>	
TQ55	Tqidxr	Index Pulse Recognized to Position Counter Reset (ungated index)	3 TCY	—	ns		

**Note 1:** These parameters are characterized but not tested in manufacturing.

2: Alignment of index pulses to QEA and QEB is shown for position counter Reset timing only. Shown for forward direction only (QEA leads QEB). Same timing applies for reverse direction (QEA lags QEB) but index pulse recognition occurs on the falling edge.

# TABLE 30-37:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)TIMING REQUIREMENTS

АС СНА	ARACTERIS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	-	—	Lesser of FP or 15	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)
SP60	TssL2doV	SDO2 Data Output Valid after SS2 Edge	-	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

# 44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	Ν		44		
Number of Pins per Side	ND		12		
Number of Pins per Side	NE		10		
Pitch	е		0.50 BSC		
Overall Height	А	0.80 0.90 1.00			
Standoff	A1	0.025	-	0.075	
Overall Width	Е		6.00 BSC		
Exposed Pad Width	E2	4.40	4.55	4.70	
Overall Length	D		6.00 BSC		
Exposed Pad Length	D2	4.40	4.55	4.70	
Contact Width	b	0.20	0.25	0.30	
Contact Length	L	0.20 0.25 0.30			
Contact-to-Exposed Pad	К	0.20	-	-	

#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

- 3. Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-157C Sheet 2 of 2

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



#### **RECOMMENDED LAND PATTERN**

	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B