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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

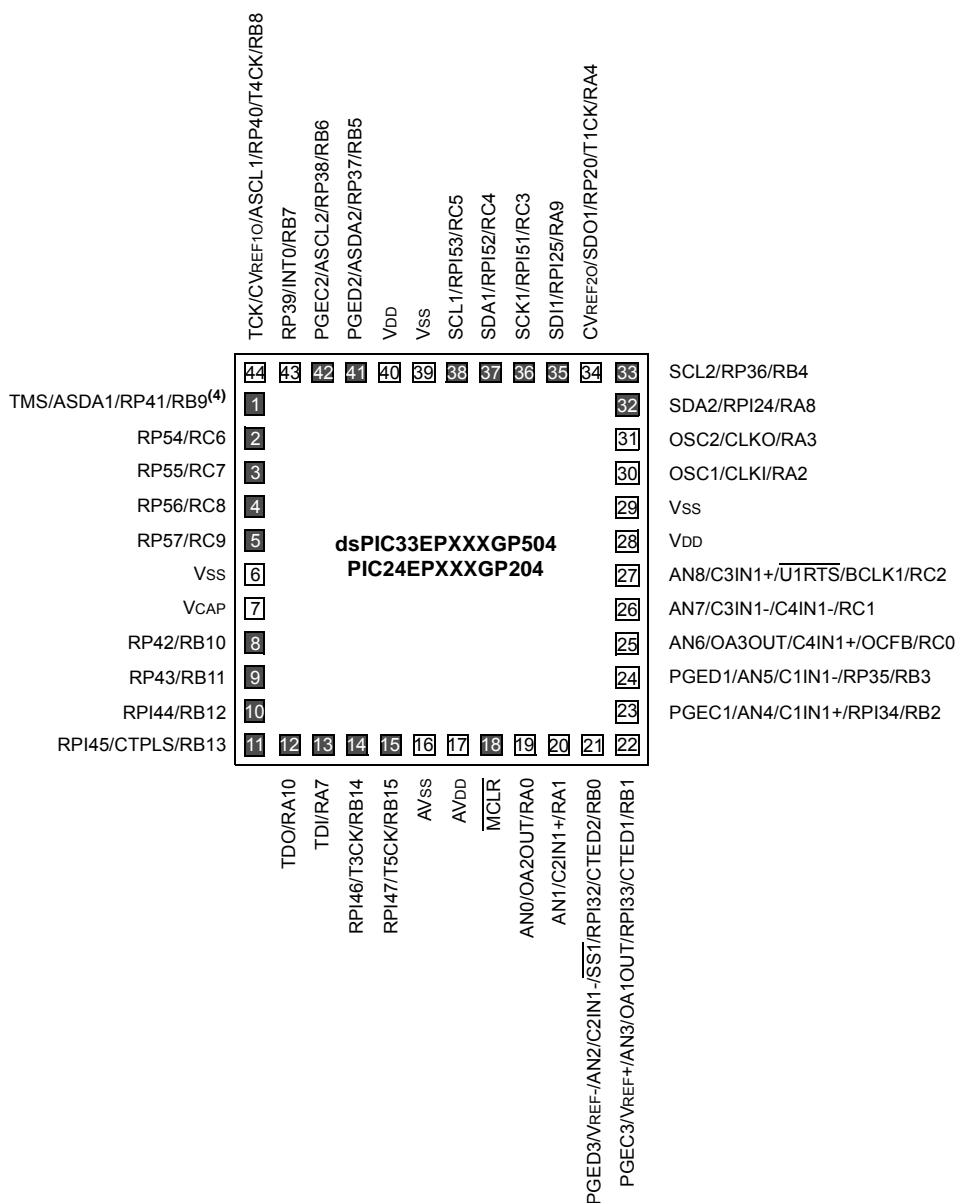
#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc203t-i-tl">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc203t-i-tl</a>

## Pin Diagrams (Continued)

44-Pin VTLA<sup>(1,2,3)</sup>

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
- Note 4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## 1.0 DEVICE OVERVIEW

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com))

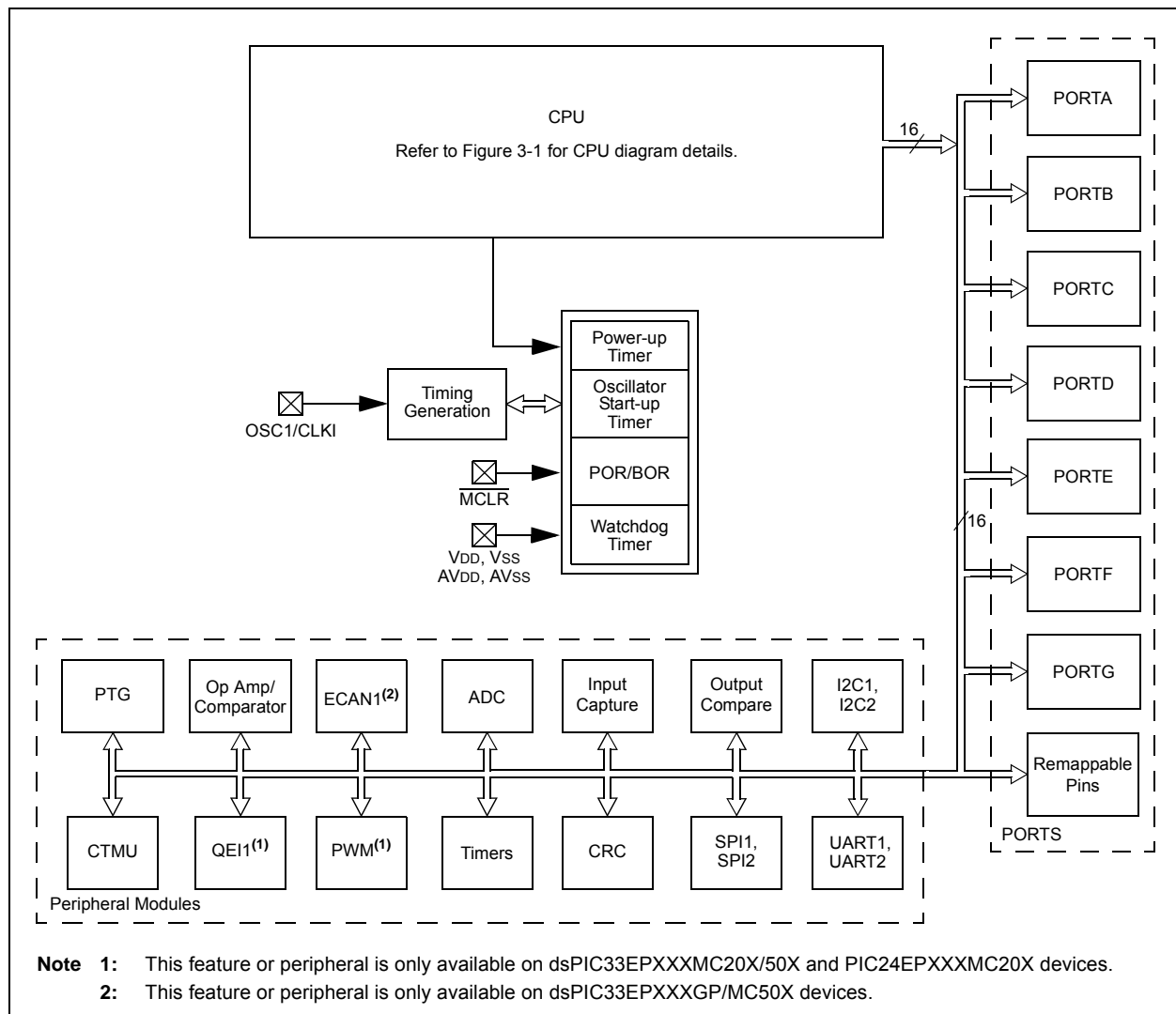
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

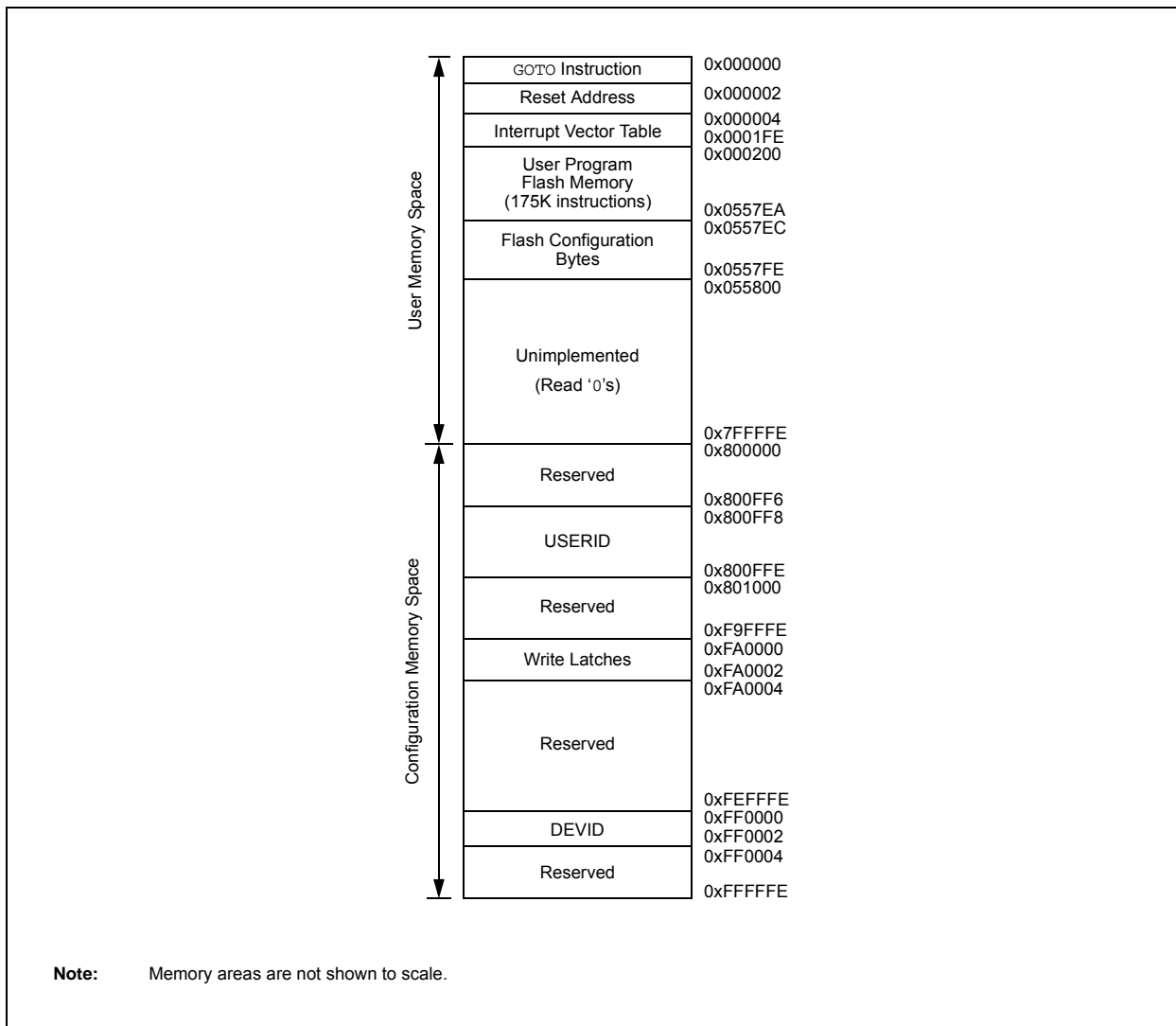
dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM**



**FIGURE 4-5: PROGRAM MEMORY MAP FOR dsPIC33EP512GP50X, dsPIC33EP512MC20X/50X AND PIC24EP512GP/MC20X DEVICES**



## 4.2 Data Address Space

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU has a separate 16-bit-wide data memory space. The Data Space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps, which are presented by device family and memory size, are shown in Figure 4-7 through Figure 4-16.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This arrangement gives a base Data Space address range of 64 Kbytes (32K words).

The base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space, which has a total address range of 16 Mbytes.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement up to 52 Kbytes of data memory (4 Kbytes of data memory for Special Function Registers and up to 48 Kbytes of data memory for RAM). If an EA points to a location outside of this area, an all-zero word or byte is returned.

### 4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte-addressable, 16-bit-wide blocks. Data is aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

### 4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® MCU devices and improve Data Space memory usage efficiency, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB. The MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

### 4.2.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X core and peripheral modules for controlling the operation of the device.

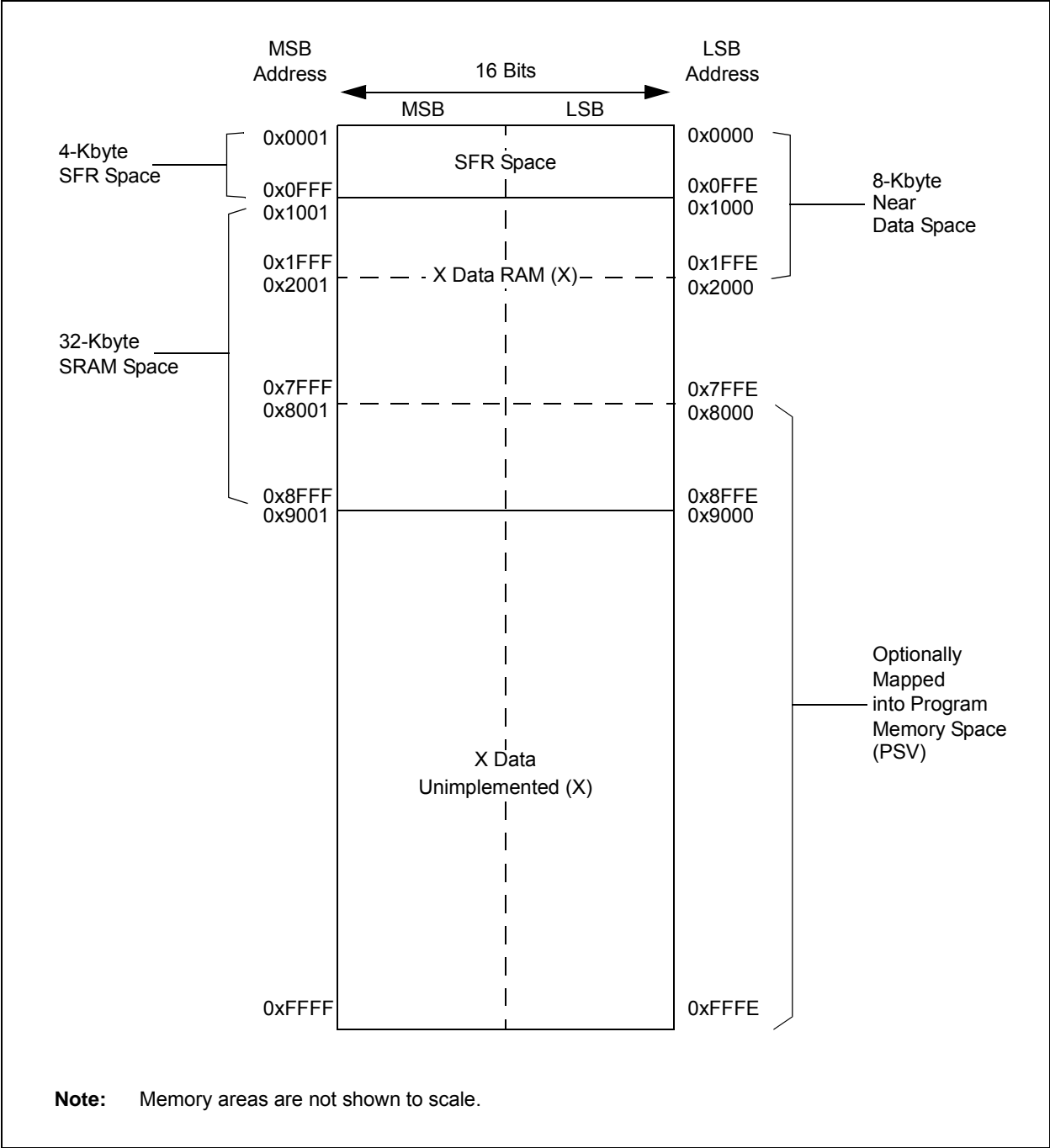
SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

**Note:** The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

### 4.2.4 NEAR DATA SPACE

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a working register as an Address Pointer.

FIGURE 4-15: DATA MEMORY MAP FOR PIC24EP256GP/MC20X/50X DEVICES



**TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000	
CORCON	0044	VAR	—	US<1:0>		EDT	DL<2:0>			SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF	0020	
MODCON	0046	XMODEN	YMODEN	—	—	BWM<3:0>				YWM<3:0>				XWM<3:0>				0000	
XMODSRT	0048	XMODSRT<15:0>																—	0000
XMODEND	004A	XMODEND<15:0>																—	0001
YMODSRT	004C	YMODSRT<15:0>																—	0000
YMODEND	004E	YMODEND<15:0>																—	0001
XBREV	0050	BREN	XBREV<14:0>																0000
DISCNT	0052	—	—	DISCNT<13:0>															0000
TBLPAG	0054	—	—	—	—	—	—	—	—	TBLPAG<7:0>									0000
MSTRPR	0058	MSTRPR<15:0>																0000	

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-12: PWM REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0C00	PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC<2:0>			SEVTPS<3:0>				0000
PTCON2	0C02	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
PTPER	0C04	PTPER<15:0>																00F8
SEVTCMP	0C06	SEVTCMP<15:0>																0000
MDC	0C0A	MDC<15:0>																0000
CHOP	0C1A	CHPCLKEN	—	—	—	—	—	CHOPCLK<9:0>										0000
PWMKEY	0C1E	PWMKEY<15:0>																0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-13: PWM GENERATOR 1 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTEN	CLLEN	TRGIEN	ITB	MDCS	DTC<1:0>		DTCP	—	MTBS	CAM	XPRES	IUE	0000	
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	C000	
FCLCON1	0C24	—	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>			0000
PDC1	0C26	PDC1<15:0>																	FFF8
PHASE1	0C28	PHASE1<15:0>																	0000
DTR1	0C2A	—	—	DTR1<13:0>															0000
ALTDTR1	0C2C	—	—	ALTDTR1<13:0>															0000
TRIG1	0C32	TRGCMPL<15:0>																	0000
TRGCON1	0C34	TRGDIV<3:0>				—	—	—	—	—	—	TRGSTRT<5:0>							0000
LEBCON1	0C3A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000	
LEBDLY1	0C3C	—	—	—	—	LEB<11:0>													0000
AUXCON1	0C3E	—	—	—	—	BLANKSEL<3:0>				—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000	

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



**TABLE 4-24: CRC REGISTER MAP**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON1	0640	CRCEN	—	CSIDL	VWORD<4:0>					CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—	0000
CRCCON2	0642	—	—	—	DWIDTH<4:0>					—	—	—	PLEN<4:0>					0000
CRCXORL	0644	X<15:1>															—	0000
CRCXORH	0646	X<31:16>															0000	
CRCDATL	0648	CRC Data Input Low Word															0000	
CRCDATH	064A	CRC Data Input High Word															0000	
CRCWDATL	064C	CRC Result Low Word															0000	
CRCWDATH	064E	CRC Result High Word															0000	

**Legend:** — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

**TABLE 4-25: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC202/502 AND PIC24EPXXXGP/MC202 DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-26: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC203/503 AND PIC24EPXXXGP/MC203 DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000
RPOR5	068A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
RPOR6	068C	—	—	—	—	—	—	—	—	—	—	RP56R<5:0>						0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 11-26: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP118R<5:0>					
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-14                      **Unimplemented:** Read as '0'

bit 13-8                      **RP118R<5:0>:** Peripheral Output Function is Assigned to RP118 Output Pin bits  
(see Table 11-3 for peripheral function numbers)

bit 7-0                      **Unimplemented:** Read as '0'

**REGISTER 11-27: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP120R<5:0>					
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-6                      **Unimplemented:** Read as '0'

bit 5-0                      **RP120R<5:0>:** Peripheral Output Function is Assigned to RP120 Output Pin bits  
(see Table 11-3 for peripheral function numbers)

## 14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	IC11	IC10	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7						bit 0	

<b>Legend:</b>	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Stop in Idle Control bit  
 1 = Input capture will Halt in CPU Idle mode  
 0 = Input capture will continue to operate in CPU Idle mode

bit 12-10 **ICTSEL<2:0>:** Input Capture Timer Select bits  
 111 = Peripheral clock (FP) is the clock source of the ICx  
 110 = Reserved  
 101 = Reserved  
 100 = T1CLK is the clock source of the ICx (only the synchronous clock is supported)  
 011 = T5CLK is the clock source of the ICx  
 010 = T4CLK is the clock source of the ICx  
 001 = T2CLK is the clock source of the ICx  
 000 = T3CLK is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **IC1<1:0>:** Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)  
 11 = Interrupt on every fourth capture event  
 10 = Interrupt on every third capture event  
 01 = Interrupt on every second capture event  
 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)  
 1 = Input capture buffer overflow occurred  
 0 = No input capture buffer overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)  
 1 = Input capture buffer is not empty, at least one more capture value can be read  
 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits  
 111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)  
 110 = Unused (module is disabled)  
 101 = Capture mode, every 16th rising edge (Prescaler Capture mode)  
 100 = Capture mode, every 4th rising edge (Prescaler Capture mode)  
 011 = Capture mode, every rising edge (Simple Capture mode)  
 010 = Capture mode, every falling edge (Simple Capture mode)  
 001 = Capture mode, every edge rising and falling (Edge Detect mode (IC1<1:0>) is not used in this mode)  
 000 = Input capture module is turned off

**REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)**

bit 4-2      **SPRE<2:0>**: Secondary Prescale bits (Master mode)<sup>(3)</sup>

111 = Secondary prescale 1:1

110 = Secondary prescale 2:1

•

•

•

000 = Secondary prescale 8:1

bit 1-0      **PPRE<1:0>**: Primary Prescale bits (Master mode)<sup>(3)</sup>

11 = Primary prescale 1:1

10 = Primary prescale 4:1

01 = Primary prescale 16:1

00 = Primary prescale 64:1

- Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
- 2:** This bit must be cleared when FRMEN = 1.
- 3:** Do not set both primary and secondary prescalers to the value of 1:1.

## 19.0 INTER-INTEGRATED CIRCUIT™ (I<sup>2</sup>C™)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Inter-Integrated Circuit™ (I<sup>2</sup>C™)**” (DS70330) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

- 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.
- 3: There are minimum bit rates of approximately  $F_{CY}/512$ . As a result, high processor speeds may not support 100 Kbit/second operation. See timing specifications, IM10 and IM11, and the “**Baud Rate Generator**” in the “*dsPIC33/PIC24 Family Reference Manual*”.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices contains two Inter-Integrated Circuit (I<sup>2</sup>C) modules: I2C1 and I2C2.

The I<sup>2</sup>C module provides complete hardware support for both Slave and Multi-Master modes of the I<sup>2</sup>C serial communication standard, with a 16-bit interface.

The I<sup>2</sup>C module has a 2-pin interface:

- The SCLx pin is clock
- The SDAx pin is data

The I<sup>2</sup>C module offers the following key features:

- I<sup>2</sup>C interface supporting both Master and Slave modes of operation
- I<sup>2</sup>C Slave mode supports 7 and 10-bit addressing
- I<sup>2</sup>C Master mode supports 7 and 10-bit addressing
- I<sup>2</sup>C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I<sup>2</sup>C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I<sup>2</sup>C supports multi-master operation, detects bus collision and arbitrates accordingly
- Intelligent Platform Management Interface (IPMI) support
- System Management Bus (SMBus) support

## 20.3 UARTx Control Registers

**REGISTER 20-1: UxMODE: UARTx MODE REGISTER**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN <sup>(1)</sup>	—	USIDL	IREN <sup>(2)</sup>	RTSMD	—	UEN1	UEN0
bit 15						bit 8	

R/W-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7						bit 0	

<b>Legend:</b>	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15      **UARTEN:** UARTx Enable bit<sup>(1)</sup>  
1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>  
0 = UARTx is disabled; all UARTx pins are controlled by PORT latches; UARTx power consumption is minimal
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **USIDL:** UARTx Stop in Idle Mode bit  
1 = Discontinues module operation when device enters Idle mode  
0 = Continues module operation in Idle mode
- bit 12      **IREN:** IrDA<sup>®</sup> Encoder and Decoder Enable bit<sup>(2)</sup>  
1 = IrDA encoder and decoder are enabled  
0 = IrDA encoder and decoder are disabled
- bit 11      **RTSMD:** Mode Selection for  $\overline{\text{UxRTS}}$  Pin bit  
1 =  $\overline{\text{UxRTS}}$  pin is in Simplex mode  
0 =  $\overline{\text{UxRTS}}$  pin is in Flow Control mode
- bit 10      **Unimplemented:** Read as '0'
- bit 9-8      **UEN<1:0>:** UARTx Pin Enable bits  
11 = UxTX, UxRX and BCLKx pins are enabled and used;  $\overline{\text{UxCTS}}$  pin is controlled by PORT latches<sup>(3)</sup>  
10 = UxTX, UxRX,  $\overline{\text{UxCTS}}$  and  $\overline{\text{UxRTS}}$  pins are enabled and used<sup>(4)</sup>  
01 = UxTX, UxRX and  $\overline{\text{UxRTS}}$  pins are enabled and used;  $\overline{\text{UxCTS}}$  pin is controlled by PORT latches<sup>(4)</sup>  
00 = UxTX and UxRX pins are enabled and used;  $\overline{\text{UxCTS}}$  and  $\overline{\text{UxRTS}}$ /BCLKx pins are controlled by PORT latches
- bit 7      **WAKE:** Wake-up on Start bit Detect During Sleep Mode Enable bit  
1 = UARTx continues to sample the UxRX pin; interrupt is generated on the falling edge; bit is cleared in hardware on the following rising edge  
0 = No wake-up is enabled
- bit 6      **LPBACK:** UARTx Loopback Mode Select bit  
1 = Enables Loopback mode  
0 = Loopback mode is disabled

- Note 1:** Refer to the “UART” (DS70582) section in the “dsPIC33/PIC24 Family Reference Manual” for information on enabling the UARTx module for receive or transmit operation.
- 2:** This feature is only available for the 16x BRG mode (BRGH = 0).
- 3:** This feature is only available on 44-pin and 64-pin devices.
- 4:** This feature is only available on 64-pin devices.

**REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-0                      **EID<15:0>**: Extended Identifier bits  
1 = Message address bit, EIDx, must be '1' to match filter  
0 = Message address bit, EIDx, must be '0' to match filter

**REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER 1**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MSK<1:0>		F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>	
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-14                      **F7MSK<1:0>**: Mask Source for Filter 7 bits  
11 = Reserved  
10 = Acceptance Mask 2 registers contain mask  
01 = Acceptance Mask 1 registers contain mask  
00 = Acceptance Mask 0 registers contain mask

bit 13-12                      **F6MSK<1:0>**: Mask Source for Filter 6 bits (same values as bits<15:14>)

bit 11-10                      **F5MSK<1:0>**: Mask Source for Filter 5 bits (same values as bits<15:14>)

bit 9-8                      **F4MSK<1:0>**: Mask Source for Filter 4 bits (same values as bits<15:14>)

bit 7-6                      **F3MSK<1:0>**: Mask Source for Filter 3 bits (same values as bits<15:14>)

bit 5-4                      **F2MSK<1:0>**: Mask Source for Filter 2 bits (same values as bits<15:14>)

bit 3-2                      **F1MSK<1:0>**: Mask Source for Filter 1 bits (same values as bits<15:14>)

bit 1-0                      **F0MSK<1:0>**: Mask Source for Filter 0 bits (same values as bits<15:14>)

## 23.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Analog-to-Digital Converter (ADC)**” (DS70621) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices have one ADC module. The ADC module supports up to 16 analog input channels.

On ADC1, the AD12B bit (AD1CON1<10>) allows the ADC module to be configured by the user as either a 10-bit, 4 Sample-and-Hold (S&H) ADC (default configuration) or a 12-bit, 1 S&H ADC.

**Note:** The ADC module needs to be disabled before modifying the AD12B bit.

## 23.1 Key Features

### 23.1.1 10-BIT ADC CONFIGURATION

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) conversion
- Conversion speeds of up to 1.1 Msps
- Up to 16 analog input pins
- Connections to three internal op amps
- Connections to the Charge Time Measurement Unit (CTMU) and temperature measurement diode
- Channel selection and triggering can be controlled by the Peripheral Trigger Generator (PTG)
- External voltage reference input pins
- Simultaneous sampling of:
  - Up to four analog input pins
  - Three op amp outputs
  - Combinations of analog inputs and op amp outputs
- Automatic Channel Scan mode
- Selectable conversion Trigger source
- Selectable Buffer Fill modes
- Four result alignment options (signed/unsigned, fractional/integer)
- Operation during CPU Sleep and Idle modes

### 23.1.2 12-BIT ADC CONFIGURATION

The 12-bit ADC configuration supports all the features listed above, with the exception of the following:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only one S&H amplifier in the 12-bit configuration; therefore, simultaneous sampling of multiple channels is not supported.

Depending on the particular device pinout, the ADC can have up to 16 analog input pins, designated AN0 through AN15. These analog inputs are shared with op amp inputs and outputs, comparator inputs, and external voltage references. When op amp/comparator functionality is enabled, or an external voltage reference is used, the analog input that shares that pin is no longer available. The actual number of analog input pins, op amps and external voltage reference input configuration depends on the specific device.

A block diagram of the ADC module is shown in Figure 23-1. Figure 23-2 provides a diagram of the ADC conversion clock period.



TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DI10 DI18 DI19	V <sub>IL</sub>	<b>Input Low Voltage</b>					
		Any I/O Pin and $\overline{\text{MCLR}}$	V <sub>SS</sub>	—	0.2 V <sub>DD</sub>	V	
		I/O Pins with SDAx, SCLx	V <sub>SS</sub>	—	0.3 V <sub>DD</sub>	V	SMBus disabled
		I/O Pins with SDAx, SCLx	V <sub>SS</sub>	—	0.8	V	SMBus enabled
DI20	V <sub>IH</sub>	<b>Input High Voltage</b>					
		I/O Pins Not 5V Tolerant	0.8 V <sub>DD</sub>	—	V <sub>DD</sub>	V	(Note 3)
		I/O Pins 5V Tolerant and $\overline{\text{MCLR}}$	0.8 V <sub>DD</sub>	—	5.5	V	(Note 3)
		I/O Pins with SDAx, SCLx	0.8 V <sub>DD</sub>	—	5.5	V	SMBus disabled
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled
DI30	ICNPU	<b>Change Notification Pull-up Current</b>	150	250	550	μA	V <sub>DD</sub> = 3.3V, V <sub>PIN</sub> = V <sub>SS</sub>
DI31	ICNPD	<b>Change Notification Pull-Down Current<sup>(4)</sup></b>	20	50	100	μA	V <sub>DD</sub> = 3.3V, V <sub>PIN</sub> = V <sub>DD</sub>

**Note 1:** The leakage current on the  $\overline{\text{MCLR}}$  pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

**2:** Negative current is defined as current sourced by the pin.

**3:** See the “Pin Diagrams” section for the 5V tolerant I/O pins.

**4:** V<sub>IL</sub> source < (V<sub>SS</sub> – 0.3). Characterized but not tested.

**5:** Non-5V tolerant pins V<sub>IH</sub> source > (V<sub>DD</sub> + 0.3), 5V tolerant pins V<sub>IH</sub> source > 5.5V. Characterized but not tested.

**6:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.

**7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

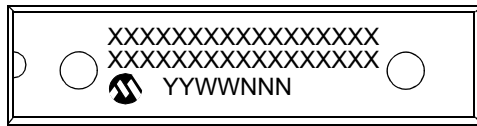
**8:** Any number and/or combination of I/O pins not excluded under I<sub>ICL</sub> or I<sub>ICH</sub> conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

**NOTES:**

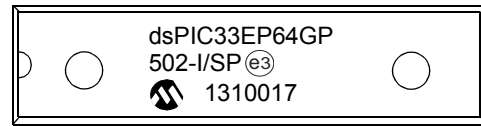
## 33.0 PACKAGING INFORMATION

### 33.1 Package Marking Information

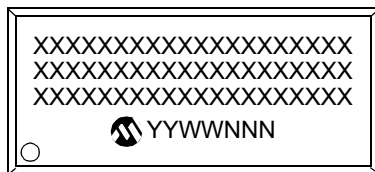
28-Lead SPDIP



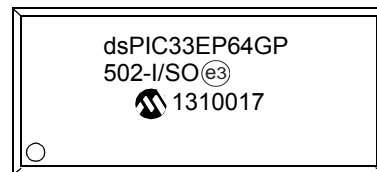
Example



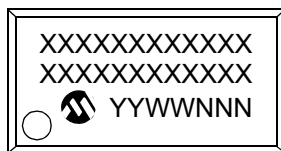
28-Lead SOIC (.300")



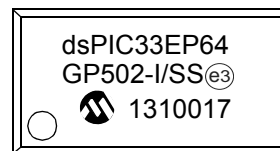
Example



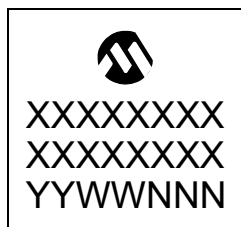
28-Lead SSOP



Example



28-Lead QFN-S (6x6x0.9 mm)



Example



<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.



TABLE A-5: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
<b>Section 30.0 “Electrical Characteristics”</b>	<ul style="list-style-type: none"> <li>• Throughout: qualifies all footnotes relating to the operation of analog modules below VDDMIN (replaces “will have” with “may have”)</li> <li>• Throughout: changes all references of SPI timing parameter symbol “TscP” to “FscP”</li> <li>• Table 30-1: changes VDD range to 3.0V to 3.6V</li> <li>• Table 30-4: removes Parameter DC12 (RAM Retention Voltage)</li> <li>• Table 30-7: updates Maximum values at 10 and 20 MIPS</li> <li>• Table 30-8: adds Maximum IPD values, and removes all <math>\Delta I_{WDT}</math> entries</li> <li>• Adds new Table 30-9 (Watchdog Timer Delta Current) with consolidated values removed from Table 30-8. All subsequent tables are renumbered accordingly.</li> <li>• Table 30-10: adds footnote for all parameters for 1:2 Doze ratio</li> <li>• Table 30-11: <ul style="list-style-type: none"> <li>- changes Minimum and Maximum values for D120 and D130</li> <li>- adds Minimum and Maximum values for D131</li> <li>- adds Minimum and Maximum values for D150 through D156, and removes Typical values</li> </ul> </li> <li>• Table 30-12: <ul style="list-style-type: none"> <li>- reformats table for readability</li> <li>- changes IOL conditions for DO10</li> </ul> </li> <li>• Table 30-14: adds footnote to D135</li> <li>• Table 30-17: changes Minimum and Maximum values for OS30</li> <li>• Table 30-19: <ul style="list-style-type: none"> <li>- splits temperature range and adds new values for F20a</li> <li>- reduces temperature range for F20b to extended temperatures only</li> </ul> </li> <li>• Table 30-20: <ul style="list-style-type: none"> <li>- splits temperature range and adds new values for F21a</li> <li>- reduces temperature range for F20b to extended temperatures only</li> </ul> </li> <li>• Table 30-53: <ul style="list-style-type: none"> <li>- adds Maximum value to CM30</li> <li>- adds footnote (“Parameter characterized...”) to multiple parameters</li> </ul> </li> <li>• Table 30-55: adds Minimum and Maximum values for all CTMUI specifications, and removes Typical values</li> <li>• Table 30-57: adds new footnote to AD09</li> <li>• Table 30-58: <ul style="list-style-type: none"> <li>- removes all specifications for accuracy with external voltage references</li> <li>- removes Typical values for AD23a and AD24a</li> <li>- replaces Minimum and Maximum values for AD21a, AD22a, AD23a and AD24a with new values, split by Industrial and Extended temperatures</li> <li>- removes Maximum value of AD30</li> <li>- removes Minimum values from AD31a and AD32a</li> <li>- adds or changes Typical values for AD30, AD31a, AD32a and AD33a</li> </ul> </li> <li>• Table 30-59: <ul style="list-style-type: none"> <li>- removes all specifications for accuracy with external voltage references</li> <li>- removes Maximum value of AD30</li> <li>- removes Typical values for AD23b and AD24b</li> <li>- replaces Minimum and Maximum values for AD21b, AD22b, AD23b and AD24b with new values, split by Industrial and Extended temperatures</li> <li>- removes Minimum and Maximum values from AD31b, AD32b, AD33b and AD34b</li> <li>- adds or changes Typical values for AD30, AD31a, AD32a and AD33a</li> </ul> </li> <li>• Table 30-61: Adds footnote to AD51</li> </ul>
<b>Section 32.0 “DC and AC Device Characteristics Graphs”</b>	<ul style="list-style-type: none"> <li>• Updates Figure 32-6 (Typical IDD @ 3.3V) with individual current vs. processor speed curves for the different program memory sizes</li> </ul>
<b>Section 33.0 “Packaging Information”</b>	<ul style="list-style-type: none"> <li>• Replaces drawing C04-149C (64-pin QFN, 7.15 x 7.15 exposed pad) with C04-154A (64-pin QFN, 5.4 x 5.4 exposed pad)</li> </ul>