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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc204-e-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES

		<u>~</u>				Re	mappa	ble P	eriphe	erals											
Device	Page Erase Size (Instructions)	Program Flash Memory (Kbyte	RAM (Kbytes)	16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM ⁽⁴⁾ (Channels)	Quadrature Encoder Interface	UART	SPI ⁽²⁾	ECAN™ Technology	External Interrupts ⁽³⁾	I²C™	CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	СТМИ	PTG	l/O Pins	Pins	Packages
PIC24EP32MC202	512	32	4																		
PIC24EP64MC202	1024	64	8																		SPDIP,
PIC24EP128MC202	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SOIC,
PIC24EP256MC202	1024	256	32																		QFN-S
PIC24EP512MC202	1024	512	48																		
PIC24EP32MC203	512	32	4	-			_	4	0	0		0	0	4	•	2/4	V	Vee	05	20	
PIC24EP64MC203	1024	64	8	5	4	4	ю	1	2	2	_	3	2	1	8	3/4	res	res	25	30	VILA
PIC24EP32MC204	512	32	4																		
PIC24EP64MC204	1024	64	8																		VTLA ⁽⁵⁾ ,
PIC24EP128MC204	1024	128	16	5	4	4	6	1	2	2	-	3	2	1	9	3/4	Yes	Yes	35	44/ 48	TQFP,
PIC24EP256MC204	1024	256	32																		UQFN
PIC24EP512MC204	1024	512	48																		
PIC24EP64MC206	1024	64	8																		
PIC24EP128MC206	1024	128	16	_					-			•									TQFP.
PIC24EP256MC206	1024	256	32	5	4	4	6	1	2	2	_	3	2	1	16	3/4	res	res	53	64	QFN
PIC24EP512MC206	1024	512	48																		
dsPIC33EP32MC202	512	32	4																		
dsPIC33EP64MC202	1024	64	8																		SPDIP,
dsPIC33EP128MC202	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	6	2/3(1)	Yes	Yes	21	28	SOIC,
dsPIC33EP256MC202	1024	256	32																		QFN-S
dsPIC33EP512MC202	1024	512	48																		
dsPIC33EP32MC203	512	32	4	_		_			-	_											
dsPIC33EP64MC203	1024	64	8	5	4	4	6	1	2	2	—	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
dsPIC33EP32MC204	512	32	4																		
dsPIC33EP64MC204	1024	64	8																		VTLA ⁽⁵⁾ ,
dsPIC33EP128MC204	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	9	3/4	Yes	Yes	35	44/	TQFP,
dsPIC33EP256MC204	1024	256	32																	40	UQFN,
dsPIC33EP512MC204	1024	512	48																		
dsPIC33EP64MC206	1024	64	8																		
dsPIC33EP128MC206	1024	128	16	_					-			-	-								TOFP
dsPIC33EP256MC206	1024	256	32	5	4	4	6	1	2	2	—	3	2	1	16	3/4	Yes	Yes	53	64	QFN
dsPIC33EP512MC206	1024	512	48																		
dsPIC33EP32MC502	512	32	4																		
dsPIC33EP64MC502	1024	64	8																		SPDIP,
dsPIC33EP128MC502	1024	128	16	5	4	4	6	1	2	2	1	3	2	1	6	2/3(1)	Yes	Yes	21	28	SFDIF, SOIC, SSOP ⁽⁵⁾ , QFN-S
dsPIC33EP256MC502	1024	256	32												0						
dsPIC33EP512MC502	1024	512	48																		_
dsPIC33EP32MC503	512	32	4	_			6		_	-			-		_	.		~	a-		
dsPIC33EP64MC503	1024	64	8	5	4	4	6	1	2	2	1	3	2	1	8	3/4	res	res	25	36	VILA

Note 1: On 28-pin devices, Comparator 4 does not have external connections. Refer to Section 25.0 "Op Amp/Comparator Module" for details. 2: Only SPI2 is remappable.

3: INTO is not remappable.

4: Only the PWM Faults are remappable.

5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

3.5 **Programmer's Model**

The programmer's model for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X is shown in Figure 3-2. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/

MC20X devices contain control registers for Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only), Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only) and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory mapped, as shown in Table 4-1.

Register(s) Name	Description
W0 through W15	Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
DSWPAG	Extended Data Space (EDS) Write Page Register
RCOUNT	REPEAT Loop Count Register
DCOUNT ⁽¹⁾	DO Loop Count Register
DOSTARTH ^(1,2) , DOSTARTL ^(1,2)	DO Loop Start Address Register (High and Low)
DOENDH ⁽¹⁾ , DOENDL ⁽¹⁾	DO Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Note 1: This register is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

2: The DOSTARTH and DOSTARTL registers are read-only.

9.0 OSCILLATOR CONFIGURATION

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Oscillator" (DS70580) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X oscillator system provides:

- On-chip Phase-Locked Loop (PLL) to boost internal operating frequency on select internal and external oscillator sources
- On-the-fly clock switching between various clock sources
- · Doze mode for system power savings
- Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Configuration bits for clock source selection
- A simplified diagram of the oscillator system is shown in Figure 9-1.

FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM



2: The term, FP, refers to the clock source for all peripherals, while FCY refers to the clock source for the CPU. Throughout this document, FCY and FP are used interchangeably, except in the case of Doze mode. FP and FCY will be different when Doze mode is used with a doze ratio of 1:2 or lower.

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	xx	101	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	0.0	011	1
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

9.2 Oscillator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

9.2.1 KEY RESOURCES

- "Oscillator" (DS70580) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- · Development Tools

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
ROON		ROSSLP	ROSEL	RODIV3 ⁽¹⁾	RODIV2 ⁽¹⁾	RODIV1 ⁽¹⁾	RODIV0 ⁽¹⁾						
bit 15				•		•	bit 8						
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0						
		<u> </u>				<u> </u>							
bit 7							bit 0						
Legend:													
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'							
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown						
bit 15	ROON: Refer	ence Oscillato	Output Enab	ole bit									
Sit 10	1 = Reference oscillator output is enabled on the REFCLK pin ⁽²⁾ 0 = Reference oscillator output is disabled												
bit 14	Unimplemen	Unimplemented: Read as '0'											
bit 13	ROSSLP: Reference Oscillator Run in Sleep bit												
	1 = Reference	e oscillator outp	out continues	to run in Sleep									
	0 = Reference	e oscillator outp	out is disabled	l in Sleep									
bit 12	ROSEL: Refe	erence Oscillato	or Source Sel	ect bit									
	1 = Oscillator	crystal is used	as the refere	nce clock									
hit 11_8		Peference Os	cillator Divide	r hite(1)									
Dit 11-0	1111 = Refer	ence clock divi	ded by 32 76	R									
	1110 = Refer	ence clock divi	ded by 16,384	4									
	1101 = Refer	ence clock divi	ded by 8,192										
	1100 = Refer	ence clock divi	ded by 4,096										
	1011 = Refer	ence clock divi	ded by 2,048										
	1010 = Relef	ence clock divi	ded by 1,024 ded by 512										
	1000 = Refer	ence clock divi	ded by 256										
	0111 = Refer	ence clock divi	ded by 128										
	0110 = Refer	ence clock divi	ded by 64										
	0101 = Refer	ence clock divi	ded by 32										
	ULUU = Reference clock divided by 16												
	0011 = Refer	ence clock divi	ded by 6 ded by 4										
	0001 = Refer	ence clock divi	ded by 2										
	0000 = Refer	ence clock	-										
bit 7-0	Unimplemen	ted: Read as '	כ'										

REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

- **Note 1:** The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
 - 2: This pin is remappable. See Section 11.4 "Peripheral Pin Select (PPS)" for more information.

11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, "RPn" or "RPIn", in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs. In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C^{TM} and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and nonremappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheralselectable pin is handled in two different ways, depending on whether an input or output is being mapped.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 16-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	id as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			

bit 15-0 **PDCx<15:0>:** PWMx Generator # Duty Cycle Value bits

REGISTER 16-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	Ex<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	SEx<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable b	it	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at P	OR	'1' = Bit is set	t '0' = Bit is cleared x = Bit is unknow			nown	

bit 15-0 PHASEx<15:0>: PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs

 If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL NOTES:

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	EC<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	EC<23:16>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is		x = Bit is unkr	iown

REGISTER 17-15: QEI1GECH: QEI1 GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER

bit 15-0 QEIGEC<31:16>: High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

REGISTER 17-16: QEI1GECL: QEI1 GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			QEIGE	C<15:8>				
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			QEIG	EC<7:0>				
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit l			U = Unimplemented bit, read as '0'					
-n = Value at F	ue at POR '1' = Bit is set '0' = Bit is cleared x = Bit		x = Bit is unkr	nown				

bit 15-0 QEIGEC<15:0>: Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

21.4 ECAN Control Registers

REGISTER 21-1:	CxCTRL1: ECANx CONTROL REGISTER 1
----------------	-----------------------------------

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0				
		CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0				
bit 15				·			bit 8				
R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0				
OPMODE2	OPMODE1	OPMODE0		CANCAP	—	—	WIN				
bit 7							bit 0				
[
Legena:	hit	M = M/ritabla I		II – Unimplor	nonted bit read						
		'1' = Bit is set	JIL	$0^{\circ} = \text{Bit is closed}$	ared	v = Bitis unkr					
	UK	I - DILIS SEL			aleu		IOWIT				
bit 15-14 Unimplemented: Read as '0'											
bit 13	CSIDL: ECAN	Nx Stop in Idle I	Mode bit								
	1 = Discontin	ues module ope	eration when	device enters I	dle mode						
	0 = Continues	s module opera	tion in Idle m	ode							
bit 12	ABAT: Abort	All Pending Tra	nsmissions b	it							
	1 = Signals al	I transmit buffe	rs to abort tra when all tran	ansmission smissions are a	aborted						
bit 11		CANCKS: ECANY Module Clock (ECAN) Source Select bit									
2	1 = FCAN is e	qual to 2 * FP									
	0 = FCAN is e	qual to FP									
bit 10-8	REQOP<2:0>	Request Ope	ration Mode	bits							
	111 = Set Lis	ten All Messag	es mode								
	101 = Reserv	red									
	100 = Set Co	nfiguration mod	le								
	011 = Set Lis	ten Only mode									
	001 = Set Dis	able mode									
	000 = Set No	rmal Operation	mode								
bit 7-5	OPMODE<2:	0> : Operation N	/lode bits								
	111 = Module	e is in Listen All	Messages m	node							
	110 = Reserv 101 = Reserv	red red									
	100 = Module	e is in Configura	ation mode								
	011 = Module	e is in Listen Or	ly mode								
	010 = Module	e is in Loopback e is in Disable n	node								
	000 = Module	e is in Normal C	peration mod	de							
bit 4	Unimplemen	ted: Read as 'o)'								
bit 3	CANCAP: CA	N Message Re	eceive Timer	Capture Event	Enable bit						
	1 = Enables in 0 = Disables (nput capture ba CAN capture	ised on CAN	message recei	ve						
bit 2-1	Unimplemen	ted: Read as '()'								
bit 0	WIN: SFR Ma	ap Window Sele	ect bit								
	1 = Uses filter	r window									
	0 = Uses buff	er window									

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
	WAKFIL		—		SEG2PH2	SEG2PH1	SEG2PH0
bit 15						1	bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEG2PHTS	SAM	SEG1PH2	SEG1PH1	SEG1PH0	PRSEG2	PRSEG0	
bit 7							bit 0
Legend:							
R = Readable b	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown
bit 15	Unimplemen	ted: Read as ')'				
bit 14	WAKFIL: Sele	ect CAN Bus Li	ne Filter for V	Vake-up bit			
	1 = Uses CAP 0 = CAN bus	N DUS line filter	tor wake-up				
hit 13-11	Unimplemen	ted: Read as '	n'	, ab			
bit 10-8	SFG2PH<2:0	>: Phase Segn	nent 2 bits				
	111 = Lenath	is 8 x TQ					
	•						
	•						
	•						
	000 = Length	is 1 x Tq					
bit 7	SEG2PHTS:	Phase Segmer	nt 2 Time Sele	ct bit			
	1 = Freely pro 0 = Maximum	ogrammable of SEG1PHx b	oits or Informa	tion Processin	g Time (IPT), w	/hichever is gre	eater
bit 6	SAM: Sample	of the CAN Bu	us Line bit			-	
	1 = Bus line is 0 = Bus line is	s sampled three s sampled once	e times at the at the sample	sample point e point			
bit 5-3	SEG1PH<2:0	>: Phase Segr	nent 1 bits	I			
	111 = Length	is 8 x Tq					
	•						
	•						
	•						
	000 = Length	is 1 x Tq					
bit 2-0	PRSEG<2:0>	: Propagation	Time Segmen	t bits			
	111 = Length	is 8 x Tq					
	•						
	•						
	-	is 1 x To					

REGISTER 21-10: CxCFG2: ECANx BAUD RATE CONFIGURATION REGISTER 2

NOTES:

REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1 (CONTINUED)

bit 7-5	SSRC<2:0>: Sample Trigger Source Select bits
	If SSRCG = 1: 111 = Reserved 110 = PTGO15 primary trigger compare ends sampling and starts conversion ⁽¹⁾ 101 = PTGO14 primary trigger compare ends sampling and starts conversion ⁽¹⁾ 100 = PTGO13 primary trigger compare ends sampling and starts conversion ⁽¹⁾ 011 = PTGO12 primary trigger compare ends sampling and starts conversion ⁽¹⁾ 010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion ⁽²⁾ 001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion ⁽²⁾ 000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion ⁽²⁾
	If SSRCG = 0: 111 = Internal counter ends sampling and starts conversion (auto-convert) 110 = CTMU ends sampling and starts conversion 101 = Reserved
	 101 - Reserved 100 = Timer5 compare ends sampling and starts conversion 011 = PWM primary Special Event Trigger ends sampling and starts conversion 010 = Timer3 compare ends sampling and starts conversion 001 = Active transition on the INT0 pin ends sampling and starts conversion 000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)
bit 4	SSRCG: Sample Trigger Source Group bit
	See SSRC<2:0> for details.
bit 3	SIMSAM: Simultaneous Sample Select bit (only applicable when CHPS<1:0> = 01 or 1x) In 12-bit mode (AD21B = 1), SIMSAM is Unimplemented and is Read as '0': 1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS<1:0> = 1x); or samples CH0 and CH1 simultaneously (when CHPS<1:0> = 01) 0 = Samples multiple channels individually in sequence
bit 2	ASAM: ADC1 Sample Auto-Start bit
	 1 = Sampling begins immediately after the last conversion; SAMP bit is auto-set 0 = Sampling begins when the SAMP bit is set
bit 1	SAMP: ADC1 Sample Enable bit
	 1 = ADC Sample-and-Hold amplifiers are sampling 0 = ADC Sample-and-Hold amplifiers are holding If ASAM = 0, software can write '1' to begin sampling. Automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write '0' to end sampling and start conversion. If SSRC<2:0> ≠ 000, automatically cleared by hardware to end sampling and start conversion.
bit 0	DONE: ADC1 Conversion Status bit ⁽³⁾
	 1 = ADC conversion cycle has completed 0 = ADC conversion has not started or is in progress Automatically set by hardware when the ADC conversion is complete. Software can write '0' to clear the DONE status bit (software is not allowed to write '1'). Clearing this bit does NOT affect any operation in progress. Automatically cleared by hardware at the start of a new conversion.
Note 1:	See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

- 2: This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- **3:** Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	_				—				
bit 15							bit 8		
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0		
bit 7									
Lorendi									
R = Reada	able hit	W = Writable	hit	= Inimpler	mented hit read	ae 'O'			
-n = Value	at POR	'1' = Rit is set	bit	'0' = Bit is cle	ared	x = Rit is unkr	nown		
II Value		1 Dit lo oot					lowin		
bit 15-7	Unimplemen	nted: Read as '	0'						
bit 6-4	CFSEL<2:0>	: Comparator I	-ilter Input Clo	ck Select bits					
	111 = T5CLK	(1)							
	110 = T4CLK	(2) (1)							
	101 = T3CLK	(1) (2)							
	100 = 12CLP	ved							
	010 = SYNC	01 ⁽³⁾							
	001 = Fosc ⁽⁴	4)							
	000 = FP ⁽⁴⁾								
bit 3	CFLTREN: C	comparator Filte	er Enable bit						
	1 = Digital filt	er is enabled							
hit 2-0		Comparator F	ilter Clock Div	ide Select hits					
511 2-0	111 = Clock	Divide 1.128							
	110 = Clock	Divide 1:64							
	101 = Clock Divide 1:32								
	100 = Clock Divide 1:16								
	011 = Clock Divide 1:8 010 = Clock Divide 1:4								
	0.10 = Clock Divide 1.4 0.01 = Clock Divide 1.2								
	000 = Clock	Divide 1:1							
Note 1:	See the Type C Ti	mer Block Diac	ram (Figure 1	3-2).					
2:	: See the Type B Timer Block Diagram (Figure 13-1).								

REGISTER 25-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER

- 3: See the High-Speed PWMx Module Register Interconnection Diagram (Figure 16-2).
 - 4: See the Oscillator System Diagram (Figure 9-1).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

FIGURE 30-6: INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS



TABLE 30-26: INPUT CAPTURE x MODULE TIMING REQUIREMENTS

АС СНА	AC CHARACTERISTICS Standard Operation Operating tempe					3.0V to 3.6V TA \leq +85°C for Indu TA \leq +125°C for Ext	strial ended	
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Max.	Units	Conditions		
IC10	TccL	ICx Input Low Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15		
IC11	ТссН	ICx Input High Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15	N = prescale value (1, 4, 16)	
IC15	TccP	ICx Input Period	Greater of 25 + 50 or (1 Tcy/N) + 50	_	ns			

Note 1: These parameters are characterized, but not tested in manufacturing.





TABLE 30-34: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS				$\label{eq:constraint} \begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param. Symbol Characteristic ⁽¹⁾				Typ. ⁽²⁾	Max.	Units	Conditions	
SP10	FscP	Maximum SCK2 Frequency	—	_	15	MHz	(Note 3)	
SP20	TscF	SCK2 Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)	
SP21	TscR	SCK2 Output Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO2 Data Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO2 Data Output Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns		
SP36	TdiV2scH, TdiV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	_	ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

DC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)(1)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial								
			$-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended							
Param No.	Symbol	Characteristic	Min.	Тур. ⁽²⁾	Max.	Units	Conditions			
Compa	rator AC Ch	naracteristics								
CM10	Tresp	Response Time ⁽³⁾	_	19	_	ns	V+ input step of 100 mV, V- input held at VDD/2			
CM11	Тмс2о∨	Comparator Mode Change to Output Valid		_	10	μs				
Compa	Comparator DC Characteristics									
CM30	VOFFSET	Comparator Offset Voltage	—	±10	40	mV				
CM31	VHYST	Input Hysteresis Voltage ⁽³⁾	_	30	—	mV				
CM32	Trise/ Tfall	Comparator Output Rise/ Fall Time ⁽³⁾	—	20	—	ns	1 pF load capacitance on input			
CM33	Vgain	Open-Loop Voltage Gain ⁽³⁾	—	90	—	db				
CM34	VICM	Input Common-Mode Voltage	AVss	—	AVdd	V				
Op Am	p AC Chara	cteristics								
CM20	SR	Slew Rate ⁽³⁾		9		V/µs	10 pF load			
CM21a	Рм	Phase Margin (Configuration A) ^(3,4)	_	55	—	Degree	G = 100V/V; 10 pF load			
CM21b	Рм	Phase Margin (Configuration B) ^(3,5)	—	40	_	Degree	G = 100V/V; 10 pF load			
CM22	Gм	Gain Margin ⁽³⁾	—	20	—	db	G = 100V/V; 10 pF load			
CM23a	GBW	Gain Bandwidth (Configuration A) ^(3,4)	_	10	—	MHz	10 pF load			
CM23b	Gвw	Gain Bandwidth (Configuration B) ^(3,5)	—	6	_	MHz	10 pF load			

TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
- 3: Parameter is characterized but not tested in manufacturing.
- 4: See Figure 25-6 for configuration information.
- 5: See Figure 25-7 for configuration information.
- 6: Resistances can vary by ±10% between op amps.

31.2 **AC Characteristics and Timing Parameters**

The information contained in this section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in Section 30.2 "AC Characteristics and Timing Parameters", with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in Section 30.2 "AC Characteristics and Timing Parameters" is the Industrial and Extended temperature equivalent of HOS53.

TABLE 31-9: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

	Standard Operating Conditions: 3.0V to 3.6V
	(unless otherwise stated)
AC CHARACTERISTICS	Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$
	Operating voltage VDD range as described in Table 31-1.

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



TABLE 31-10: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Param No. Symbol Characteristic		Min	Тур	Max	Units	Conditions	
HOS53	DCLK	CLKO Stability (Jitter) ⁽¹⁾	-5	0.5	5	%	Measured over 100 ms period

These parameters are characterized by similarity, but are not tested in manufacturing. This specification is Note 1: based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time bases or communication clocks use this formula:

$$Peripheral Clock Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Peripheral Bit Rate Clock}}}$$

For example: FOSC = 32 MHz, DCLK = 5%, SPIx bit rate clock (i.e., SCKx) is 2 MHz. Г

$$SPI SCK Jitter = \left\lfloor \frac{D_{CLK}}{\sqrt{\left(\frac{32 MHz}{2 MHz}\right)}} \right\rfloor = \left\lfloor \frac{5\%}{\sqrt{16}} \right\rfloor = \left\lfloor \frac{5\%}{4} \right\rfloor = 1.25\%$$

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44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	Ν		44		
Number of Pins per Side	ND		12		
Number of Pins per Side	NE		10		
Pitch	е	0.50 BSC			
Overall Height	Α	0.80	0.90	1.00	
Standoff	A1	0.025	-	0.075	
Overall Width	Е	6.00 BSC			
Exposed Pad Width	E2	4.40	4.55	4.70	
Overall Length	D	6.00 BSC			
Exposed Pad Length	D2	4.40	4.55	4.70	
Contact Width	b	0.20	0.25	0.30	
Contact Length	L	0.20	0.25	0.30	
Contact-to-Exposed Pad	К	0.20	-	-	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-157C Sheet 2 of 2

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