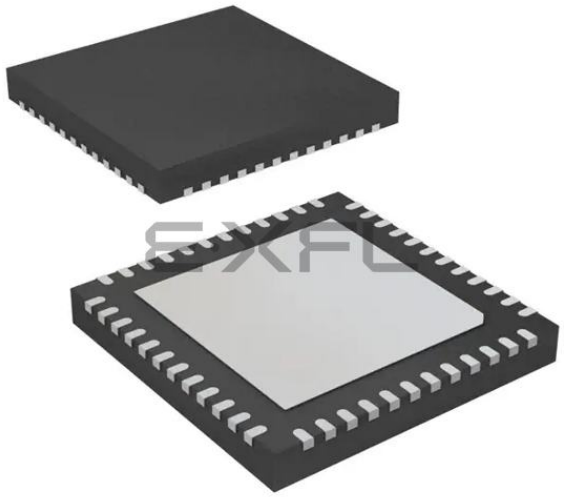
Microchip Technology - DSPIC33EP32MC204-E/MV Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

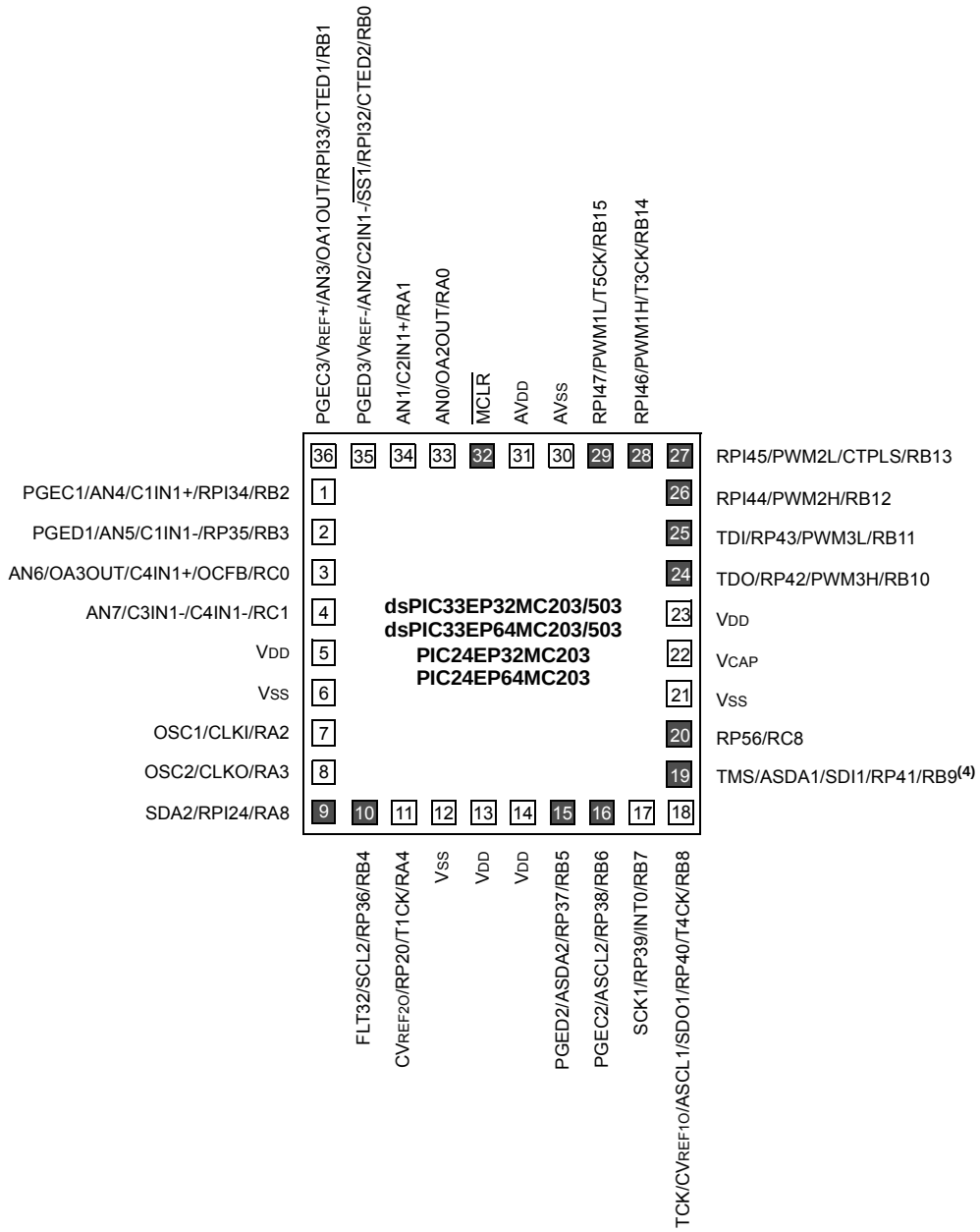
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc204-e-mv

Pin Diagrams (Continued)

36-Pin VTLA(1,2,3)

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

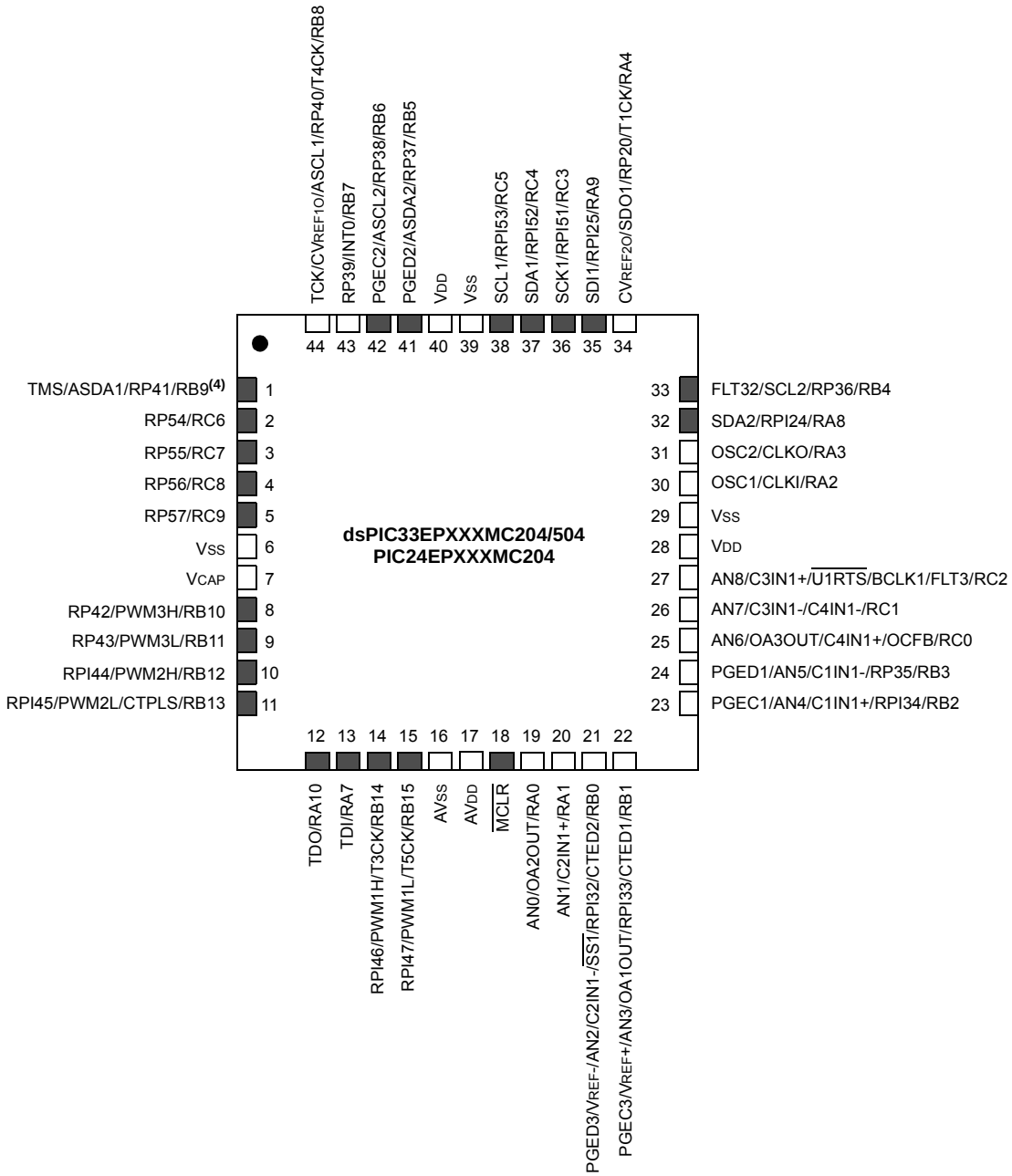
3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Pin Diagrams (Continued)

44-Pin QFN(1,2,3)

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

TABLE 4-23: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400-041E	See definition when WIN = x																
C1BUFPNT1	0420	F3BP<3:0>				F2BP<3:0>				F1BP<3:0>				F0BP<3:0>				0000
C1BUFPNT2	0422	F7BP<3:0>				F6BP<3:0>				F5BP<3:0>				F4BP<3:0>				0000
C1BUFPNT3	0424	F11BP<3:0>				F10BP<3:0>				F9BP<3:0>				F8BP<3:0>				0000
C1BUFPNT4	0426	F15BP<3:0>				F14BP<3:0>				F13BP<3:0>				F12BP<3:0>				0000
C1RXM0SID	0430	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM0EID	0432	EID<15:8>								EID<7:0>								xxxx
C1RXM1SID	0434	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM1EID	0436	EID<15:8>								EID<7:0>								xxxx
C1RXM2SID	0438	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM2EID	043A	EID<15:8>								EID<7:0>								xxxx
C1RXF0SID	0440	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF0EID	0442	EID<15:8>								EID<7:0>								xxxx
C1RXF1SID	0444	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF1EID	0446	EID<15:8>								EID<7:0>								xxxx
C1RXF2SID	0448	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF2EID	044A	EID<15:8>								EID<7:0>								xxxx
C1RXF3SID	044C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF3EID	044E	EID<15:8>								EID<7:0>								xxxx
C1RXF4SID	0450	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF4EID	0452	EID<15:8>								EID<7:0>								xxxx
C1RXF5SID	0454	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF5EID	0456	EID<15:8>								EID<7:0>								xxxx
C1RXF6SID	0458	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF6EID	045A	EID<15:8>								EID<7:0>								xxxx
C1RXF7SID	045C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF7EID	045E	EID<15:8>								EID<7:0>								xxxx
C1RXF8SID	0460	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF8EID	0462	EID<15:8>								EID<7:0>								xxxx
C1RXF9SID	0464	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF9EID	0466	EID<15:8>								EID<7:0>								xxxx
C1RXF10SID	0468	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF10EID	046A	EID<15:8>								EID<7:0>								xxxx
C1RXF11SID	046C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.6 Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.6.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified, and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.6.2 W ADDRESS REGISTER SELECTION

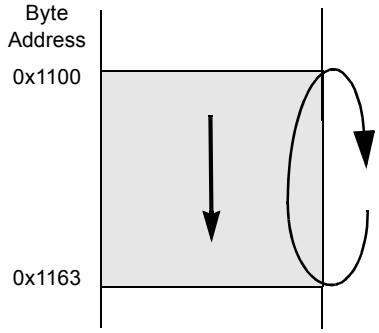
The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '1111' and the XMODEN bit is set (MODCON<15>).

The Y Address Space Pointer W register (YWM), to which Modulo Addressing is to be applied, is stored in MODCON<7:4>. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '1111' and the YMODEN bit is set at MODCON<14>.

FIGURE 4-20: MODULO ADDRESSING OPERATION EXAMPLE




```
MOV     #0x1100, W0
MOV     W0, XMODSRT     ;set modulo start address
MOV     #0x1163, W0
MOV     W0, MODEND      ;set modulo end address
MOV     #0x8001, W0
MOV     W0, MODCON      ;enable W1, X AGU for modulo

MOV     #0x0000, W0     ;W0 holds buffer fill value

MOV     #0x1110, W1     ;point W1 to buffer

DO      AGAIN, #0x31    ;fill the 50 buffer locations
MOV     W0, [W1++]      ;fill the next location
AGAIN:  INC W0, W0      ;increment the fill value
```

8.0 DIRECT MEMORY ACCESS (DMA)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Direct Memory Access (DMA)"** (DS70348) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The DMA Controller transfers data between Peripheral Data registers and Data Space SRAM

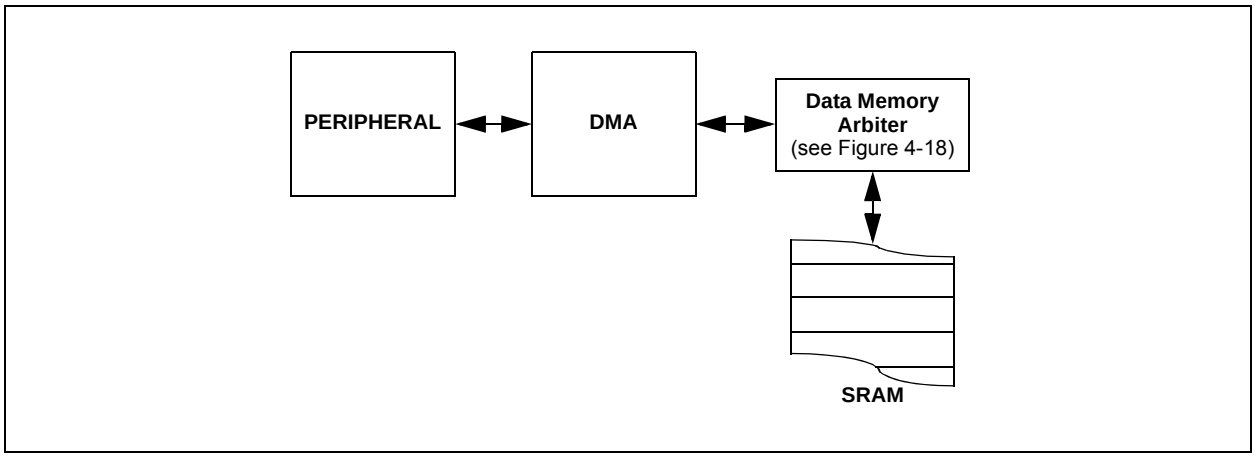
In addition, DMA can access the entire data memory space. The Data Memory Bus Arbiter is utilized when either the CPU or DMA attempts to access SRAM, resulting in potential DMA or CPU stalls.

The DMA Controller supports 4 independent channels. Each channel can be configured for transfers to or from selected peripherals. Some of the peripherals supported by the DMA Controller include:

- ECAN™
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI)
- UART
- Input Capture
- Output Compare

Refer to Table 8-1 for a complete list of supported peripherals.

FIGURE 8-1: DMA CONTROLLER MODULE



NOTES:

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits

11111 = OCxRS compare event is used for synchronization
11110 = INT2 pin synchronizes or triggers OCx
11101 = INT1 pin synchronizes or triggers OCx
11100 = CTMU module synchronizes or triggers OCx
11011 = ADC1 module synchronizes or triggers OCx
11010 = CMP3 module synchronizes or triggers OCx
11001 = CMP2 module synchronizes or triggers OCx
11000 = CMP1 module synchronizes or triggers OCx
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = Reserved
10011 = IC4 input capture event synchronizes or triggers OCx
10010 = IC3 input capture event synchronizes or triggers OCx
10001 = IC2 input capture event synchronizes or triggers OCx
10000 = IC1 input capture event synchronizes or triggers OCx
01111 = Timer5 synchronizes or triggers OCx
01110 = Timer4 synchronizes or triggers OCx
01101 = Timer3 synchronizes or triggers OCx
01100 = Timer2 synchronizes or triggers OCx **(default)**
01011 = Timer1 synchronizes or triggers OCx
01010 = PTGOx synchronizes or triggers OCx**(3)**
01001 = Reserved
01000 = Reserved
00111 = Reserved
00110 = Reserved
00101 = Reserved
00100 = OC4 module synchronizes or triggers OCx**(1,2)**
00011 = OC3 module synchronizes or triggers OCx**(1,2)**
00010 = OC2 module synchronizes or triggers OCx**(1,2)**
00001 = OC1 module synchronizes or triggers OCx**(1,2)**
00000 = No Sync or Trigger source for OCx

Note 1: Do not use the OCx module as its own Synchronization or Trigger source.

2: When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

3: Each Output Compare x module (OCx) has one PTG Trigger/Synchronization source. See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO0 = OC1
PTGO1 = OC2
PTGO2 = OC3
PTGO3 = OC4

REGISTER 17-15: QEI1GECH: QEI1 GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **QEIGEC<31:16>:** High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

REGISTER 17-16: QEI1GECL: QEI1 GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER

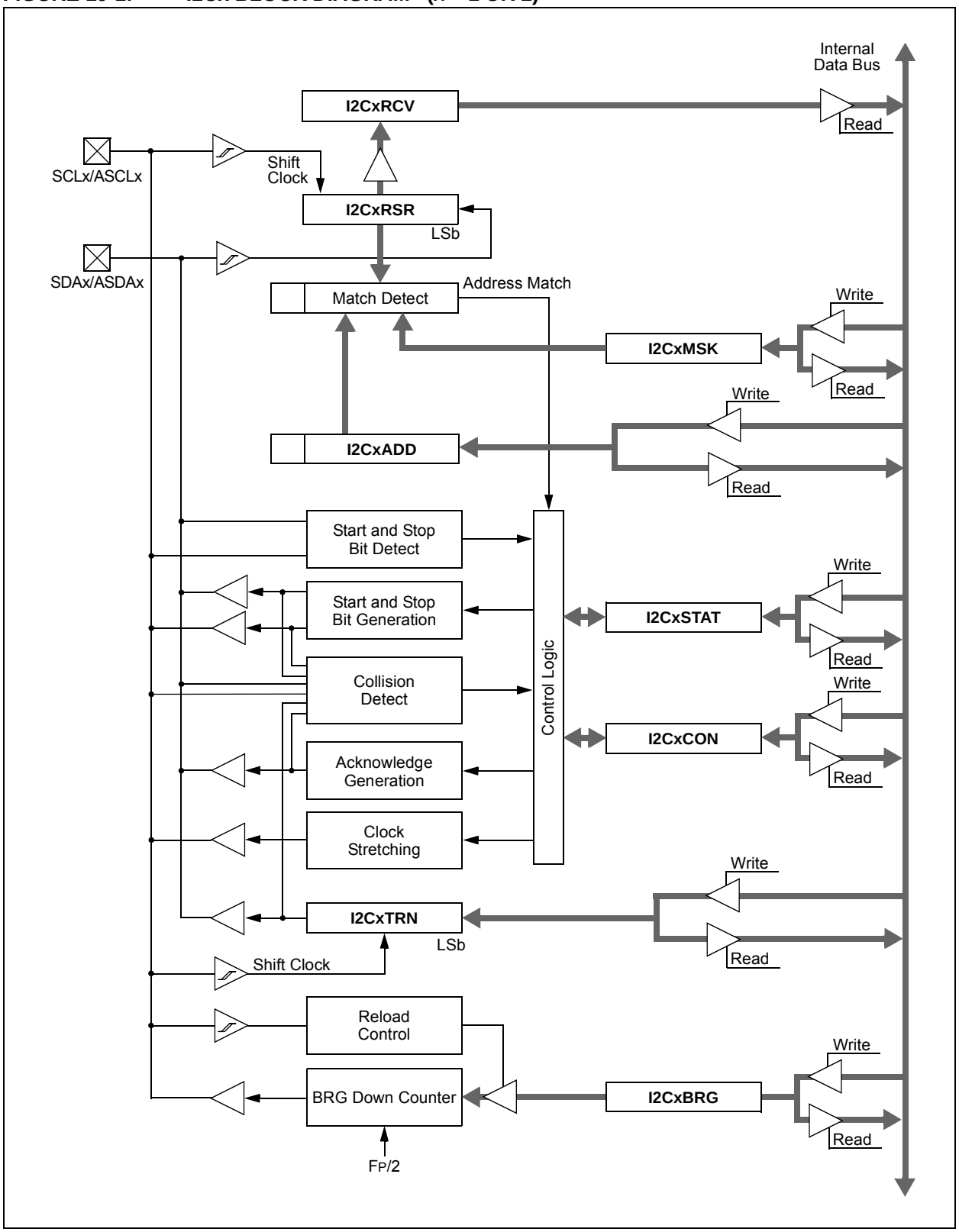
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **QEIGEC<15:0>:** Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

FIGURE 19-1: I2Cx BLOCK DIAGRAM (x = 1 OR 2)



REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN(1)	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 **UTXISEL<1:0>:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** UARTx Transmit Polarity Inversion bit

If IREN = 0:
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IREN = 1:
- 1 = IrDA encoded, UxTX Idle state is '1'
- 0 = IrDA encoded, UxTX Idle state is '0'

bit 12 **Unimplemented:** Read as '0'

bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or completed

bit 10 **UTXEN:** UARTx Transmit Enable bit(1)
- 1 = Transmit is enabled, UxTX pin is controlled by UARTx
- 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; UxTX pin is controlled by the PORT

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
- 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
- 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters

Note 1: Refer to the **"UART"** (DS70582) section in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **EID<15:0>:** Extended Identifier bits
1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MSK<1:0>		F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **F7MSK<1:0>:** Mask Source for Filter 7 bits
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F6MSK<1:0>:** Mask Source for Filter 6 bits (same values as bits<15:14>)

bit 11-10 **F5MSK<1:0>:** Mask Source for Filter 5 bits (same values as bits<15:14>)

bit 9-8 **F4MSK<1:0>:** Mask Source for Filter 4 bits (same values as bits<15:14>)

bit 7-6 **F3MSK<1:0>:** Mask Source for Filter 3 bits (same values as bits<15:14>)

bit 5-4 **F2MSK<1:0>:** Mask Source for Filter 2 bits (same values as bits<15:14>)

bit 3-2 **F1MSK<1:0>:** Mask Source for Filter 1 bits (same values as bits<15:14>)

bit 1-0 **F0MSK<1:0>:** Mask Source for Filter 0 bits (same values as bits<15:14>)

NOTES:

TABLE 30-39: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK2 Input Frequency	—	—	15	MHz	**(Note 3)**
SP72	TscF	SCK2 Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS2}$ ↑ to SDO2 Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH TscL2ssH	$\overline{SS2}$ ↑ after SCK2 Edge	1.5 TCY + 40	—	—	ns	**(Note 4)**

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-34: ECANx MODULE I/O TIMING CHARACTERISTICS

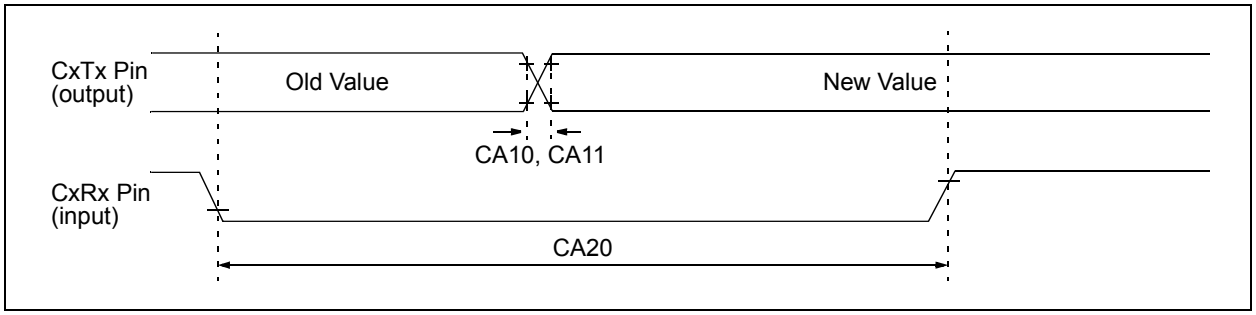


TABLE 30-51: ECANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
CA10	TIOF	Port Output Fall Time	—	—	—	ns	See Parameter DO32
CA11	TIOR	Port Output Rise Time	—	—	—	ns	See Parameter DO31
CA20	TCWF	Pulse Width to Trigger CAN Wake-up Filter	120	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 30-35: UARTx MODULE I/O TIMING CHARACTERISTICS

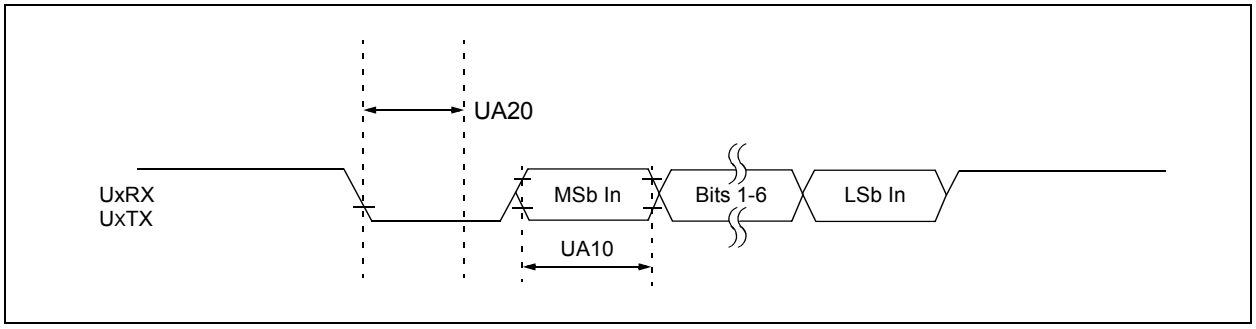


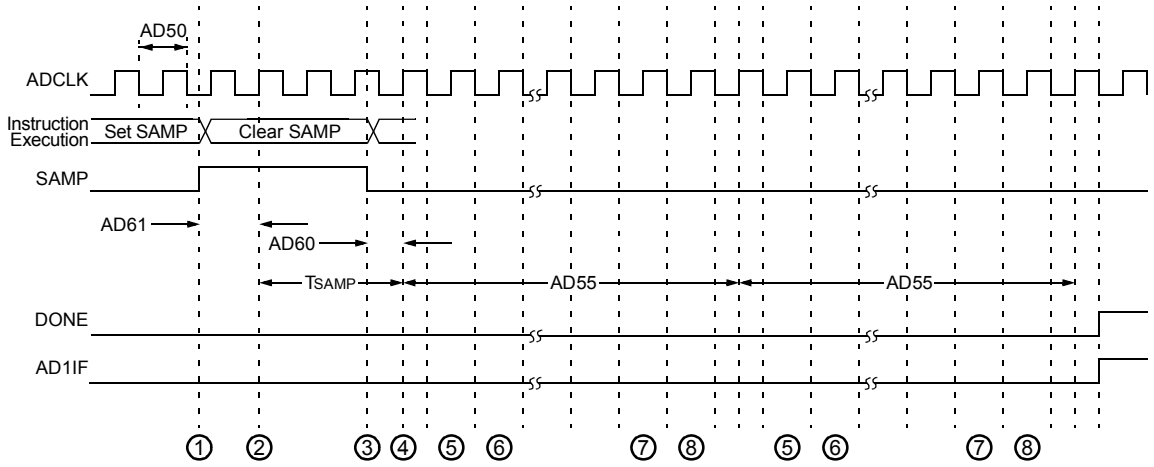
TABLE 30-52: UARTx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
UA10	TUABAUD	UARTx Baud Time	66.67	—	—	ns	
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps	
UA20	TCWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 30-37: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)



1 – Software sets AD1CON1. SAMP to start sampling.

2 – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*.

3 – Software clears AD1CON1. SAMP to start conversion.

4 – Sampling ends, conversion sequence starts.

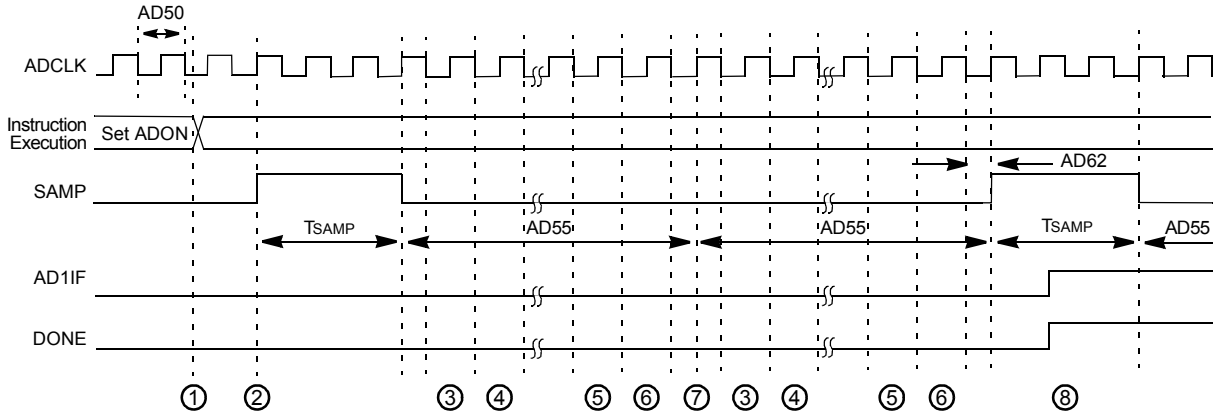
5 – Convert bit 9.

6 – Convert bit 8.

7 – Convert bit 0.

8 – One TAD for end of conversion.

FIGURE 30-38: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SSRCG = 0, SAMC<4:0> = 00010)



1 – Software sets AD1CON1. ADON to start AD operation.

2 – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*.

3 – Convert bit 9.

4 – Convert bit 8.

5 – Convert bit 0.

6 – One TAD for end of conversion.

7 – Begin conversion of next channel.

8 – Sample for time specified by SAMC<4:0>.

TABLE 31-12: ADC MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-Bit Mode)(1)							
HAD20a	Nr	Resolution(3)	12 Data Bits			bits	
HAD21a	INL	Integral Nonlinearity	-5.5	—	5.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD22a	DNL	Differential Nonlinearity	-1	—	1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD23a	GERR	Gain Error	-10	—	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD24a	EOFF	Offset Error	-5	—	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
Dynamic Performance (12-Bit Mode)(2)							
HAD33a	FNYQ	Input Signal Bandwidth	—	—	200	kHz	

Note 1: These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

TABLE 31-13: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (10-Bit Mode)(1)							
HAD20b	Nr	Resolution(3)	10 Data Bits			bits	
HAD21b	INL	Integral Nonlinearity	-1.5	—	1.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD22b	DNL	Differential Nonlinearity	-0.25	—	0.25	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD23b	GERR	Gain Error	-2.5	—	2.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
HAD24b	EOFF	Offset Error	-1.25	—	1.25	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
Dynamic Performance (10-Bit Mode)(2)							
HAD33b	FNYQ	Input Signal Bandwidth	—	—	400	kHz	

Note 1: These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

FIGURE 32-5: TYPICAL IPD CURRENT @ VDD = 3.3V

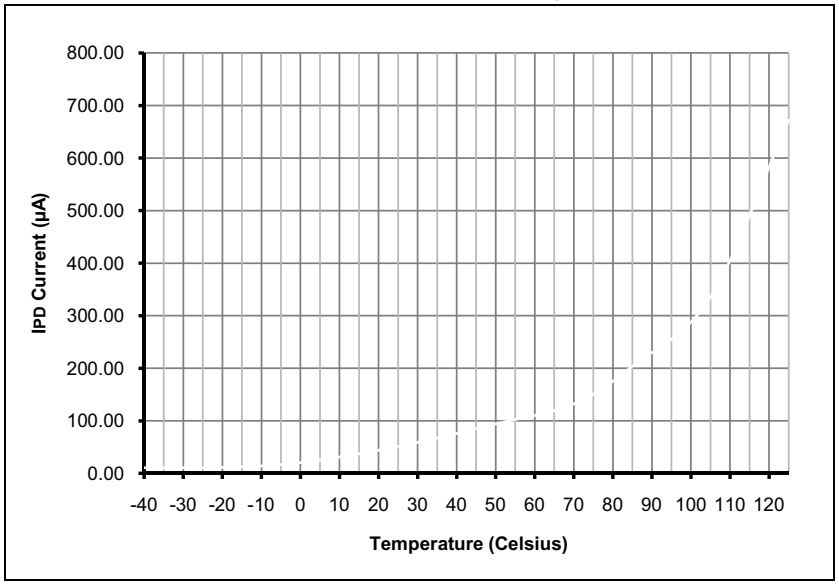


FIGURE 32-6: TYPICAL/MAXIMUM IDD CURRENT @ VDD = 3.3V

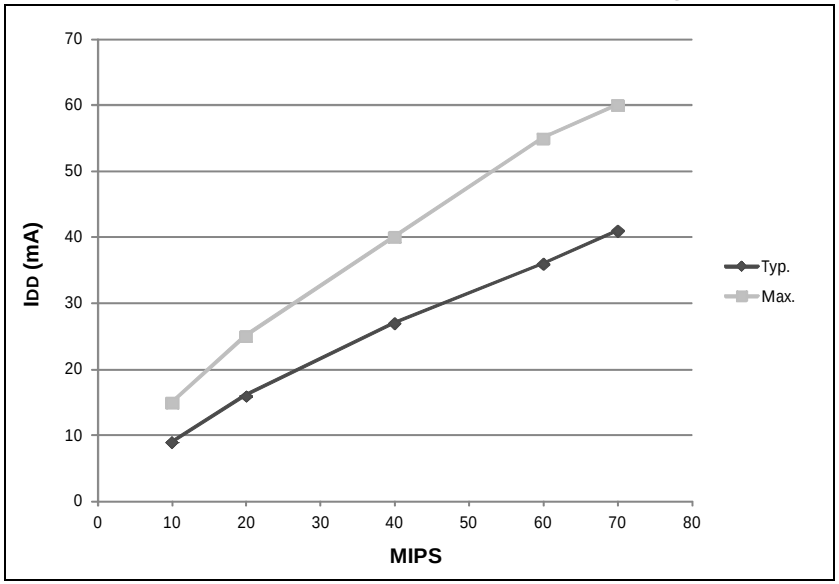


FIGURE 32-7: TYPICAL IDOZE CURRENT @ VDD = 3.3V

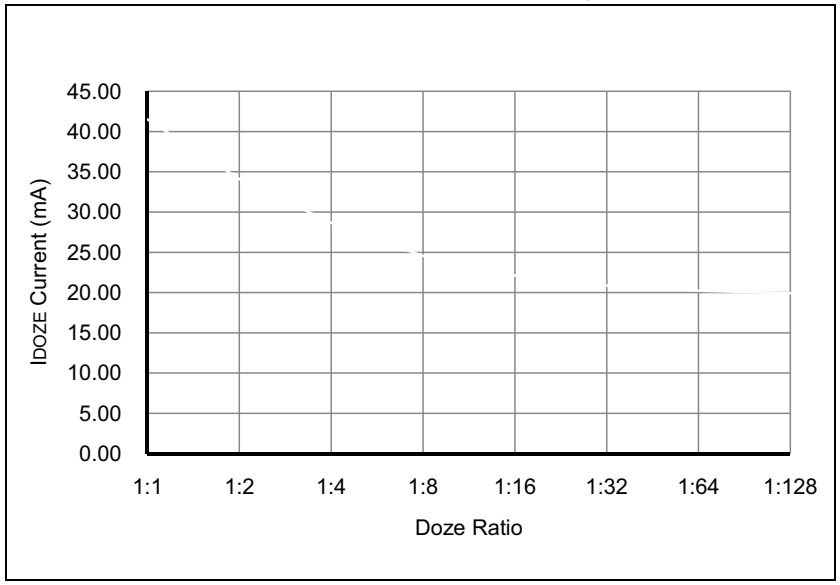
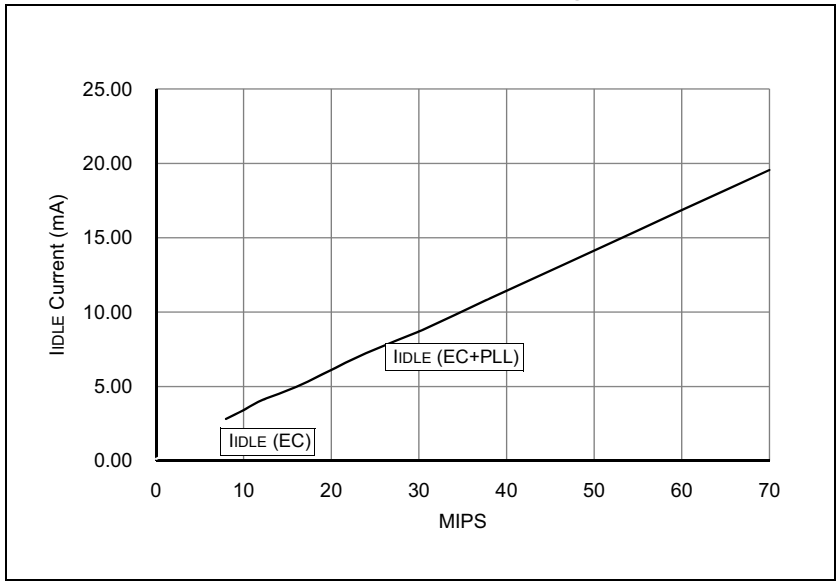


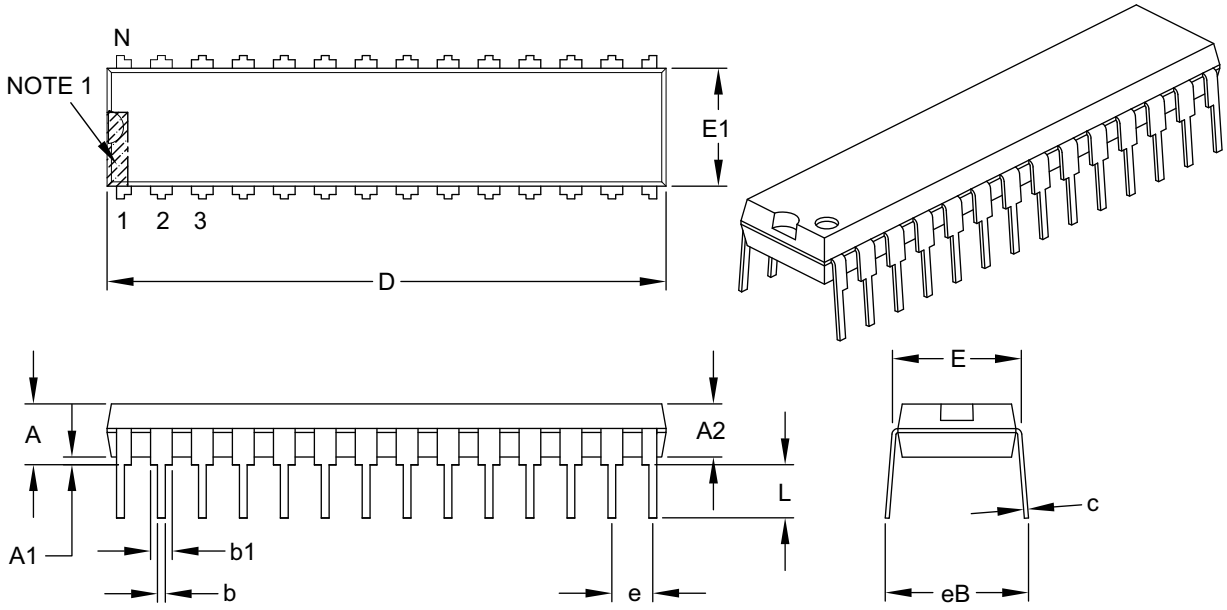
FIGURE 32-8: TYPICAL IIDLE CURRENT @ VDD = 3.3V



33.2 Package Details

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

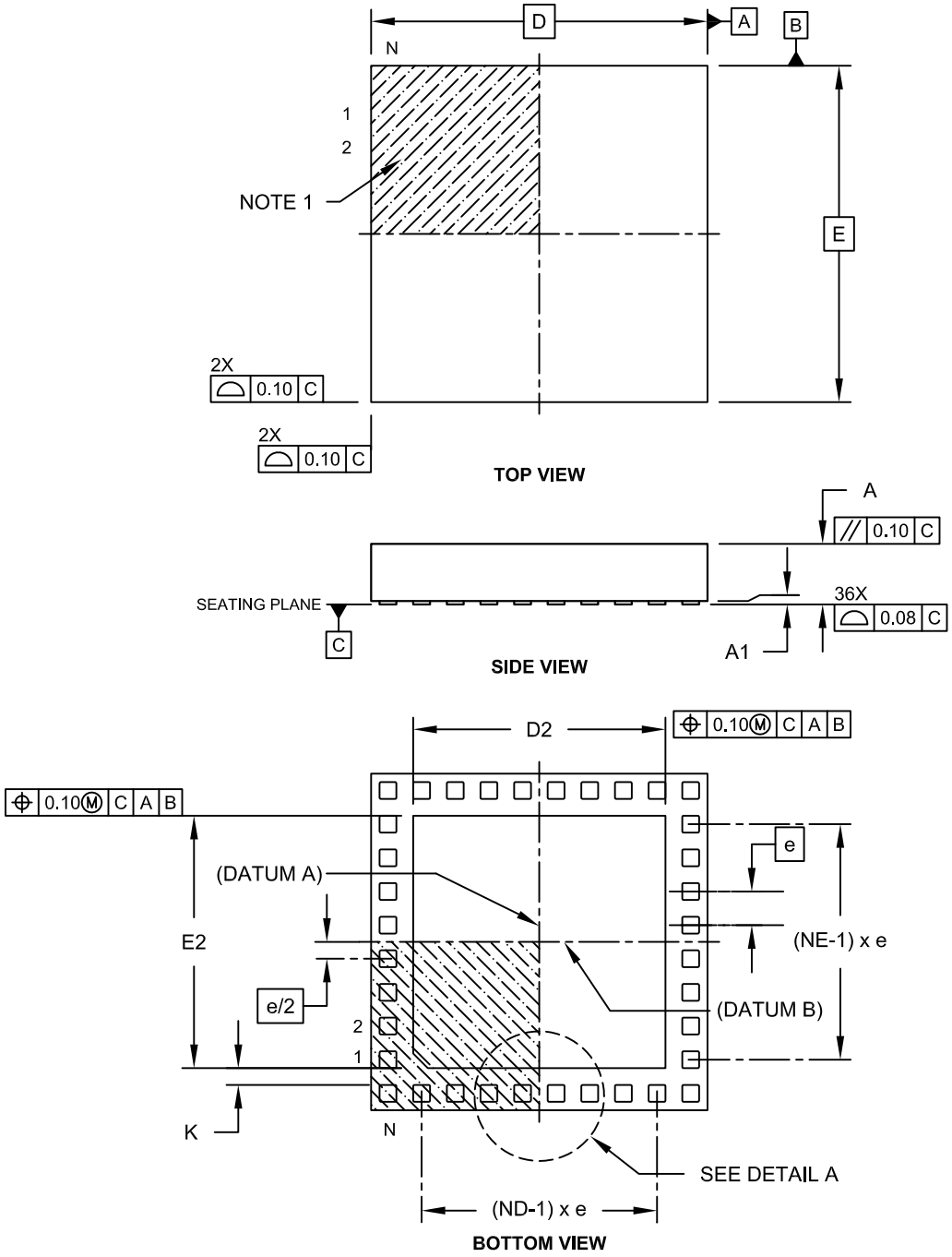
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-187C Sheet 1 of 2

NOTES: