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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc204-h-tl

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4.5.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions. which apply to dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and the DSP accumulator class of instructions, which apply to the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.5.4 MAC INSTRUCTIONS (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X DEVICES ONLY)

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY. N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The Two-Source Operand Prefetch registers must be members of the set: {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the ${\tt MAC}$ class of instructions:

- · Register Indirect
- Register Indirect Post-Modified by 2
- · Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.5.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

5.0 FLASH PROGRAM MEMORY

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP/MC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows for a dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data a single program memory word, and erase program memory in blocks or 'pages' of 1024 instructions (3072 bytes) at a time.

5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CHEN	SIZE	DIR	HALF	NULLW	_	—	—
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
		AMODE1	AMODE0			MODE1	MODE0
bit 7							bit 0
Legend:			,			(0)	
R = Readable	bit	W = Writable	bit		mented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		0^{\prime} = Bit is cle	eared	x = Bit is unkn	IOWN
bit 15		Channel Enabl	o hit				
bit 15	1 = Channel	is enabled					
	0 = Channel	is disabled					
bit 14	SIZE: DMA D	ata Transfer Si	ze bit				
	1 = Byte						
	0 = Word						
bit 13	DIR: DMA Transfer Direction bit (source/destination bus select)						
	\perp = Reads from RAM address, writes to peripheral address 0 = Reads from peripheral address, writes to RAM address						
bit 12	HALF: DMA	Block Transfer	Interrupt Sele	ct bit			
	1 = Initiates i	nterrupt when I	nalf of the dat	a has been mo	oved		
	0 = Initiates i	nterrupt when a	all of the data	has been mov	ved		
bit 11	NULLW: Null Data Peripheral Write Mode Select bit						
	1 = Null data write to peripheral in addition to RAM write (DIR bit must also be clear)						
bit 10-6	Unimplemen	ted: Read as '	ר'				
bit 5-4	AMODE<1:0	: DMA Channe	el Addressina	Mode Select	bits		
	11 = Reserve	ed					
	10 = Peripher	ral Indirect Add	ressing mode				
	01 = Register	Indirect withou	ut Post-Increm	nent mode			
hit 3 2		tod: Pood as '	ost-incremen	tmode			
bit 1_0		DMA Channel	Operating Mc	nda Salact hits			
bit 1-0	11 = One-Sh	ot. Pina-Pona r	nodes are en	abled (one blo	ck transfer from	/to each DMA b	ouffer)
	10 = Continue	ous, Ping-Pong	modes are e	nabled			
	01 = One-Sho	ot, Ping-Pong r	nodes are dis	abled			
		ous, Ping-Pong	modes are d	ISADIEO			

REGISTER 8-1: DMAXCON: DMA CHANNEL X CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	_	PPST3	PPST2	PPST1	PPST0
bit 7							bit 0

REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

Legend:						
R = Readable bit -n = Value at POR		W = Writable bit	U = Unimplemented bit, read as '0'			
		'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		
bit 15-4 Unimplemented: Read as '0'						
bit 3 PPST3: DM		MA Channel 3 Ping-Pong	Mode Status Flag bit			
	1 = DMA	STB3 register is selected				
	0 = DMA	STA3 register is selected				
bit 2	PPST2: [MA Channel 2 Ping-Pong	Mode Status Flag bit			
	1 = DMA	STB2 register is selected				
	0 = DMA	STA2 register is selected				
bit 1	PPST1: [MA Channel 1 Ping-Pong	Mode Status Flag bit			

- 1 = DMASTB1 register is selected0 = DMASTA1 register is selected
- bit 0 PPST0: DMA Channel 0 Ping-Pong Mode Status Flag bit
 - 1 = DMASTB0 register is selected
 - 0 = DMASTA0 register is selected

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

- bit 3 SPI1MD: SPI1 Module Disable bit 1 = SPI1 module is disabled
 - 0 = SPI1 module is enabled
- bit 2 Unimplemented: Read as '0'
- bit 1 C1MD: ECAN1 Module Disable bit⁽²⁾ 1 = ECAN1 module is disabled 0 = ECAN1 module is enabled
- bit 0 AD1MD: ADC1 Module Disable bit 1 = ADC1 module is disabled 0 = ADC1 module is enabled
- Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
 - 2: This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP43	R<5:0>		
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP42	R<5:0>		

REGISTER 11-22: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

bit	7

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	RP43R<5:0>: Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP42R<5:0>: Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-23: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP55	SR<5:0>		
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP54	R<5:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	RP55R<5:0>: Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP54R<5:0>: Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 0

REGISTER 16-2: PTCON2: PWMx PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER
--

U-0	U-0	U-0	U-0	U-0	U-0 U-0 U-0		U-0	
—	—	—	_				—	
bit 15	pit 15							
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
	_	—	—	—	PCLKDIV2 ⁽¹⁾	PCLKDIV1 ⁽¹⁾	PCLKDIV0(1)	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'		
-n = Value at POR '1' = Bit is set				'0' = Bit is cleared x = Bit			iown	
hit 15.2 Unimplemented: Read as (a)								

bit 15-3 Unimplemented: Read as '0'

bit 2-0 PCLKDIV<2:0>: PWMx Input Clock Prescaler (Divider) Select bits⁽¹⁾

- 111 = Reserved 110 = Divide-by-64 101 = Divide-by-32
- 100 = Divide-by-32100 = Divide-by-16
- 011 = Divide-by-8
- 010 = Divide-by-4
- 001 = Divide-by-2
- 000 = Divide-by-1, maximum PWMx timing resolution (power-on default)
- **Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 16-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	id as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 **PDCx<15:0>:** PWMx Generator # Duty Cycle Value bits

REGISTER 16-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	Ex<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	SEx<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable b	it	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkı	nown

bit 15-0 PHASEx<15:0>: PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs

 If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0		
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_		
bit 15	1		1		1		bit 8		
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—	—	BCH(")	BCL	BPHH	BPHL	BPLH	BPLL		
bit 7							bit 0		
Leaend:									
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'			
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown		
bit 15	PHR: PWMxH	Rising Edge	Trigger Enabl	e bit					
	\perp = Rising edg 0 = Leading-E	ge of PyvivixH v Edge Blanking i	anores risina	edge of PWM	anking counter kH				
bit 14	PHF: PWMxH	Falling Edge	Trigger Enabl	e bit					
	1 = Falling ed	ge of PWMxH	will trigger Le	ading-Edge Bla	anking counter				
	0 = Leading-E	Edge Blanking i	gnores falling	g edge of PWM	хH				
bit 13	PLR: PWMxL	. Rising Edge T	rigger Enable	e bit oding Edgo Blo	nking countor				
	0 = Leading-E	Edge Blanking i	gnores rising	edge of PWM	kL				
bit 12	PLF: PWMxL	Falling Edge T	rigger Enable	e bit					
	1 = Falling ed	ge of PWMxL	will trigger Le	ading-Edge Bla	anking counter				
	0 = Leading-E	Edge Blanking i	gnores falling	g edge of PWM	xL				
bit 11	1 = Leading-F	-ault Input Lea Edge Blanking i	ding-Edge Bla	anking Enable	bit				
	0 = Leading-E	Edge Blanking i	s not applied	to selected Fa	ult input				
bit 10	CLLEBEN: C	urrent-Limit Le	ading-Edge E	Blanking Enable	e bit				
	1 = Leading-E	Edge Blanking i	s applied to s	selected curren	t-limit input				
hit 0.6	0 = Leading-E	tode Blanking I	s not applied	to selected cul	rrent-limit input				
bit 5	BCH Blankin	a in Selected F	J Blanking Sign	al High Enable	hit(1)				
bit 5	1 = State blan	kina (of curren	t-limit and/or	Fault input sigr	nals) when seled	ted blanking s	ianal is hiah		
	0 = No blankii	ng when select	ed blanking s	signal is high	,	5	0 0		
bit 4	BCL: Blanking	g in Selected B	lanking Signa	al Low Enable I	bit ⁽¹⁾				
	1 = State blan	iking (of curren	t-limit and/or	Fault input sigr	nals) when seled	cted blanking s	ignal is low		
bit 3	BPHH: Blanki	ing in PWMxH	High Enable	hit					
bit o	1 = State blan	iking (of curren	t-limit and/or	Fault input sigr	nals) when PWN	/IxH output is h	igh		
	0 = No blanki	ng when PWM	xH output is h	nigh			-		
bit 2	BPHL: Blanki	ng in PWMxH	Low Enable b	pit					
	1 = State blan 0 = No blankii	nking (of curren ng when PWM	t-limit and/or xH output is le	Fault input sigr ow	nals) when PWN	IxH output is lo	W		
bit 1	BPLH: Blanki	ng in PWMxL I	High Enable b	oit					
	1 = State blan 0 = No blankii	nking (of curren ng when PWM	t-limit and/or xL output is h	Fault input sigr igh	nals) when PWN	/IxL output is hi	igh		
bit 0	BPLL: Blanki	ng in PWMxL L	ow Enable b	it					
	1 = State blan	king (of curren	t-limit and/or	Fault input sigr	nals) when PWN	IxL output is lo	W		
	v = i N o diankii		x∟ output is io	JVV					

REGISTER 16-16: LEBCONX: PWMx LEADING-EDGE BLANKING CONTROL REGISTER

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.



FIGURE 19-1: I2Cx BLOCK DIAGRAM (X = 1 OR 2)

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	_	—	—	BCL	GCSTAT	ADD10
bit 15					•		bit 8
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF
bit 7							bit 0
Legend:		C = Clearab	le bit	HS = Hardwa	re Settable bit	HSC = Hardware S	ettable/Clearable bit
R = Readabl	e bit	W = Writable	e bit	U = Unimplen	nented bit, read	as '0'	
-n = Value at POR '1' = Bit is set			'0' = Bit is clea	ared	x = Bit is unknown		

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

bit 15	ACKSTAT: Acknowledge Status bit (when operating as I^2C^{TM} master, applicable to master transmit operation)
	1 = NACK received from slave 0 = ACK received from slave
	Hardware is set or clear at the end of slave Acknowledge.
bit 14	TRSTAT: Transmit Status bit (when operating as I^2C master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK)
	0 = Master transmit is not in progress Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
bit 13-11	Unimplemented: Read as '0'
bit 10	BCL: Master Bus Collision Detect bit
	1 = A bus collision has been detected during a master operation0 = No bus collision detected
	Hardware is set at detection of a bus collision.
bit 9	GCSTAT: General Call Status bit
	1 = General call address was received
	0 = General call address was not received
1.11.0	Hardware is set when address matches general call address. Hardware is clear at Stop detection.
DIT 8	ADD10: 10-Bit Address Status bit
	I = 10-bit address was matched 0 = 10-bit address was not matched
	Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
bit 7	IWCOL: I2Cx Write Collision Detect bit
	1 = An attempt to write to the I2CxTRN register failed because the I^2 C module is busy 0 = No collision
	Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
bit 6	I2COV: I2Cx Receive Overflow Flag bit
	 1 = A byte was received while the I2CxRCV register was still holding the previous byte 0 = No overflow
	Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
bit 5	D_A: Data/Address bit (when operating as I ² C slave)
	1 = Indicates that the last byte received was data
	 Indicates that the last byte received was a device address Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	F15B	P<3:0>			F14B	P<3:0>	
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
-	F13B	P<3:0>		F12BP<3:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at POR		'1' = Bit is set		'0' = Bit is cle	'0' = Bit is cleared		nown
L							
bit 15-12	F15BP<3:0	>: RX Buffer Ma	sk for Filter 1	5 bits			
	1111 = Filte	er hits received in	n RX FIFO bu	uffer			
	1110 = Filte	r hits received in	n RX Buffer 1	4			
	•						
	•						
	•	n hito no ocivio d iv					
	0001 = Filte	r hits received ii	DRX Builler I				
h:+ 44 0				4 h:ta (a a ma a ma)			
DIT 11-8	F14BP<3:0	>: RX Buffer Ma	SK for Fliter 1	4 bits (same va	iues as bits<15):12>)	
bit 7-4	F13BP<3:0	>: RX Buffer Ma	sk for Filter 1	3 bits (same va	lues as bits<15	5:12>)	
bit 3-0 F12BP<3:0>: RX Buffer Mask for Filter 12 bits (same values as bits<15:12>)							

REGISTER 21-15: CxBUFPNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4

REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER (CONTINUED)

- bit 3-0 SELSRCA<3:0>: Mask A Input Select bits
 - 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0101 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H 0000 = PWM1L

29.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

29.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

29.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a highspeed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

29.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a fullspeed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming[™] (ICSP[™]).

29.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

DC CHARACT	ERISTICS		Standard O (unless othe Operating te	perating Condition erwise stated) emperature -40°C -40°C	s: 3.0V to 3.6V ≤ Ta ≤ +85°C for Ind ≤ Ta ≤ +125°C for E	ustrial ktended		
Parameter No.	Тур.	Max.	Units	Conditions				
Operating Cur	rent (IDD) ⁽¹⁾							
DC20d	9	15	mA	-40°C				
DC20a	9	15	mA	+25°C	3 3\/			
DC20b	9	15	mA	+85°C	3.5 V	TO MIPS		
DC20c	9	15	mA	+125°C				
DC22d	16	25	mA	-40°C				
DC22a	16	25	mA	+25°C	3.3V			
DC22b	16	25	mA	+85°C		20 WIF 3		
DC22c	16	25	mA	+125°C				
DC24d	27	40	mA	-40°C				
DC24a	27	40	mA	+25°C	2 2)/			
DC24b	27	40	mA	+85°C	3.3V	40 101175		
DC24c	27	40	mA	+125°C				
DC25d	36	55	mA	-40°C				
DC25a	36	55	mA	+25°C	2.21/			
DC25b	36	55	mA	+85°C	3.3V	60 MIPS		
DC25c	36	55	mA	+125°C				
DC26d	41	60	mA	-40°C				
DC26a	41	60	mA	+25°C	3.3V	70 MIPS		
DC26b	41	60	mA	+85°C	7			

TABLE 30-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

• Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration Word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing while(1) {NOP(); } statement
- · JTAG is disabled



			Standard Ope (unless other) Operating tem	rating Co wise state perature	pnditions: 3.0V to 3.6V ed) $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended			
Param No.	Symb	Characteristic	Min.	Тур. ⁽¹⁾	Max.	Units	Conditions	
OS10 FIN		External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	_	60	MHz	EC	
		Oscillator Crystal Frequency	3.5 10	—	10 25	MHz MHz	XT HS	
OS20	Tosc	Tosc = 1/Fosc	8.33	—	DC	ns	+125°C	
		Tosc = 1/Fosc	7.14	—	DC	ns	+85°C	
OS25	TCY	Instruction Cycle Time ⁽²⁾	16.67	—	DC	ns	+125°C	
		Instruction Cycle Time ⁽²⁾	14.28	—	DC	ns	+85°C	
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x Tosc	—	0.55 x Tosc	ns	EC	
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC	
OS40	TckR	CLKO Rise Time ^(3,4)	—	5.2	—	ns		
OS41	TckF	CLKO Fall Time ^(3,4)	—	5.2	—	ns		
OS42	Gм	External Oscillator Transconductance ⁽⁴⁾	—	12	—	mA/V	HS, VDD = 3.3V, TA = +25°C	
			—	6	—	mA/V	XT, VDD = 3.3V, TA = +25°C	

TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- 2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.
- 3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
- 4: This parameter is characterized, but not tested in manufacturing.

TABLE 30-48:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)TIMING REQUIREMENTS

АС СНА	ARACTERIS	TICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency		_	11	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	_		_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time			_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120		—	ns	
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	_	ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

NOTES:

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Microchip Technology Drawing C04-052C Sheet 1 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	Units	MILLIMETERS				
Dimension	l Limits	MIN	NOM	MAX		
Number of Pins	Ν		28			
Pitch	е		1.27 BSC			
Overall Height	Α	-	-	2.65		
Molded Package Thickness	A2	2.05	-	-		
Standoff §	A1	0.10	-	0.30		
Overall Width	E	10.30 BSC				
Molded Package Width	E1	7.50 BSC				
Overall Length	D		17.90 BSC			
Chamfer (Optional)	h	0.25	-	0.75		
Foot Length	L	0.40	-	1.27		
Footprint	L1		1.40 REF			
Lead Angle	Θ	0°	-	-		
Foot Angle	φ	0°	-	8°		
Lead Thickness	С	0.18	-	0.33		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5°	-	15°		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2