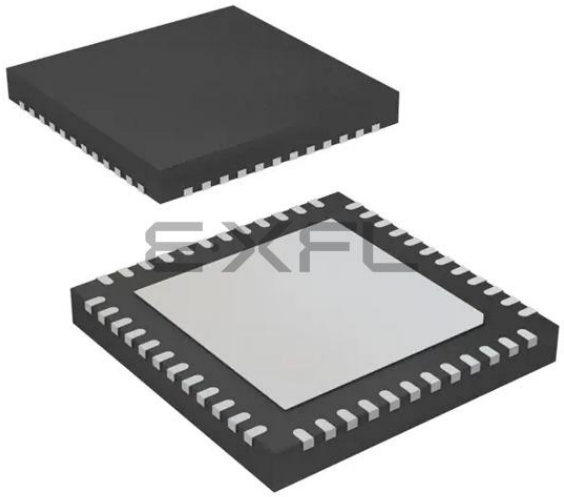
# Microchip Technology - DSPIC33EP32MC204-I/MV Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | I²C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 32KB (10.7K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 9x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-UFQFN Exposed Pad |
| Supplier Device Package | 48-UQFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc204-i-mv |

## 1.0 DEVICE OVERVIEW

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com)

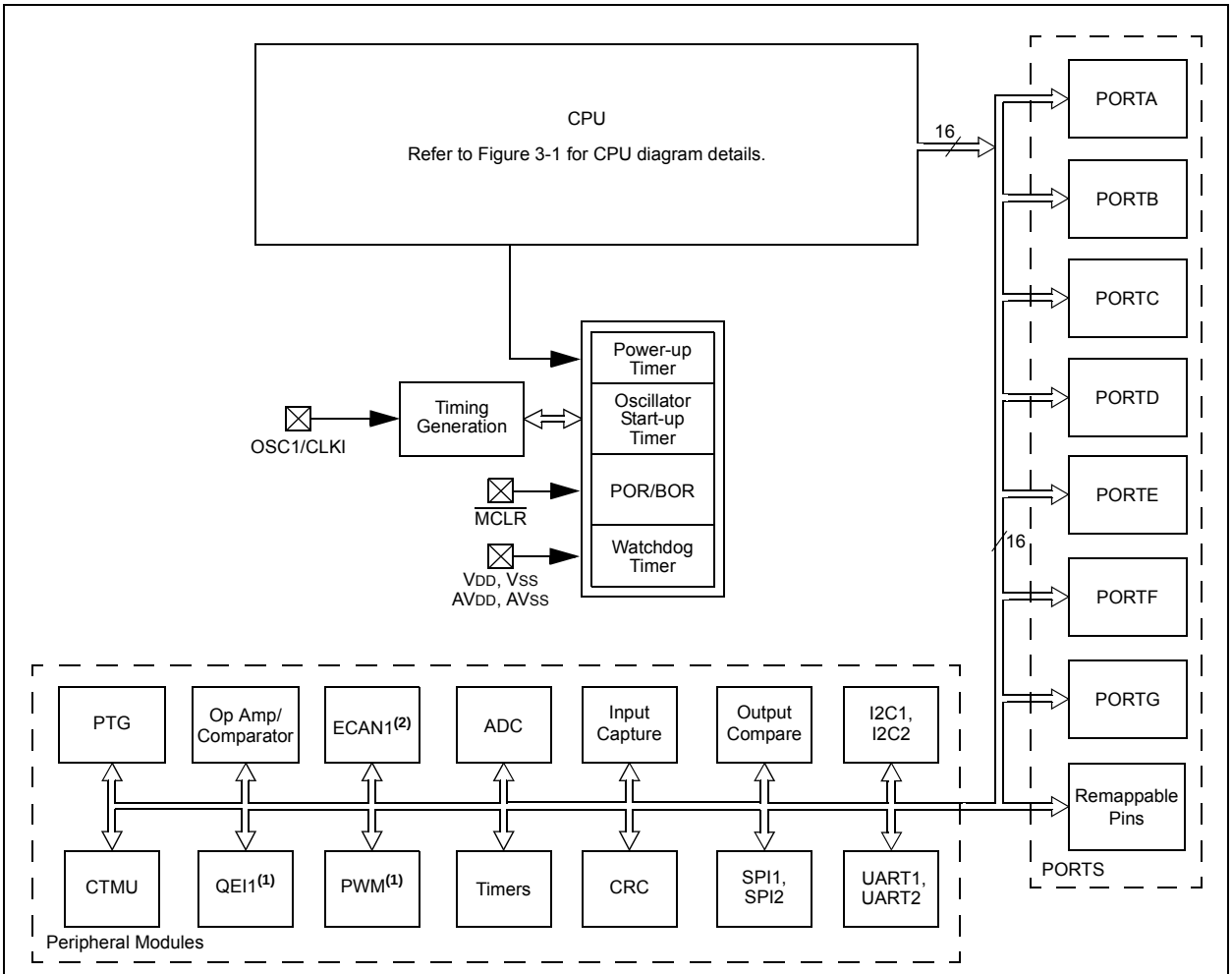
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM**




**Note 1:** This feature or peripheral is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**2:** This feature or peripheral is only available on dsPIC33EPXXXGP/MC50X devices.

**TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | — | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | — | — | — | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | — | — | — | — | — | — | — | — | — | IC4IF | IC3IF | DMA3IF | — | — | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | — | — | — | — | QEI1IF | PSEMIF | — | — | — | — | — | — | MI2C2IF | SI2C2IF | — | 0000 |
| IFS4 | 0808 | — | — | CTMUIF | — | — | — | — | — | — | — | — | — | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS5 | 080A | PWM2IF | PWM1IF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IF | 0000 |
| IFS8 | 0810 | JTAGIF | ICDIF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS9 | 0812 | — | — | — | — | — | — | — | — | — | PTG3IF | PTG2IF | PTG1IF | PTG0IF | PTGWDTIF | PTGSTEPIF | — | 0000 |
| IEC0 | 0820 | — | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | — | — | — | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | — | — | — | — | — | — | — | — | — | IC4IE | IC3IE | DMA3IE | — | — | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | — | — | — | — | QEI1IE | PSEMIE | — | — | — | — | — | — | MI2C2IE | SI2C2IE | — | 0000 |
| IEC4 | 0828 | — | — | CTMUIE | — | — | — | — | — | — | — | — | — | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC5 | 082A | PWM2IE | PWM1IE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC6 | 082C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IE | 0000 |
| IEC8 | 0830 | JTAGIE | ICDIE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC9 | 0832 | — | — | — | — | — | — | — | — | — | PTG3IE | PTG2IE | PTG1IE | PTG0IE | PTGWDTIE | PTGSTEPIE | — | 0000 |
| IPC0 | 0840 | — | T1IP<2:0> | | | — | OC1IP<2:0> | | | — | IC1IP<2:0> | | | — | INT0IP<2:0> | | | 4444 |
| IPC1 | 0842 | — | T2IP<2:0> | | | — | OC2IP<2:0> | | | — | IC2IP<2:0> | | | — | DMA0IP<2:0> | | | 4444 |
| IPC2 | 0844 | — | U1RXIP<2:0> | | | — | SPI1IP<2:0> | | | — | SPI1EIP<2:0> | | | — | T3IP<2:0> | | | 4444 |
| IPC3 | 0846 | — | — | — | — | — | DMA1IP<2:0> | | | — | AD1IP<2:0> | | | — | U1TXIP<2:0> | | | 0444 |
| IPC4 | 0848 | — | CNIP<2:0> | | | — | CMIP<2:0> | | | — | MI2C1IP<2:0> | | | — | SI2C1IP<2:0> | | | 4444 |
| IPC5 | 084A | — | — | — | — | — | — | — | — | — | — | — | — | — | INT1IP<2:0> | | | 0004 |
| IPC6 | 084C | — | T4IP<2:0> | | | — | OC4IP<2:0> | | | — | OC3IP<2:0> | | | — | DMA2IP<2:0> | | | 4444 |
| IPC7 | 084E | — | U2TXIP<2:0> | | | — | U2RXIP<2:0> | | | — | INT2IP<2:0> | | | — | T5IP<2:0> | | | 4444 |
| IPC8 | 0850 | — | — | — | — | — | — | — | — | — | SPI2IP<2:0> | | | — | SPI2EIP<2:0> | | | 0044 |
| IPC9 | 0852 | — | — | — | — | — | IC4IP<2:0> | | | — | IC3IP<2:0> | | | — | DMA3IP<2:0> | | | 0444 |
| IPC12 | 0858 | — | — | — | — | — | MI2C2IP<2:0> | | | — | SI2C2IP<2:0> | | | — | — | — | — | 0440 |
| IPC14 | 085C | — | — | — | — | — | QEI1IP<2:0> | | | — | PSEMIP<2:0> | | | — | — | — | — | 0440 |
| IPC16 | 0860 | — | CRCIP<2:0> | | | — | U2EIP<2:0> | | | — | U1EIP<2:0> | | | — | — | — | — | 4440 |
| IPC19 | 0866 | — | — | — | — | — | — | — | — | — | CTMUIP<2:0> | | | — | — | — | — | 0040 |
| IPC23 | 086E | — | PWM2IP<2:0> | | | — | PWM1IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC24 | 0870 | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IP<2:0> | | | 4004 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | — | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | — | — | — | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | — | — | — | — | — | — | — | — | — | IC4IF | IC3IF | DMA3IF | C1IF | C1RXIF | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | — | — | — | — | — | — | — | — | — | — | — | — | MI2C2IF | SI2C2IF | — | 0000 |
| IFS4 | 0808 | — | — | CTMUIF | — | — | — | — | — | — | C1TXIF | — | — | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IF | 0000 |
| IFS8 | 0810 | JTAGIF | ICDIF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS9 | 0812 | — | — | — | — | — | — | — | — | — | PTG3IF | PTG2IF | PTG1IF | PTG0IF | PTGWDTIF | PTGSTEPIF | — | 0000 |
| IEC0 | 0820 | — | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | — | — | — | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | — | — | — | — | — | — | — | — | — | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | — | — | — | — | — | — | — | — | — | — | — | — | MI2C2IE | SI2C2IE | — | 0000 |
| IEC4 | 0828 | — | — | CTMUIE | — | — | — | — | — | — | C1TXIE | — | — | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC8 | 0830 | JTAGIE | ICDIE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC9 | 0832 | — | — | — | — | — | — | — | — | — | PTG3IE | PTG2IE | PTG1IE | PTG0IE | PTGWDTIE | PTGSTEPIE | — | 0000 |
| IPC0 | 0840 | — | T1IP<2:0> | | | — | OC1IP<2:0> | | | — | IC1IP<2:0> | | | — | INT0IP<2:0> | | | 4444 |
| IPC1 | 0842 | — | T2IP<2:0> | | | — | OC2IP<2:0> | | | — | IC2IP<2:0> | | | — | DMA0IP<2:0> | | | 4444 |
| IPC2 | 0844 | — | U1RXIP<2:0> | | | — | SPI1IP<2:0> | | | — | SPI1EIP<2:0> | | | — | T3IP<2:0> | | | 4444 |
| IPC3 | 0846 | — | — | — | — | — | DMA1IP<2:0> | | | — | AD1IP<2:0> | | | — | U1TXIP<2:0> | | | 0444 |
| IPC4 | 0848 | — | CNIP<2:0> | | | — | CMIP<2:0> | | | — | MI2C1IP<2:0> | | | — | SI2C1IP<2:0> | | | 4444 |
| IPC5 | 084A | — | — | — | — | — | — | — | — | — | — | — | — | — | INT1IP<2:0> | | | 0004 |
| IPC6 | 084C | — | T4IP<2:0> | | | — | OC4IP<2:0> | | | — | OC3IP<2:0> | | | — | DMA2IP<2:0> | | | 4444 |
| IPC7 | 084E | — | U2TXIP<2:0> | | | — | U2RXIP<2:0> | | | — | INT2IP<2:0> | | | — | T5IP<2:0> | | | 4444 |
| IPC8 | 0850 | — | C1IP<2:0> | | | — | C1RXIP<2:0> | | | — | SPI2IP<2:0> | | | — | SPI2EIP<2:0> | | | 4444 |
| IPC9 | 0852 | — | — | — | — | — | IC4IP<2:0> | | | — | IC3IP<2:0> | | | — | DMA3IP<2:0> | | | 0444 |
| IPC11 | 0856 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IPC12 | 0858 | — | — | — | — | — | MI2C2IP<2:0> | | | — | SI2C2IP<2:0> | | | — | — | — | — | 0440 |
| IPC16 | 0860 | — | CRCIP<2:0> | | | — | U2EIP<2:0> | | | — | U1EIP<2:0> | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | — | — | — | — | C1TXIP<2:0> | | | — | — | — | — | — | — | — | — | 0400 |
| IPC19 | 0866 | — | — | — | — | — | — | — | — | — | CTMUIP<2:0> | | | — | — | — | — | 0040 |
| IPC35 | 0886 | — | JTAGIP<2:0> | | | — | ICDIP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC36 | 0888 | — | PTG0IP<2:0> | | | — | PTGWDTIP<2:0> | | | — | PTGSTEPIP<2:0> | | | — | — | — | — | 4440 |
| IPC37 | 088A | — | — | — | — | — | PTG3IP<2:0> | | | — | PTG2IP<2:0> | | | — | PTG1IP<2:0> | | | 0444 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-11: PTG REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PTGCST | 0AC0 | PTGEN | — | PTGSIDL | PTGTOGL | — | PTGSWT | PTGSSEN | PTGIVIS | PTGSTRT | PTGWTO | — | — | — | — | PTGITM<1:0> | | 0000 |
| PTGCON | 0AC2 | PTGCLK<2:0> | | | PTGDIV<4:0> | | | | | PTGPWD<3:0> | | | | — | PTGWDT<2:0> | | | 0000 |
| PTGBTE | 0AC4 | ADCTS<4:1> | | | | IC4TSS | IC3TSS | IC2TSS | IC1TSS | OC4CS | OC3CS | OC2CS | OC1CS | OC4TSS | OC3TSS | OC2TSS | OC1TSS | 0000 |
| PTGHOLD | 0AC6 | PTGHOLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGT0LIM | 0AC8 | PTGT0LIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGT1LIM | 0ACA | PTGT1LIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGSDLIM | 0ACC | PTGSDLIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGC0LIM | 0ACE | PTGC0LIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGC1LIM | 0AD0 | PTGC1LIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGADJ | 0AD2 | PTGADJ<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGL0 | 0AD4 | PTGL0<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGQPTR | 0AD6 | — | — | — | — | — | — | — | — | — | — | — | PTGQPTR<4:0> | | | | | 0000 |
| PTGQUE0 | 0AD8 | STEP1<7:0> | | | | | | | | STEP0<7:0> | | | | | | | | 0000 |
| PTGQUE1 | 0ADA | STEP3<7:0> | | | | | | | | STEP2<7:0> | | | | | | | | 0000 |
| PTGQUE2 | 0ADC | STEP5<7:0> | | | | | | | | STEP4<7:0> | | | | | | | | 0000 |
| PTGQUE3 | 0ADE | STEP7<7:0> | | | | | | | | STEP6<7:0> | | | | | | | | 0000 |
| PTGQUE4 | 0AE0 | STEP9<7:0> | | | | | | | | STEP8<7:0> | | | | | | | | 0000 |
| PTGQUE5 | 0AE2 | STEP11<7:0> | | | | | | | | STEP10<7:0> | | | | | | | | 0000 |
| PTGQUE6 | 0AE4 | STEP13<7:0> | | | | | | | | STEP12<7:0> | | | | | | | | 0000 |
| PTGQUE7 | 0AE6 | STEP15<7:0> | | | | | | | | STEP14<7:0> | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-45: DMAC REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DMA0CON | 0B00 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA0REQ | 0B02 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA0STAL | 0B04 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA0STAH | 0B06 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA0STBL | 0B08 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA0STBH | 0B0A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA0PAD | 0B0C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA0CNT | 0B0E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA1CON | 0B10 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA1REQ | 0B12 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA1STAL | 0B14 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA1STAH | 0B16 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA1STBL | 0B18 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA1STBH | 0B1A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA1PAD | 0B1C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA1CNT | 0B1E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA2CON | 0B20 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA2REQ | 0B22 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA2STAL | 0B24 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA2STAH | 0B26 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA2STBL | 0B28 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA2STBH | 0B2A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA2PAD | 0B2C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA2CNT | 0B2E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA3CON | 0B30 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA3REQ | 0B32 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA3STAL | 0B34 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA3STAH | 0B36 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA3STBL | 0B38 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA3STBH | 0B3A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA3PAD | 0B3C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA3CNT | 0B3E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMAPWC | 0BF0 | — | — | — | — | — | — | — | — | — | — | — | — | PWCOL3 | PWCOL2 | PWCOL1 | PWCOL0 | 0000 |
| DMARQC | 0BF2 | — | — | — | — | — | — | — | — | — | — | — | — | RQCOL3 | RQCOL2 | RQCOL1 | RQCOL0 | 0000 |
| DMAPPS | 0BF4 | — | — | — | — | — | — | — | — | — | — | — | — | PPST3 | PPST2 | PPST1 | PPST0 | 0000 |
| DMALCA | 0BF6 | — | — | — | — | — | — | — | — | — | — | — | — | LSTCH<3:0> | | | | 000F |
| DSADRL | 0BF8 | DSADR<15:0> | | | | | | | | | | | | | | | | 0000 |
| DSADRH | 0BFA | — | — | — | — | — | — | — | — | DSADR<23:16> | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-59: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 0E00 | — | — | — | — | — | — | — | — | — | — | — | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 001F |
| PORTA | 0E02 | — | — | — | — | — | — | — | — | — | — | — | RA4 | RA3 | RA2 | RA1 | RA0 | 0000 |
| LATA | 0E04 | — | — | — | — | — | — | — | — | — | — | — | LATA4 | LATA3 | LATA2 | LA1TA1 | LA0TA0 | 0000 |
| ODCA | 0E06 | — | — | — | — | — | — | — | — | — | — | — | ODCA4 | ODCA3 | ODCA2 | ODCA1 | ODCA0 | 0000 |
| CNENA | 0E08 | — | — | — | — | — | — | — | — | — | — | — | CNIEA4 | CNIEA3 | CNIEA2 | CNIEA1 | CNIEA0 | 0000 |
| CNPUA | 0E0A | — | — | — | — | — | — | — | — | — | — | — | CNPUA4 | CNPUA3 | CNPUA2 | CNPUA1 | CNPUA0 | 0000 |
| CNPDA | 0E0C | — | — | — | — | — | — | — | — | — | — | — | CNPDA4 | CNPDA3 | CNPDA2 | CNPDA1 | CNPDA0 | 0000 |
| ANSELA | 0E0E | — | — | — | — | — | — | — | — | — | — | — | ANSA4 | — | — | ANSA1 | ANSA0 | 0013 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-60: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 0E10 | TRISB15 | TRISB14 | TRISB13 | TRISB12 | TRISB11 | TRISB10 | TRISB9 | TRISB8 | TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 | FFFF |
| PORTB | 0E12 | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx |
| LATB | 0E14 | LATB15 | LATB14 | LATB13 | LATB12 | LATB11 | LATB10 | LATB9 | LATB8 | LATB7 | LATB6 | LATB5 | LATB4 | LATB3 | LATB2 | LATB1 | LATB0 | xxxx |
| ODCB | 0E16 | ODCB15 | ODCB14 | ODCB13 | ODCB12 | ODCB11 | ODCB10 | ODCB9 | ODCB8 | ODCB7 | ODCB6 | ODCB5 | ODCB4 | ODCB3 | ODCB2 | ODCB1 | ODCB0 | 0000 |
| CNENB | 0E18 | CNIEB15 | CNIEB14 | CNIEB13 | CNIEB12 | CNIEB11 | CNIEB10 | CNIEB9 | CNIEB8 | CNIEB7 | CNIEB6 | CNIEB5 | CNIEB4 | CNIEB3 | CNIEB2 | CNIEB1 | CNIEB0 | 0000 |
| CNPUB | 0E1A | CNPUB15 | CNPUB14 | CNPUB13 | CNPUB12 | CNPUB11 | CNPUB10 | CNPUB9 | CNPUB8 | CNPUB7 | CNPUB6 | CNPUB5 | CNPUB4 | CNPUB3 | CNPUB2 | CNPUB1 | CNPUB0 | 0000 |
| CNPDB | 0E1C | CNPDB15 | CNPDB14 | CNPDB13 | CNPDB12 | CNPDB11 | CNPDB10 | CNPDB9 | CNPDB8 | CNPDB7 | CNPDB6 | CNPDB5 | CNPDB4 | CNPDB3 | CNPDB2 | CNPDB1 | CNPDB0 | 0000 |
| ANSELB | 0E1E | — | — | — | — | — | — | — | ANSB8 | — | — | — | — | ANSB3 | ANSB2 | ANSB1 | ANSB0 | 010F |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

### 4.5.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions, which apply to dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and the DSP accumulator class of instructions, which apply to the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

| | |
|---|---|
| **Note:** | For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one). |

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

| | |
|---|---|
| **Note:** | Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes. |

### 4.5.4 MAC INSTRUCTIONS (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X DEVICES ONLY)

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The Two-Source Operand Prefetch registers must be members of the set: {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

| | |
|---|---|
| **Note:** | Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space). |

In summary, the following addressing modes are supported by the MAC class of instructions:

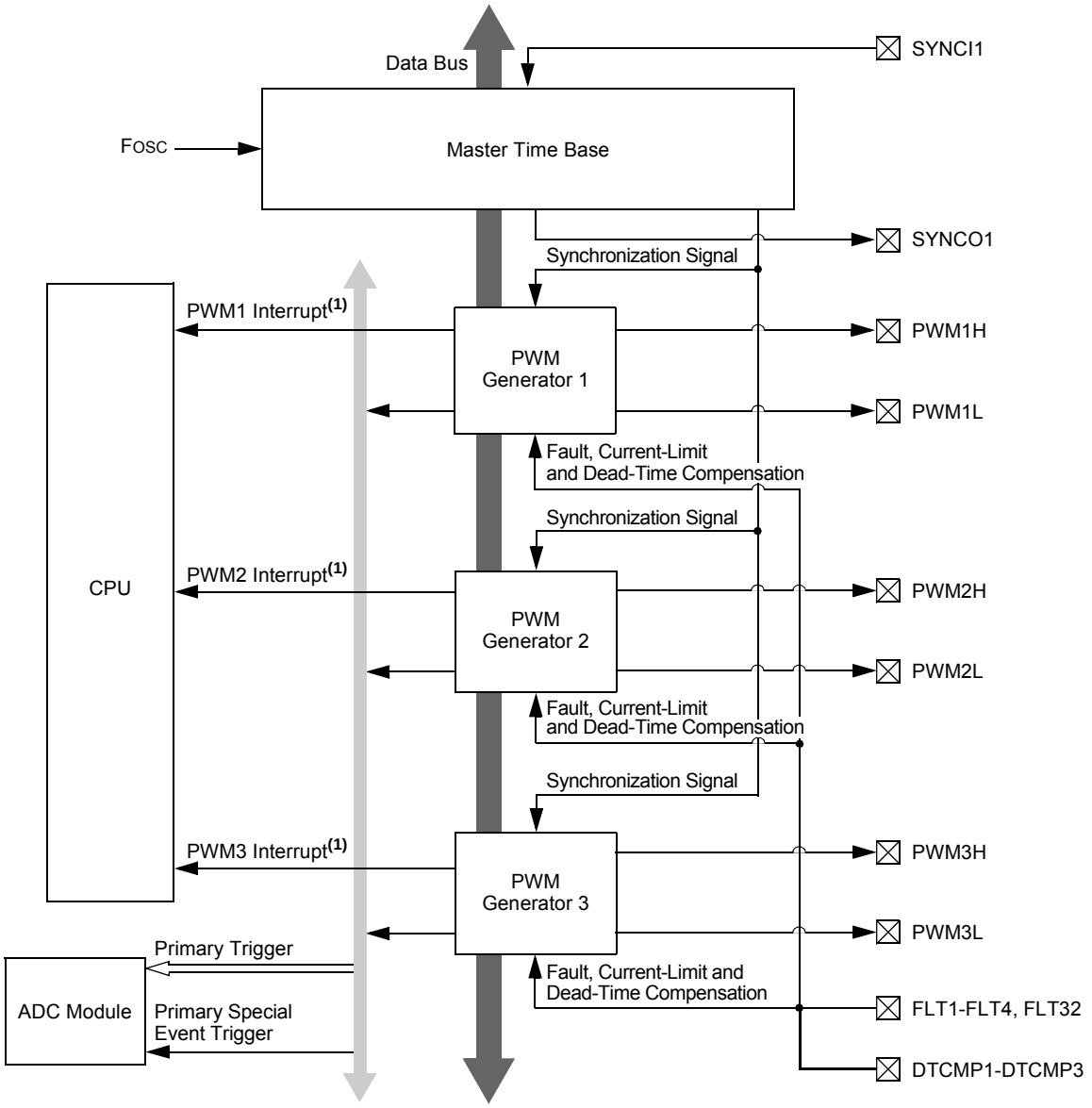
- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

### 4.5.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

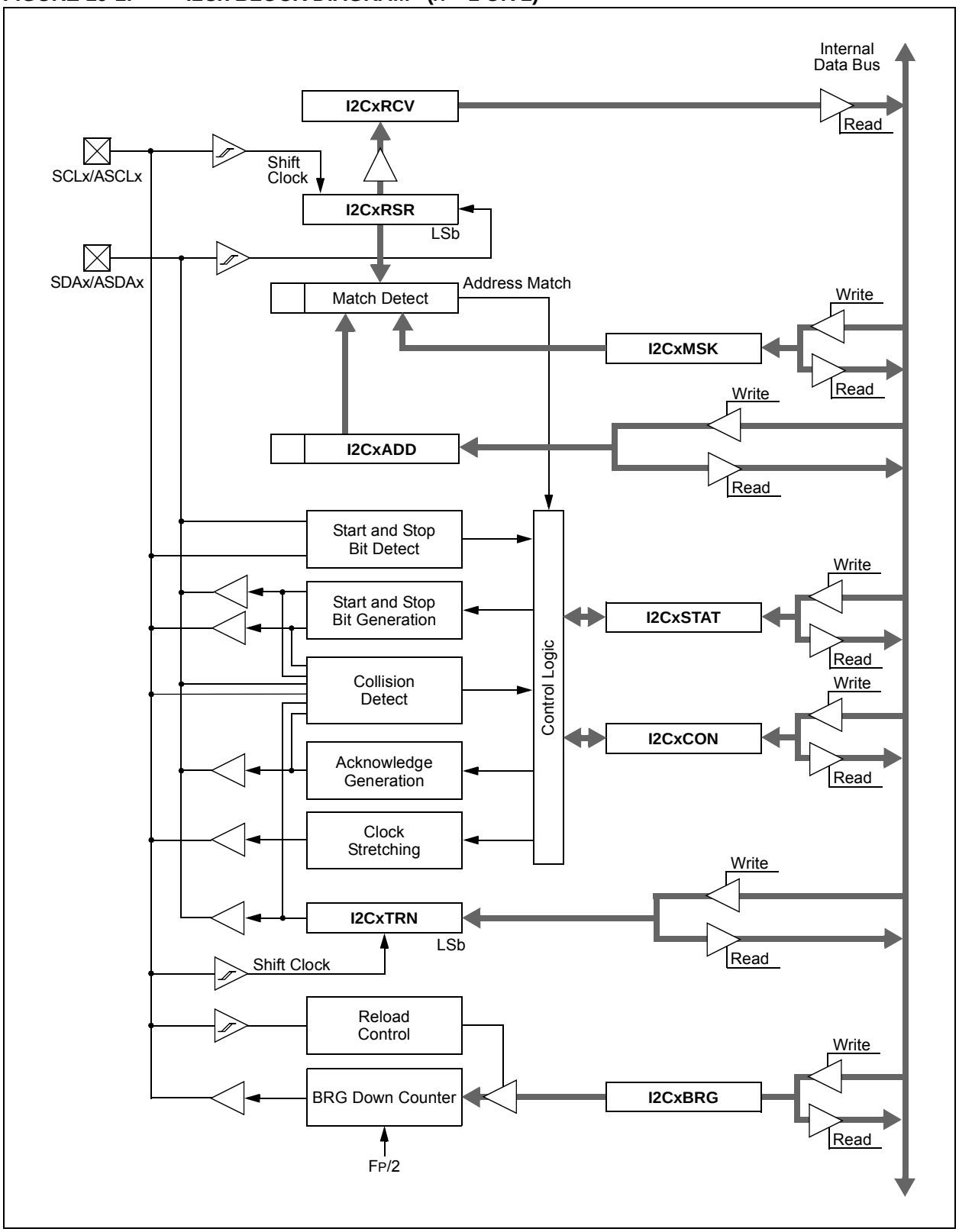
**NOTES:**

**FIGURE 16-1: HIGH-SPEED PWMx MODULE ARCHITECTURAL OVERVIEW**




**Note 1:** The PWM interrupts are generated by logically ORing the FLTSTAT, CLSTAT and TRGSTAT status bits for the given PWM generator. Refer to the "*dsPIC33/PIC24 Family Reference Manual*", **"High-Speed PWM"** (DS70645) for more information.

**FIGURE 19-1: I2Cx BLOCK DIAGRAM (x = 1 OR 2)**



**REGISTER 20-1: UxMODE: UARTx MODE REGISTER (CONTINUED)**

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion
0 = Baud rate measurement is disabled or completed

bit 4 **URXINV:** UARTx Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

**Note 1:** Refer to the **"UART"** (DS70582) section in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for receive or transmit operation.
**2:** This feature is only available for the 16x BRG mode (BRGH = 0).
**3:** This feature is only available on 44-pin and 64-pin devices.
**4:** This feature is only available on 64-pin devices.

**REGISTER 21-26: CxTRmnCON: ECANx TX/RX BUFFER mn CONTROL REGISTER (m = 0,2,4,6; n = 1,3,5,7)**

| R/W-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TXENn | TXABTn | TXLARBn | TXERRn | TXREQn | RTRENn | TXnPRI1 | TXnPRI0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TXENm | TXABTm(1) | TXLARBm(1) | TXERRm(1) | TXREQm | RTRENm | TXmPRI1 | TXmPRI0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 See Definition for bits<7:0>, Controls Buffer n

bit 7 **TXENm:** TX/RX Buffer Selection bit
1 = Buffer TRBn is a transmit buffer
0 = Buffer TRBn is a receive buffer

bit 6 **TXABTm:** Message Aborted bit(1)
1 = Message was aborted
0 = Message completed transmission successfully

bit 5 **TXLARBm:** Message Lost Arbitration bit(1)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERRm:** Error Detected During Transmission bit(1)
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQm:** Message Send Request bit
1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent
0 = Clearing the bit to '0' while set requests a message abort

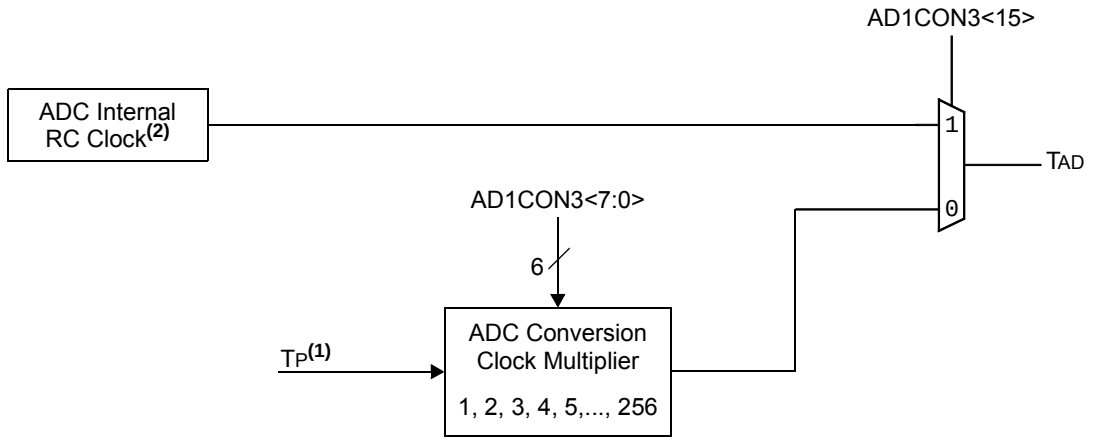
bit 2 **RTRENm:** Auto-Remote Transmit Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXmPRI<1:0>:** Message Transmission Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

**Note 1:** This bit is cleared when TXREQ is set.

**Note:** The buffers, SID, EID, DLC, Data Field, and Receive Status registers are located in DMA RAM.

**FIGURE 23-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM**




**Note 1:** TP = 1/FP.

**2:** See the ADC electrical specifications in **Section 30.0 "Electrical Characteristics"** for the exact RC clock value.

**REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2 (CONTINUED)**

bit 1 **BUFM:** Buffer Fill Mode Select bit

1 = Starts the buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on next interrupt

0 = Always starts filling the buffer from the start address.

bit 0 **ALTS:** Alternate Input Sample Mode Select bit

1 = Uses channel input selects for Sample MUXA on first sample and Sample MUXB on next sample

0 = Always uses channel input selects for Sample MUXA

## 30.2 AC Characteristics and Timing Parameters

This section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters.

**TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC**

| | |
|---|---|
| **AC CHARACTERISTICS** | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended<br>Operating voltage VDD range as described in **Section 30.1 "DC Characteristics"**. |

**FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

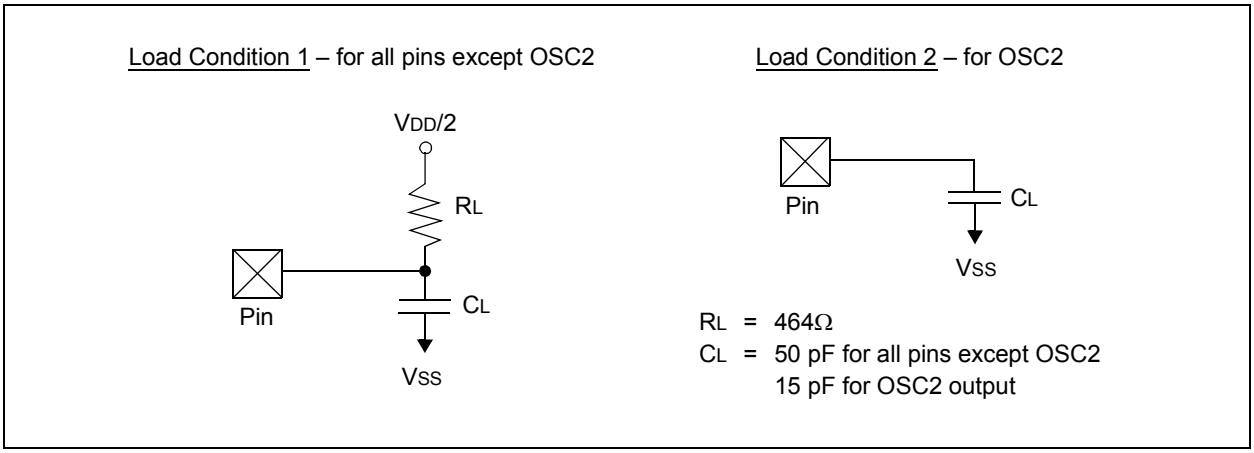



**TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS**

| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| DO50 | COSCO | OSC2 Pin | — | — | 15 | pF | In XT and HS modes, when external clock is used to drive OSC1 |
| DO56 | CIO | All I/O Pins and OSC2 | — | — | 50 | pF | EC mode |
| DO58 | CB | SCLx, SDAx | — | — | 400 | pF | In $I^2C$™ mode |

**FIGURE 30-12: QEA/QEB INPUT CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

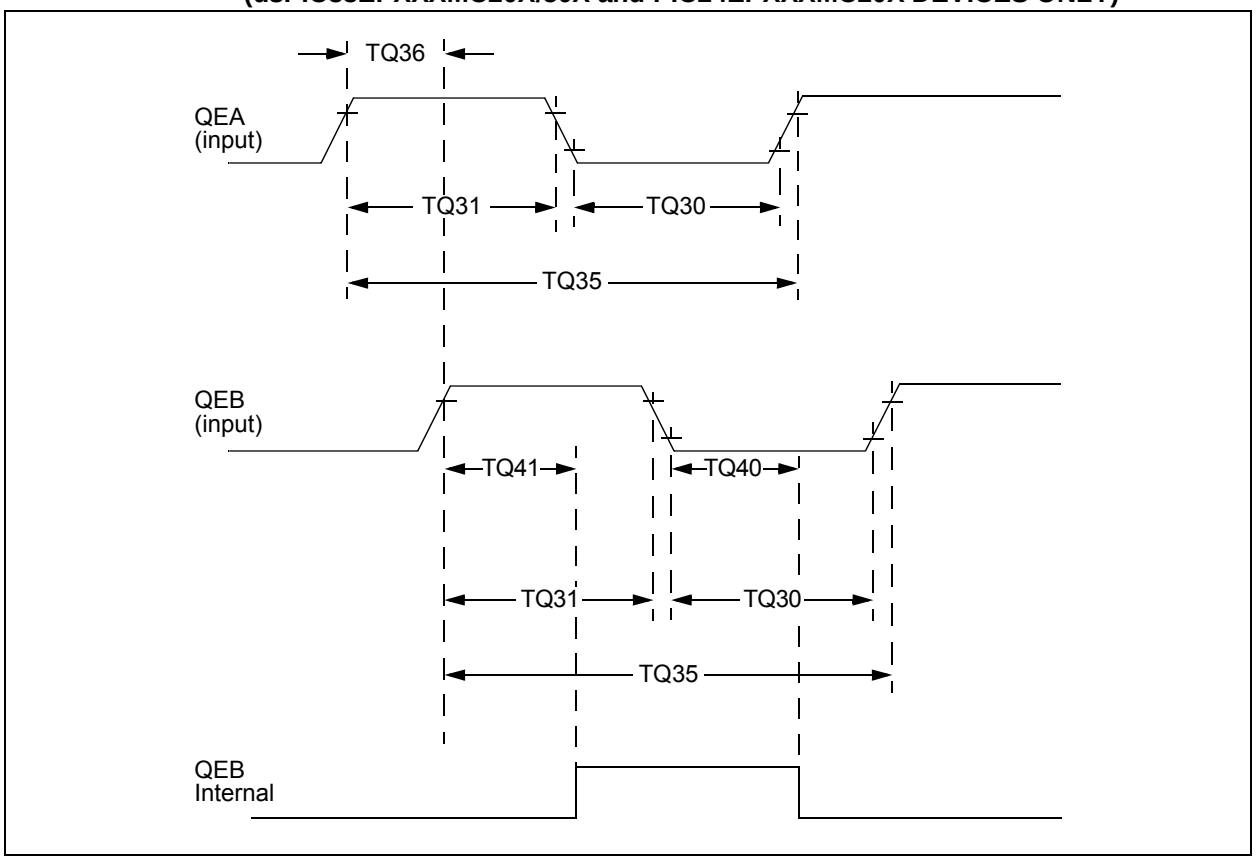



**TABLE 30-31: QUADRATURE DECODER TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| TQ30 | TQUL | Quadrature Input Low Time | 6 TCY | — | ns | |
| TQ31 | TQUH | Quadrature Input High Time | 6 TCY | — | ns | |
| TQ35 | TQUIN | Quadrature Input Period | 12 TCY | — | ns | |
| TQ36 | TQUP | Quadrature Phase Period | 3 TCY | — | ns | |
| TQ40 | TQUFL | Filter Time to Recognize Low, with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)** |
| TQ41 | TQUFH | Filter Time to Recognize High, with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)** |

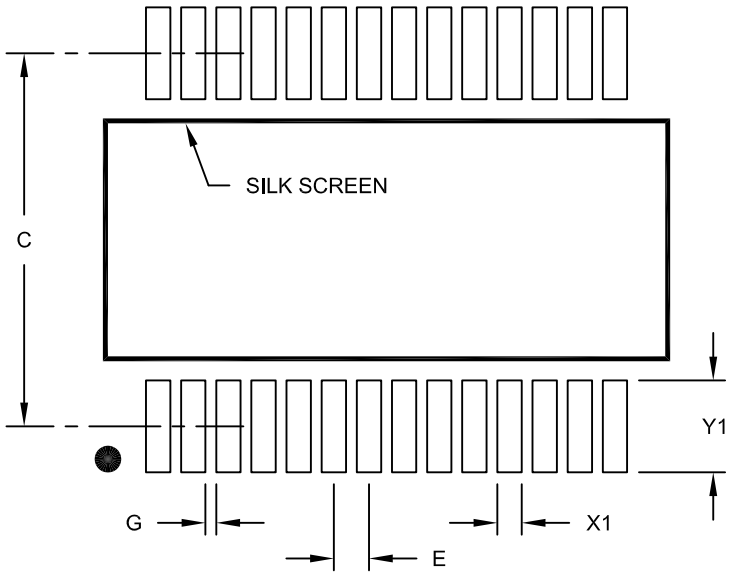
**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** N = Index Channel Digital Filter Clock Divide Select bits. Refer to **"Quadrature Encoder Interface (QEI)"** (DS70601) in the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip web site for the latest family reference manual sections.

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 7.20 | |
| Contact Pad Width (X28) | X1 | | | 0.45 |
| Contact Pad Length (X28) | Y1 | | | 1.75 |
| Distance Between Pads | G | 0.20 | | |

Notes:

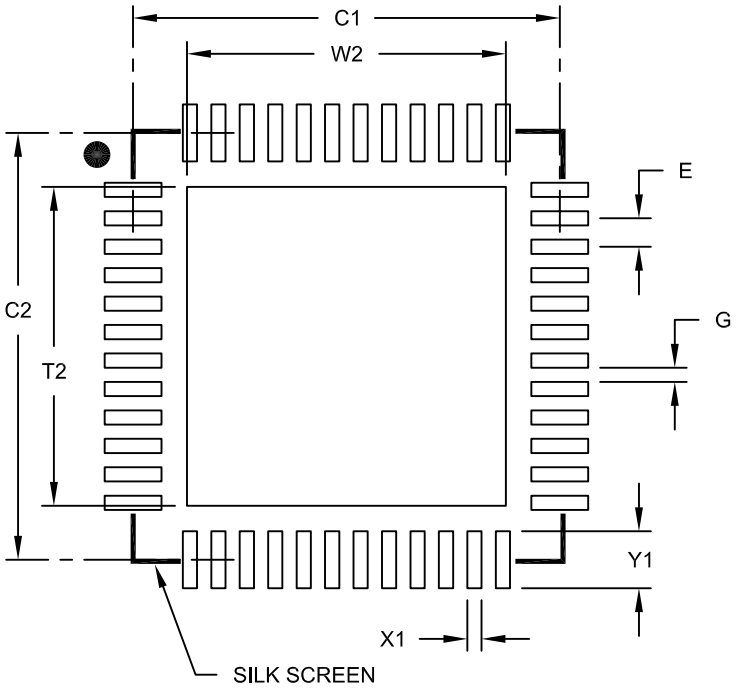
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]
With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.40 BSC | |
| Optional Center Pad Width | W2 | | | 4.45 |
| Optional Center Pad Length | T2 | | | 4.45 |
| Contact Pad Spacing | C1 | | 6.00 | |
| Contact Pad Spacing | C2 | | 6.00 | |
| Contact Pad Width (X28) | X1 | | | 0.20 |
| Contact Pad Length (X28) | Y1 | | | 0.80 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A

# INDEX

## A



## B