

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XEI

Obsolete
dsPIC
16-Bit
60 MIPs
I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
35
32KB (10.7K x 24)
FLASH
-
2K x 16
3V ~ 3.6V
A/D 9x10b/12b
Internal
-40°C ~ 125°C (TA)
Surface Mount
44-TQFP
44-TQFP (10x10)
https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc204t-e-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



Pin Diagrams (Continued)



TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC23	086E	—	F	PWM2IP<2:	0>	_	F	WM1IP<2:	:0>	_	_	—	_	_		_		4400
IPC24	0870	—	_	_	—	_	—	—	—	_	—	—		_	F	PWM3IP<2:0>		0004
IPC35	0886	—		JTAGIP<2:0)>	_		ICDIP<2:0	>	_	—	—		_	-	—		4400
IPC36	0888	—		PTG0IP<2:0)>	_	PT	GWDTIP<	2:0>	—	P	TGSTEPIP<2	:0>	_		_		4440
IPC37	088A	—	—		—	_	F	PTG3IP<2:	0>	—		PTG2IP<2:0>	•	_	-	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL		0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	_	—	—	—	_	—	—		_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—		—	_	—	—	—	_	—	DAE	DOOVR	_		_		0000
INTCON4	08C6	_	_		_	_	_	_	_	_	_	_	_	_	_	_	SGHT	0000
INTTREG	08C8	_	_		_	— ILR<3:0>						VECNU	JM<7:0>				0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TADLL 4-2		LUANT	IL GIGI				ICINE	1<02) -	· • • • • .	I I OK US			IC/GFJ					
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	_	—	CSIDL	ABAT	CANCKS	R	EQOP<2:0)>	OPN	NODE<2:0	>	_	CANCAP	_	_	WIN	0480
C1CTRL2	0402	_	—	_	—	—	—	_	_	_	—	_		D	NCNT<4:0	>		0000
C1VEC	0404	_	_	_		F	ILHIT<4:0>			_				ICODE<6:0	>			0040
C1FCTRL	0406	[DMABS<2:0	>	—	—		—	_	_	—	—			FSA<4:0>			0000
C1FIFO	0408	_	_			FBP<	5:0>			_	_			FNRB	<5:0>			0000
C1INTF	040A	_	_	ТХВО	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	_	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	_	_	_	—	—	_	_	_	IVRIE	WAKIE	ERRIE	_	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E				TERRCN	T<7:0>							RERRCM	NT<7:0>				0000
C1CFG1	0410	_	_	_	—	—	_	_	_	SJW<	1:0>			BRP	<5:0>			0000
C1CFG2	0412	_	WAKFIL	_	—	—	SI	EG2PH<2:(0>	SEG2PHTS	SAM	S	EG1PH<2	::0>	P	RSEG<2:0	>	0000
C1FEN1	0414	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C1FMSKSEL1	0418	F7MS	K<1:0>	F6MS	K<1:0>	F5MS	K<1:0>	F4MS	K<1:0>	F3MSK	<1:0>	F2MS	K<1:0>	F1MSł	<<1:0>	F0MS	<<1:0>	0000
C1FMSKSEL2	041A	F15MS	SK<1:0>	F14MS	K<1:0>	F13MS	SK<1:0>	F12MS	SK<1:0>	F11MSK	<1:0>	F10MS	K<1:0>	F9MSł	<<1:0>	F8MS	< <1:0>	0000

TABLE 4-21: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 0 OR 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 0 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400- 041E							S	ee definition	when WIN	= x							
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C1RXOVF2	042A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	OVF26 RXOVF25 RXOVF24 RXOVF23 RXOVF22 RXOVF21 RXOVF20 RXOVF19 RXOVF18 RXOVF17					RXOVF16	0000				
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PF	RI<1:0>	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PF	RI<1:0>	0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PF	RI<1:0>	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PF	RI<1:0>	0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PF	RI<1:0>	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PF	RI<1:0>	0000
C1TR67CON	0436	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	REQ7 RTREN7 TX7PRI<1:0> TXEN6 TXABAT6 TXLARB6 TXERR6 TXREQ6 RTREN6 TX6PRI<1:0> xx							xxxx				
C1RXD	0440							E	CAN1 Rece	eive Data Wo	ord							xxxx
C1TXD	0442		ECAN1 Transmit Data Word xxxx															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

IADLE 4-2	:s: ⊏	CANTI	REGISI			IN WIIN		<li<u></li<u>	$y = \perp r c$		SSELV		POUX D	EVICES	UNLT	CONTI	NUED)	
File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1RXF11EID	046E				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF12SID	0470				SID<	:10:3>					SID<2:0> — EXIDE — EID<17:16>						7:16>	xxxx
C1RXF12EID	0472		EID<15:8>										EID<	7:0>				xxxx
C1RXF13SID	0474		SID<10:3>								SID<2:0>		_	EXIDE	_	EID<1	7:16>	xxxx
C1RXF13EID	0476				EID<	<15:8>				EID<7:0>							xxxx	
C1RXF14SID	0478				SID<	<10:3>					SID<2:0>		_	EXIDE	_	EID<1	7:16>	xxxx
C1RXF14EID	047A		EID<15:8>							EID<7:0>							xxxx	
C1RXF15SID	047C		SID<10:3>							SID<2:0> — EXIDE — EID<17:"						7:16>	xxxx	
C1RXF15EID	047E		EID<15:8>										EID<	7:0>				xxxx

ECANI DECISTED MAD WHEN WIN (CICTDI 1 -0.) 1 EOD doDIC22EDXXXMC/CDE0X DEVICES ONLY (CONTINUED) 1 22.

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
 - In Word mode, this instruction maps the lower word of the Program Space location (P<15:0>) to a data address (D<15:0>)

- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.
- TBLRDH (Table Read High):
 - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. The 'phantom' byte (D<15:8>) is always '0'.
 - In Byte mode, this instruction maps the upper or lower byte of the program word to D<7:0> of the data address in the TBLRDL instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.



FIGURE 4-23: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS

REGISTER 8-3: DMAXSTAH: DMA CHANNEL X START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—		—	—	—	—	—	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STA<	23:16>			
bit 7							bit 0
Legend:							
R = Readable b	it	W = Writable bi	t	U = Unimplei	mented bit read	d as '0'	

•••			-		
-n =	= Value at POR	'1' = Bit is set	'0' =	Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 STA<23:16>: Primary Start Address bits (source or destination)

REGISTER 8-4: DMAXSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STA	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STA	<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at P	' OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unki	nown

bit 15-0 STA<15:0>: Primary Start Address bits (source or destination)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_		—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
			DMA0MD ⁽¹⁾				
_	_	_	DMA1MD ⁽¹⁾	PTGMD	_	_	_
			DMA2MD ⁽¹⁾	1 TOME			
			DMA3MD ⁽¹⁾				
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown
bit 15-5	Unimplement	ted: Read as '	D'				
bit 4	DMA0MD: DN	/A0 Module Di	sable bit ⁽¹⁾				
	1 = DMA0 mo	dule is disable	d				
	0 = DMA0 mo	dule is enable	d 				
	DMA1MD: DN	/A1 Module Di	sable bit(")				
	1 = DMA1 mo 0 = DMA1 mo	dule is disable	d d				
			sable bit(1)				
	1 = DMA2 mo	dule is disable	d				
	0 = DMA2 mo	dule is enable	d				
	DMA3MD: DN	/A3 Module Di	sable bit ⁽¹⁾				
	1 = DMA3 mo	dule is disable	d				
	0 = DMA3 mo	dule is enable	b				
bit 3	PTGMD: PTG	Module Disab	le bit				
	1 = PTG mod	ule is disabled					
	$0 = PIG \mod 1$	uie is enabled	-1				
DIT 2-0	Unimplement	tea: Read as '	J.				
Note 1: Th	nis single bit ena	ables and disat	oles all four DM	A channels.			

REGISTER 10-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, "RPn" or "RPIn", in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs. In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C^{TM} and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and nonremappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheralselectable pin is handled in two different ways, depending on whether an input or output is being mapped.

REGISTER 11-26: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP118	8R<5:0>		
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—		_	_	_	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	RP118R<5:0>: Peripheral Output Function is Assigned to RP118 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-0 Unimplemented: Read as '0'

REGISTER 11-27: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—		RP120R<5:0>					
bit 7							bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 Unimplemented: Read as '0'

bit 5-0 **RP120R<5:0>:** Peripheral Output Function is Assigned to RP120 Output Pin bits (see Table 11-3 for peripheral function numbers)

12.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

12.1.1 KEY RESOURCES

- "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

NOTES:

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	TRGDIV<3:0>				—	—	—
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			TRGSTF	RT<5:0>(1)		
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own
bit 15-12	TRGDIV<3:0)>: Trigger # Ou	tput Divider b	vits			
	1111 = Trigg	er output for ev	ery 16th trigg	er event			
	1110 = Trigg	er output for ev	ery 15th trigg	er event			
	1101 = Trigg	er output for ev	ery 14th trigg	er event			
	1100 = Trigg	er output for ev	ery 13th trigg	er event			
	1011 = Irigg	er output for ev	ery 12th trigg	er event			
	1010 = Trigg	per output for ev	ery 11th trigge	er event			
	1001 - Trigg	er output for ev	ery 9th triage	r event			
	0111 = Trigg	er output for ev	erv 8th triage	r event			
	0110 = Trigg	er output for ev	erv 7th triage	r event			
	0101 = Trigg	er output for ev	ery 6th trigge	r event			
	0100 = Trigg	, jer output for ev	ery 5th trigge	r event			
	0011 = Trigg	er output for ev	ery 4th trigge	r event			
	0010 = Trigg	er output for ev	ery 3rd trigge	r event			
	0001 = Trigg	er output for ev	ery 2nd trigge	erevent			
	0000 = Trigg	ger output for ev	ery trigger ev	ent			
bit 11-6	Unimplemer	nted: Read as '	0'				
bit 5-0	TRGSTRT<5	5:0>: Trigger Po	stscaler Start	Enable Select	bits ⁽¹⁾		
	111111 = W	aits 63 PWM cy	cles before g	enerating the fir	rst trigger event	after the modu	le is enabled
	•						
	•						
	•						
	000010 = W	aits 2 PWM cyc	les before ge	nerating the firs	t trigger event a	after the module	e is enabled
	000001 = W	aits 1 PWM cyc	le before gen	erating the first	trigger event a	fter the module	is enabled
	000000 = W	aits 0 PWM cyc	les before ge	nerating the firs	t trigger event a	after the module	e is enabled

REGISTER 16-12: TRGCONx: PWMx TRIGGER CONTROL REGISTER



R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			TRGC	/IP<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			TRGC	MP<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

REGISTER 16-14: TRIGX: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

bit 15-0 TRGCMP<15:0>: Trigger Control Value bits

When the primary PWMx functions in local time base, this register contains the compare values that can trigger the ADC module.

REGISTER 17-19: INT1HLDH: INTERVAL 1 TIMER HOLD HIGH WORD REGIS	TER
---	-----

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTHL	D<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTHL	D<23:16>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	nented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 INTHLD<31:16>: Hold Register for Reading and Writing INT1TMRH bits

REGISTER 17-20: INT1HLDL: INTERVAL 1 TIMER HOLD LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTHL	D<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTH	_D<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable b	pit	U = Unimplen	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 INTHLD<15:0>: Hold Register for Reading and Writing INT1TMRL bits

19.0 INTER-INTEGRATED CIRCUIT[™] (I²C[™])

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Inter-Integrated Circuit™ (I²C™)" (DS70330) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.
 - 3: There are minimum bit rates of approximately FCY/512. As a result, high processor speeds may not support 100 Kbit/second operation. See timing specifications, IM10 and IM11, and the "Baud Rate Generator" in the "dsPIC33/PIC24 Family Reference Manual".

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X family of devices contains two Inter-Integrated Circuit (I²C) modules: I2C1 and I2C2.

The l^2C module provides complete hardware support for both Slave and Multi-Master modes of the l^2C serial communication standard, with a 16-bit interface.

The I^2C module has a 2-pin interface:

- · The SCLx pin is clock
- The SDAx pin is data

The I²C module offers the following key features:

- I²C interface supporting both Master and Slave modes of operation
- I²C Slave mode supports 7 and 10-bit addressing
- I²C Master mode supports 7 and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation, detects bus collision and arbitrates accordingly
- Intelligent Platform Management Interface (IPMI)
 support
- System Management Bus (SMBus) support

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN ⁽¹⁾	UTXBF	TRMT
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0
Legend:		HC = Hardwar	e Clearable bit	C = Clearable	e bit		
R = Readable	bit	W = Writable b	bit	U = Unimpler	mented bit, read	d as '0'	

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 UTXINV: UARTx Transmit Polarity Inversion bit
 - $\frac{\text{If IREN = 0:}}{1 = \text{UxTX Idle state is '0'}}$
 - 0 = UxTX Idle state is '1'
 - If IREN = 1:
 - 1 = IrDA encoded, UxTX Idle state is '1'
 - 0 = IrDA encoded, UxTX Idle state is '0'
- bit 12 Unimplemented: Read as '0'
- bit 11 UTXBRK: UARTx Transmit Break bit
 - 1 = Sends Sync Break on next transmission Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 - 0 = Sync Break transmission is disabled or completed
- bit 10 UTXEN: UARTx Transmit Enable bit⁽¹⁾ 1 = Transmit is enabled, UxTX pin is controlled by UARTx
 - 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; UxTX pin is controlled by the PORT
- bit 9 UTXBF: UARTx Transmit Buffer Full Status bit (read-only)
 - 1 = Transmit buffer is full
 - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 TRMT: Transmit Shift Register Empty bit (read-only)
 - 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits
 - 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
 - 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
 - 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters
- **Note 1:** Refer to the "**UART**" (DS70582) section in the "*dsPIC33/PIC24 Family Reference Manual*" for information on enabling the UARTx module for transmit operation.

21.2 Modes of Operation

The ECAN module can operate in one of several operation modes selected by the user. These modes include:

- · Initialization mode
- Disable mode
- Normal Operation mode
- · Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

21.3 ECAN Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

21.3.1 KEY RESOURCES

- "Enhanced Controller Area Network (ECAN™)" (DS70353) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- · Development Tools

23.2 ADC Helpful Tips

- 1. The SMPIx control bits in the AD1CON2 register:
 - a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
 - b) When the CSCNA bit in the AD1CON2 registers is set to '1', this determines when the ADC analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.
 - c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
 - d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.
- 2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
- 3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADC1BUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
- 4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.

5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for ANO, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUXA selections use ANO-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. Configuration examples are available in the "Analog-to-Digital Converter (ADC)" (DS70621) section in the "dsPIC33/ PIC24 Family Reference Manual".

23.3 ADC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the				
	product page using the link above, enter				
	this URL in your browser:				
	http://www.microchip.com/wwwproducts/				
	Devices.aspx?dDocName=en555464				

23.3.1 KEY RESOURCES

- "Analog-to-Digital Converter (ADC)" (DS70621) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

DC CHARACTERISTICS		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
	VIL	Input Low Voltage					
DI10		Any I/O Pin and MCLR	Vss	—	0.2 VDD	V	
DI18		I/O Pins with SDAx, SCLx	Vss	_	0.3 VDD	V	SMBus disabled
DI19		I/O Pins with SDAx, SCLx	Vss	_	0.8	V	SMBus enabled
	Vih	Input High Voltage					
DI20		I/O Pins Not 5V Tolerant	0.8 VDD	—	Vdd	V	(Note 3)
		I/O Pins 5V Tolerant and MCLR	0.8 VDD	—	5.5	V	(Note 3)
		I/O Pins with SDAx, SCLx	0.8 VDD	_	5.5	V	SMBus disabled
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled
	ICNPU	Change Notification Pull-up Current					
DI30			150	250	550	μA	VDD = 3.3V, VPIN = VSS
	ICNPD	Change Notification Pull-Down Current ⁽⁴⁾					
DI31			20	50	100	μA	VDD = 3.3V, VPIN = VDD

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (VSS 0.3). Characterized but not tested.

5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.