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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc204t-e-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



1.0 DEVICE OVERVIEW

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com)
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM



3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls.

3.2 Instruction Set

The instruction set for dsPIC33EPXXXGP50X and dsPIC33EPXXXMC20X/50X devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The instruction set for PIC24EPXXXGP/MC20X devices has the MCU class of instructions only and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The base Data Space can be addressed as 64 Kbytes (32K words).

The Data Space includes two ranges of memory, referred to as X and Y data memory. Each memory range is accessible through its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Spaces have memory locations that are device-specific, and are described further in the data memory maps in **Section 4.2 "Data Address Space"**.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 32-Kbyte aligned program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to the "**Data Memory**" (DS70595) and "**Program Memory**" (DS70613) sections in the "*dsPIC33/PIC24 Family Reference Manual*" for more details on EDS, PSV and table accesses.

On the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms. PIC24EPXXXGP/MC20X devices do not support Modulo and Bit-Reversed Addressing.

3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- · Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory and to program two instruction words at a time. See the General Purpose and Motor Control Family tables (Table 1 and Table 2, respectively) for the page sizes of each device.

For more information on erasing and programming Flash memory, refer to "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual".

5.3 **Programming Operations**

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time) in Table 30-14 in **Section 30.0 "Electrical Characteristics"**.

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS.

Refer to **Flash Programming**" (DS70609) in the "*dsPIC33/PIC24 Family Reference Manual*" for details and codes examples on programming using RTSP.

5.4 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

5.4.1 KEY RESOURCES

- "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

5.5 Control Registers

Four SFRs are used to erase and write the program Flash memory: NVMCON, NVMKEY, NVMADRH and NVMADRL.

The NVMCON register (Register 5-1) enables and initiates Flash memory erase and write operations.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRH and NVMADRL. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations or the selected page for erase operations.

The NVMADRH register is used to hold the upper 8 bits of the EA, while the NVMADRL register is used to hold the lower 16 bits of the EA.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_		—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
			DMA0MD ⁽¹⁾				
_	_	_	DMA1MD ⁽¹⁾	PTGMD	_	_	_
			DMA2MD ⁽¹⁾	1 TOME			
			DMA3MD ⁽¹⁾				
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown
bit 15-5	Unimplement	ted: Read as '	D'				
bit 4	DMA0MD: DN	/A0 Module Di	sable bit ⁽¹⁾				
	1 = DMA0 mo	dule is disable	d				
	0 = DMA0 mo	dule is enable	d 				
	DMA1MD: DN	/A1 Module Di	sable bit(")				
	1 = DMA1 mo 0 = DMA1 mo	dule is disable	d d				
			sable bit(1)				
	1 = DMA2 mo	dule is disable	d				
	0 = DMA2 mo	dule is enable	d				
	DMA3MD: DN	/A3 Module Di	sable bit ⁽¹⁾				
	1 = DMA3 mo	dule is disable	d				
	0 = DMA3 mo	dule is enable	b				
bit 3	PTGMD: PTG	Module Disab	le bit				
	1 = PTG mod	ule is disabled					
	$0 = PIG \mod 1$	uie is enabled	-1				
DIT 2-0	Unimplement	tea: Read as '	J.				
Note 1: Th	nis single bit ena	ables and disat	oles all four DM	A channels.			

REGISTER 10-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the op amp/ comparator module (see Figure 25-1 in Section 25.0 "Op Amp/Comparator Module"), and the PTG module (see Section 24.0 "Peripheral Trigger Generator (PTG) Module").

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QEI module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)".

Virtual connections provide a simple way of interperipheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of `b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEI module allows peripherals to be connected to the QEI digital filter input. To utilize this filter, the QEI module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEI digital filter.

EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE

RPINR15 = 0x2500;	/* Connect the QEI1 HOME1 input to RP37 (pin 43) */
RPINR7 = 0x009;	/* Connect the IC1 input to the digital filter on the FHOME1 input */
QEI1IOC = 0x4000;	/* Enable the QEI digital filter */
QEI1CON = 0x8000;	/* Enable the QEI module */

11.4.4.2 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 11-18 through Register 11-27). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 11-3: MULTIPLEXING REMAPPABLE OUTPUT FOR RPn



11.4.4.3 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-toone and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPxR<5:0> Output Name			
Default PORT	000000	RPn tied to Default Pin		
U1TX	000001	RPn tied to UART1 Transmit		
U2TX	000011	RPn tied to UART2 Transmit		
SDO2	001000	RPn tied to SPI2 Data Output		
SCK2	001001	RPn tied to SPI2 Clock Output		
SS2	001010	RPn tied to SPI2 Slave Select		
C1TX ⁽²⁾	001110	RPn tied to CAN1 Transmit		
OC1	010000	RPn tied to Output Compare 1 Output		
OC2	010001	RPn tied to Output Compare 2 Output		
OC3	010010	RPn tied to Output Compare 3 Output		
OC4	010011	RPn tied to Output Compare 4 Output		
C1OUT	011000	RPn tied to Comparator Output 1		
C2OUT	011001	RPn tied to Comparator Output 2		
C3OUT	011010	RPn tied to Comparator Output 3		
SYNCO1 ⁽¹⁾	101101	RPn tied to PWM Primary Time Base Sync Output		
QEI1CCMP ⁽¹⁾	101111	RPn tied to QEI 1 Counter Comparator Output		
REFCLKO	110001	RPn tied to Reference Clock Output		
C4OUT	110010	RPn tied to Comparator Output 4		

Note 1: This function is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This function is available in dsPIC33EPXXXGP/MC50X devices only.

REGISTER 11-16: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38 (dsPIC33EPXXXMC20X AND PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				DTCMP1R<6:	0>		
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—	_		—	—	_	—
bit 7		·		÷			bit 0
Legend:							
R = Readabl	e bit	W = Writable bit U = Unimplemented bit, read as '0				l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown	
bit 15	Unimplemer	ted: Read as '	0'				
bit 14-8	DTCMP1R<6 (see Table 11	::0>: Assign PV -2 for input pin	VM Dead-Tim selection nun	e Compensation nbers)	on Input 1 to the	e Correspondine	g RPn Pin bits
	1111001 = 	nput tied to RPI	121				
	•						
	•						
	0000001 =	nput tied to CM	P1				
	0000000 = li	nput tied to Vss	}				
bit 7-0	Unimplemer	ted: Read as '	0'				

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)

- bit 3 TRIGMODE: Trigger Status Mode Select bit
 - 1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
 - 0 = TRIGSTAT is cleared only by software
- bit 2-0 OCM<2:0>: Output Compare x Mode Select bits
 - 111 = Center-Aligned PWM mode: Output set high when OCxTMR = OCxR and set low when OCxTMR = OCxRS⁽¹⁾
 - 110 = Edge-Aligned PWM mode: Output set high when OCxTMR = 0 and set low when OCxTMR = OCxR⁽¹⁾
 - 101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS
 - 100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle
 - 011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin
 - 010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low
 - 001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high
 - 000 = Output compare channel is disabled
- Note 1: OCxR and OCxRS are double-buffered in PWM mode only.
 - 2: Each Output Compare x module (OCx) has one PTG clock source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.
 - PTGO4 = OC1 PTGO5 = OC2
 - PTGO6 = OC3 PTGO7 = OC4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0	
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	
PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, reac	l as '0'		
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown	
bit 15-13 PTGCLK<2:0>: Select PTG Module Clock Source bits 111 = Reserved 110 = Reserved 101 = PTG module clock source will be T3CLK 100 = PTG module clock source will be T2CLK 011 = PTG module clock source will be T1CLK 010 = PTG module clock source will be TAD 001 = PTG module clock source will be Fosc 000 = PTG module clock source will be FP bit 12-8 PTGDIV<4:0>: PTG Module Clock Prescaler (divider) bits								
	11111 = Divic 11110 = Divic • • • • • • • • • • • • • • • • • • •	de-by-32 de-by-31 de-by-2 de-by-1						
bit 7-4	PTGPWD<3:0	0>: PTG Trigge	er Output Pulse	e-Width bits				
	<pre>1111 = All trigger outputs are 16 PTG clock cycles wide 1110 = All trigger outputs are 15 PTG clock cycles wide</pre>							
bit 3	Unimplemen	ted: Read as '	0'					
bit 2-0	PTGWDT<2:0	0>: Select PTG	Watchdog Tir	mer Time-out	Count Value bits	3		
	PTGWDT<2:0>: Select PTG Watchdog Timer Time-out Count Value bits 111 = Watchdog Timer will time-out after 512 PTG clocks 110 = Watchdog Timer will time-out after 256 PTG clocks 101 = Watchdog Timer will time-out after 128 PTG clocks 100 = Watchdog Timer will time-out after 64 PTG clocks 011 = Watchdog Timer will time-out after 32 PTG clocks 010 = Watchdog Timer will time-out after 16 PTG clocks 010 = Watchdog Timer will time-out after 8 PTG clocks 001 = Watchdog Timer will time-out after 8 PTG clocks 000 = Watchdog Timer is disabled							

REGISTER 24-2: PTGCON: PTG CONTROL REGISTER

NOTES:

Bit Field	Description
WDTPRE	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST<3:0>	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • • • • • • • • • • •
WDTWIN<1:0>	Watchdog Window Select bits 11 = WDT window is 25% of WDT period 10 = WDT window is 37.5% of WDT period 01 = WDT window is 50% of WDT period 00 = WDT window is 75% of WDT period
ALTI2C1	Alternate I2C1 pin 1 = I2C1 is mapped to the SDA1/SCL1 pins 0 = I2C1 is mapped to the ASDA1/ASCL1 pins
ALTI2C2	Alternate I2C2 pin 1 = I2C2 is mapped to the SDA2/SCL2 pins 0 = I2C2 is mapped to the ASDA2/ASCL2 pins
JTAGEN ⁽²⁾	JTAG Enable bit 1 = JTAG is enabled 0 = JTAG is disabled
ICS<1:0>	ICD Communication Channel Select bits 11 = Communicate on PGEC1 and PGED1 10 = Communicate on PGEC2 and PGED2 01 = Communicate on PGEC3 and PGED3 00 = Reserved, do not use

TABLE 27-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	С
26	DEC	DEC	f	f = f - 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws - 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws - 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF	Wm, Wn ⁽¹⁾	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO	#lit15,Expr ⁽¹⁾	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO	Wn, Expr ⁽¹⁾	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd ⁽¹⁾	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC	Wm*Wm,Acc,Wx,Wy,Wxd ⁽¹⁾	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
34	EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL	Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	С
36	FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	С
37	FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	С
38	GOTO	GOTO	Expr	Go to address	2	4	None
		GOTO	Wn	Go to indirect	1	4	None
		GOTO.L	Wn	Go to indirect (long address)	1	4	None
39	INC	INC	f	f = f + 1	1	1	C,DC,N,OV,Z
		INC	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2	f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2	f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2	Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR	f	f = f .IOR. WREG	1	1	N,Z
		IOR	f,WREG	WREG = f.IOR. WREG	1	1	N,Z
		IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC	Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
43	LNK	LNK	#lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR	f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB ⁽¹⁾	Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd ⁽¹⁾	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Тур.	Max.	Units	Conditions
ТВ10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or (TcY + 20)/N		_	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N		_	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns	

TABLE 30-24:	TIMER2 AND TI	MER4 (TYPE B TIM	ER) EXTERNAL CLOC	K TIMING REQUIREMENTS
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Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Тур.	Max.	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous, with prescaler	2 Tcy + 40	—	_	ns	N = prescale value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

FIGURE 30-11: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)



TABLE 30-30: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Тур.	Max.	Units	Conditions
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 TCY/N) + 25			ns	Must also meet Parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	_	_	ns	Must also meet Parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	Greater of 25 + 50 or (1 Tcy/N) + 50	_	_	ns	
TQ20	TCKEXTMRL	Delay from External TQCK Clock Edge to Timer Increment		_	1	Тсү	—	

Note 1: These parameters are characterized but not tested in manufacturing.

AC CHARA	CTERISTICS		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	СКР	SMP	
15 MHz	Table 30-42			0,1	0,1	0,1	
10 MHz	—	Table 30-43	—	1	0,1	1	
10 MHz	—	Table 30-44	—	0	0,1	1	
15 MHz	—	—	Table 30-45	1	0	0	
11 MHz	—	—	Table 30-46	1	1	0	
15 MHz	_	_	Table 30-47	0	1	0	
11 MHz	_	_	Table 30-48	0	0	0	

TABLE 30-41: SPI1 MAXIMUM DATA/CLOCK RATE SUMMARY

FIGURE 30-22: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS





Temperature (Celsius)

70 80 90 100 110 120

TYPICAL FRC FREQUENCY @ VDD = 3.3V



-40 -30 -20 -10

0 10 20 30 40 50 60

FIGURE 32-9:

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B

APPENDIX A: REVISION HISTORY

Revision A (April 2011)

This is the initial released version of the document.

Revision B (July 2011)

This revision includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-1.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers and Microcontrollers"	Changed all pin diagrams references of VLAP to TLA.
Section 4.0 "Memory Organization"	Updated the All Resets values for CLKDIV and PLLFBD in the System Control Register Map (see Table 4-35).
Section 5.0 "Flash Program Memory"	Updated "one word" to "two words" in the first paragraph of Section 5.2 "RTSP Operation" .
Section 9.0 "Oscillator Configuration"	Updated the PLL Block Diagram (see Figure 9-2). Updated the Oscillator Mode, Fast RC Oscillator (FRC) with divide-by-N and PLL (FRCPLL), by changing (FRCDIVN + PLL) to (FRCPLL).
	Changed (FRCDIVN + PLL) to (FRCPLL) for COSC<2:0> = 001 and NOSC<2:0> = 001 in the Oscillator Control Register (see Register 9-1).
	Changed the POR value from 0 to 1 for the DOZE<1:0> bits, from 1 to 0 for the FRCDIV<0> bit, and from 0 to 1 for the PLLPOST<0> bit; Updated the default definitions for the DOZE<2:0> and FRCDIV<2:0> bits and updated all bit definitions for the PLLPOST<1:0> bits in the Clock Divisor Register (see Register 9-2).
	Changed the POR value from 0 to 1 for the PLLDIV<5:4> bits and updated the default definitions for all PLLDIV<8:0> bits in the PLL Feedback Division Register (see Register 9-2).
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Updated the bit definitions for the IRNG<1:0> bits in the CTMU Current Control Register (see Register 22-3).
Section 25.0 "Op amp/ Comparator Module"	Updated the voltage reference block diagrams (see Figure 25-1 and Figure 25-2).

Section Name	Update Description
Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"	Updated the High-Speed PWM Module Register Interconnection Diagram (see Figure 16-2). Added the TRGCONx and TRIGx registers (see Register 16-12 and Register 16-14, respectively).
Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Updated the IRNG<1:0> bit value definitions and added Note 2 in the CTMU Current Control Register (see Register 22-3).
Section 25.0 "Op amp/ Comparator Module"	Updated the Op amp/Comparator I/O Operating Modes Diagram (see Figure 25-1). Updated the User-programmable Blanking Function Block Diagram (see Figure 25-3). Updated the Digital Filter Interconnect Block Diagram (see Figure 25-4). Added Section 25.1 "Op amp Application Considerations ". Added Note 2 to the Comparator Control Register (see Register 25-2). Updated the bit definitions in the Comparator Mask Gating Control Register (see Register 25-5).
Section 27.0 "Special Features"	Updated the FICD Configuration Register, updated Note 1, and added Note 3 in the Configuration Byte Register Map (see Table 27-1). Added Section 27.2 " User ID Words ".
Section 30.0 "Electrical Characteristics"	 Updated the following Absolute Maximum Ratings: Maximum current out of Vss pin Maximum current into VDD pin Added Note 1 to the Operating MIPS vs. Voltage (see Table 30-1).
	Updated all Idle Current (IIDLE) Typical and Maximum DC Characteristics values (see Table 30-7).
	Updated all Doze Current (IDOZE) Typical and Maximum DC Characteristics values (see Table 30-9).
	Added Note 2, removed Parameter CM24, updated the Typical values Parameters CM10, CM20, CM21, CM32, CM41, CM44, and CM45, and updated the Minimum values for CM40 and CM41, and the Maximum value for CM40 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).
	Updated Note 2 and the Typical value for Parameter VR310 in the Op amp/ Comparator Reference Voltage Settling Time Specifications (see Table 30-15).
	Added Note 1, removed Parameter VRD312, and added Parameter VRD314 to the Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).
	Updated the Minimum, Typical, and Maximum values for Internal LPRC Accuracy (see Table 30-22).
	Updated the Minimum, Typical, and Maximum values for Parameter SY37 in the Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer Timing Requirements (see Table 30-24).
	The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-35)

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)