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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Ξ·ΧΕΙ

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc204t-i-mv

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 3 MHz < F_{IN} < 5.5 MHz to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between Vss and unused pins, and drive the output to logic low.

2.9 Application Examples

- · Induction heating
- Uninterruptable Power Supplies (UPS)
- DC/AC inverters
- · Compressor motor control
- · Washing machine 3-phase motor control
- BLDC motor control
- · Automotive HVAC, cooling fans, fuel pumps
- Stepper motor control
- · Audio and fluid sensor monitoring
- · Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- Consumer audio
- Industrial and building control (security systems and access control)
- · Barcode reading
- Networking: LAN switches, gateways
- Data storage device management
- · Smart cards and smart card readers

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION





FIGURE 4-5: PROGRAM MEMORY MAP FOR dsPIC33EP512GP50X, dsPIC33EP512MC20X/50X AND PIC24EP512GP/MC20X DEVICES

TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC35	0886	_		JTAGIP<2:0)>	—		ICDIP<2:0	>	_	—	—	_	—	_	-		4400
IPC36	0888	-	l	PTG0IP<2:0)>	_	PT	GWDTIP<	2:0>	_	P	TGSTEPIP<2	:0>	—	—			4440
IPC37	088A		_	_	_	_	F	PTG3IP<2:0)>	_		PTG2IP<2:0>	>	_	F	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL		0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	_			—	_	—	—	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	_	_	—	—	—	_			—	_	DAE	DOOVR	_	—			0000
INTCON4	08C6	-	_	—	_	_	_		_	_	_	—	—	—	—	_	SGHT	0000
INTTREG	08C8	-	—	—	_		ILR<	3:0>					VECNU	M<7:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

NOTES:

					UNIRUL RE		
U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	_	—	—	—	CMPMD	—	—
bit 15							bit 8
R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
CRCMD	—	—	_	—	—	I2C2MD	—
bit 7							bit C
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimplem	ented bit, read	l as '0'	
-n = Value at POR '1' = Bit is set			'0' = Bit is clea	ared	x = Bit is unknown		

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

bit 10	CMPMD: Comparator Module Disable bit
	1 = Comparator module is disabled
	0 = Comparator module is enabled
bit 9-8	Unimplemented: Read as '0'
bit 7	CRCMD: CRC Module Disable bit
	1 = CRC module is disabled
	0 = CRC module is enabled
bit 6-2	Unimplemented: Read as '0'
bit 1	I2C2MD: I2C2 Module Disable bit
	1 = I2C2 module is disabled
	0 = I2C2 module is enabled
bit 0	Unimplemented: Read as '0'

REGISTER 10-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

	-						
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—				—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
—	—	—	—	REFOMD	CTMUMD	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4	Unimplemented: Read as '0'
bit 3	REFOMD: Reference Clock Module Disable bit
	 1 = Reference clock module is disabled
	0 = Reference clock module is enabled
bit 2	CTMUMD: CTMU Module Disable bit
	1 = CTMU module is disabled
	0 = CTMU module is enabled
bit 1-0	Unimplemented: Read as '0'

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11.0 I/O PORTS

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "I/O Ports" (DS70598) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

Many of the device pins are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

Generally, a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through," in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

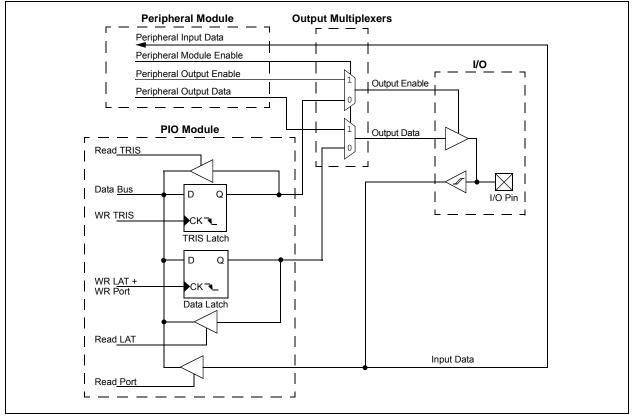
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have eight registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Latch register (LATx) read the latch. Writes to the Latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device is disabled. This means the corresponding LATx and TRISx registers and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.





REGISTER 11-17: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				DTCMP3R<6:0)>		
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
0-0	R/W-0	R/W-0	-	DTCMP2R<6:0		R/W-0	R/W-U
bit 7					17		bit 0
bit i							bit 0
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimplem	nented bit, rea	ad as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
		nput tied to CMI					
bit 7	1 = 0000000 = Ir	nput tied to CMI nput tied to Vss nted: Read as '(

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
CHPCLKEN	—	—	—	—	—	CHOPC	LK<9:8>
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			CHOPC	LK<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimplei	mented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 15 bit 14-10 bit 9-0	1 = Chop clos 0 = Chop clos Unimplemen CHOPCLK<9 The frequence	Enable Chop ck generator is ck generator is ted: Read as ' 9:0>: Chop Clo y of the chop c ncy = (FP/PCL)	enabled disabled 0' ck Divider bits lock signal is g	given by the fo	ollowing expressi + 1)	on:	

REGISTER 16-5: CHOP: PWMx CHOP CLOCK GENERATOR REGISTER

REGISTER 16-6: MDC: PWMx MASTER DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MDC	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MD	C<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	bit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unk					x = Bit is unkr	nown	

bit 15-0 MDC<15:0>: PWMx Master Duty Cycle Value bits

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
QCAPEN	FLTREN	QFDIV2	QFDIV1	QFDIV0	OUTFNC1	OUTFNC0	SWPAB					
bit 15	·	·					bit 8					
R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x					
HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA					
bit 7				TIOME	INDEX	QLD	bit (
Legend:												
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'						
-n = Value at		'1' = Bit is set		'0' = Bit is cle		x = Bit is unkn	own					
bit 15	QCAPEN: Q	EI Position Cou	nter Input Cap	ture Enable bit								
		tch event trigge										
		tch event does		-								
bit 14		Ax/QEBx/INDX	•	tal Filter Enable	e dit							
		digital filter is e digital filter is d		sed)								
bit 13-11	• •	•			Iter Clock Divid	le Select bits						
	QFDIV<2:0>: QEAx/QEBx/INDXx/HOMEx Digital Input Filter Clock Divide Select bits 111 = 1:128 clock divide											
	110 = 1:64 cl	lock divide										
	101 = 1:32 clock divide											
		100 = 1:16 clock divide 011 = 1:8 clock divide										
	011 = 1:8 clock divide 010 = 1:4 clock divide											
	001 = 1.2 clock divide											
	000 = 1:1 clo											
bit 10-9	OUTFNC<1:	0>: QEI Module	Output Functi	on Mode Selec	ct bits							
		NCMPx pin goe	-			GEC						
		NCMPx pin goe										
		NCMPx pin goe	s high when P	$OS1CNT \ge QE$	IIGEC							
L:1 0	00 = Output i											
bit 8		ap QEA and QE	•									
		d QEBx are sw d QEBx are not		quadrature dec	coder logic							
bit 7	HOMPOL: H	OMEx Input Po	larity Select bit									
	1 = Input is in											
bit 6	0 = Input is n		ty Soloot bit									
	1 = Input is in	OXx Input Polari	ly Select bit									
	0 = Input is n											
bit 5	-	EBx Input Polar	itv Select bit									
	1 = Input is i	•	.,									
	0 = Input is r											
bit 4	QEAPOL: Q	EAx Input Polar	ity Select bit									
	1 = Input is i											
	0 = Input is r	not inverted										
bit 3	HOME: Statu											
DIL 3	HOME . Statu		out Pin Alter Po	olarity Control								
DIL 3	1 = Pin is at 0 = Pin is at	logic '1'	out Pin Aiter Po	bianty Control								

REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
		QEIG	EC<31:24>					
						bit 8		
	DAMO				DAMO			
R/W-U	R/W-0			R/W-U	R/W-U	R/W-0		
		QEIGE	EC<23:16>					
						bit (
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'					
-n = Value at POR '1' = Bit is set			'0' = Bit is clea	ared	x = Bit is unknown			
		W = Writable bi	R/W-0 R/W-0 QEIGI W = Writable bit	R/W-0 R/W-0 R/W-0 QEIGEC<23:16> W = Writable bit U = Unimplem	R/W-0 R/W-0 R/W-0 QEIGEC<23:16> W = Writable bit U = Unimplemented bit, real	R/W-0 R/W-0 R/W-0 R/W-0 QEIGEC<23:16> U = Unimplemented bit, read as '0'		

REGISTER 17-15: QEI1GECH: QEI1 GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER

bit 15-0 QEIGEC<31:16>: High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

REGISTER 17-16: QEI1GECL: QEI1 GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	C<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIG	EC<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cle	ared	x = Bit is unki	nown	

bit 15-0 QEIGEC<15:0>: Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

REGISTER 18-1: SPIx STAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 1 SPITBF: SPIx Transmit Buffer Full Status bit
 - 1 = Transmit not yet started, SPIxTXB is full
 - 0 = Transmit started, SPIxTXB is empty

Standard Buffer mode:

Automatically set in hardware when core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer mode:

Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 SPIRBF: SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full

0 = Receive is incomplete, SPIxRXB is empty

Standard Buffer mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

-								
R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC	
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	
bit 15							bit 8	
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	
bit 7							bit 0	
Legend:	Legend: C = Clearable bit			HS = Hardware Settable bit HSC = Hardware Settable/Clearable bit				
R = Readab	le bit	W = Writable	e bit	U = Unimplen	nented bit, read	as '0'		
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unki					

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

hit 15	ACKSTAT: Acknowledge Status bit (when operating as I ² C™ master, applicable to master transmit operation)
bit 15	1 = NACK received from slave
	0 = ACK received from slave
	Hardware is set or clear at the end of slave Acknowledge.
bit 14	TRSTAT: Transmit Status bit (when operating as I ² C master, applicable to master transmit operation)
	1 = Master transmit is in progress (8 bits + ACK)
	0 = Master transmit is not in progress
	Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
bit 13-11	Unimplemented: Read as '0'
bit 10	BCL: Master Bus Collision Detect bit
	1 = A bus collision has been detected during a master operation
	0 = No bus collision detected Hardware is set at detection of a bus collision.
bit 9	GCSTAT: General Call Status bit
DIL 9	1 = General call address was received
	0 = General call address was not received
	Hardware is set when address matches general call address. Hardware is clear at Stop detection.
bit 8	ADD10: 10-Bit Address Status bit
	1 = 10-bit address was matched
	0 = 10-bit address was not matched
	Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
bit 7	IWCOL: I2Cx Write Collision Detect bit
	1 = An attempt to write to the I2CxTRN register failed because the I ² C module is busy
	1 = An attempt to write to the 120x million register laned because the 1-0 module is busy 0 = No collision
	Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
bit 6	I2COV: I2Cx Receive Overflow Flag bit
	1 = A byte was received while the I2CxRCV register was still holding the previous byte
	0 = No overflow
	Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
bit 5	D_A: Data/Address bit (when operating as I ² C slave)
	 I = Indicates that the last byte received was data I = Indicates that the last byte received was a device address
	Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.

REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0
bit 15							bit 8

| R/W-0 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

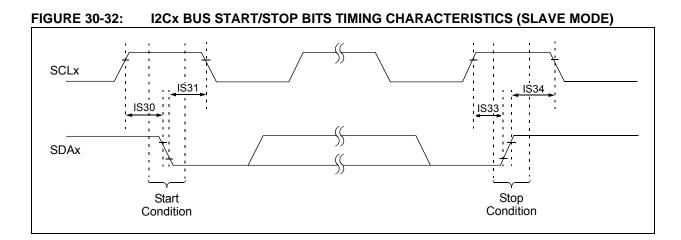
bit 15-12 Unimplemented: Read as '0'

DIL 10-12	Uninpienenteu. Reau as 0
bit 11-8	SELSRCC<3:0>: Mask C Input Select bits
	1111 = FLT4
	1110 = FLT2
	1101 = PTGO19
	1100 = PTGO18
	1011 = Reserved
	1010 = Reserved
	1001 = Reserved
	1000 = Reserved
	0111 = Reserved
	0110 = Reserved
	0101 = PWM3H
	0100 = PWM3L
	0011 = PWM2H
	0010 = PWM2L
	0001 = PWM1H
	0000 = PWM1L
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4
bit 7-4	1111 = FLT4 1110 = FLT2
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0111 = Reserved 0110 = Reserved 0110 = Reserved 0101 = PWM3H
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0111 = Reserved 0110 = Reserved 0110 = Reserved 0101 = PWM3H 0100 = PWM3L
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0111 = Reserved 0110 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0111 = Reserved 0111 = Reserved 0110 = Reserved 0101 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L
bit 7-4	1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0111 = Reserved 0110 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H

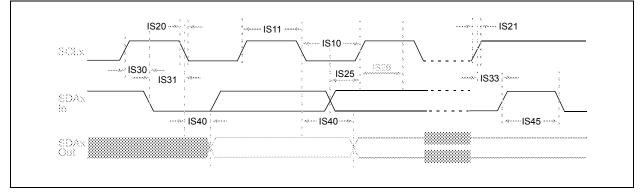
26.3 Programmable CRC Registers

REGISTER 26-1: CRCCON1: CRC CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0
CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0
bit 15	·						bit 8
R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	_	_	_
bit 7	•						bit (
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	0 = CRC mo	dule is enabled		chines, pointer	s and CRCWD	AT/CRCDAT a	re reset, othe
bit 14	Unimplemen	ted: Read as '	0'				
bit 13	CSIDL: CRC	Stop in Idle Mo	ode bit				
		nues module op es module opera			Idle mode		
				oue			
bit 12-8	VWORD<4:0	>: Pointer Value		oue			
bit 12-8	Indicates the		e bits		naximum value	of 8 when PLE	N<4:0> > 7
	Indicates the or 16 when P	number of valio	e bits d words in the		naximum value	of 8 when PLE	N<4:0> > 7
	Indicates the or 16 when P	number of valic LEN<4:0> \leq 7. C FIFO Full bit ull	e bits d words in the		naximum value	of 8 when PLE	N<4:0> > 7
bit 7	Indicates the or 16 when P CRCFUL : CR 1 = FIFO is fi 0 = FIFO is r	number of valic LEN<4:0> \leq 7. C FIFO Full bit ull	e bits d words in the		naximum value	of 8 when PLE	N<4:0> > 7
bit 7	Indicates the or 16 when P CRCFUL : CR 1 = FIFO is fi 0 = FIFO is r CRCMPT : CF 1 = FIFO is e	number of valic LEN<4:0> \leq 7. C FIFO Full bit ull not full RC FIFO Empty empty	e bits d words in the		naximum value	of 8 when PLE	N<4:0> > 7
bit 7 bit 6	Indicates the or 16 when P CRCFUL : CR 1 = FIFO is fi 0 = FIFO is r CRCMPT : CF 1 = FIFO is e 0 = FIFO is r	number of valic LEN<4:0> \leq 7. RC FIFO Full bit ull not full RC FIFO Empty empty not empty	e bits d words in the : Bit		naximum value	of 8 when PLE	N<4:0> > 7
bit 7 bit 6	Indicates the or 16 when P CRCFUL: CR 1 = FIFO is f 0 = FIFO is r CRCMPT: CF 1 = FIFO is r 0 = FIFO is r CRCISEL: CF	number of valic LEN<4:0> \leq 7. RC FIFO Full bit ull not full RC FIFO Empty empty not empty RC Interrupt Se	e bits d words in the Bit election bit	FIFO. Has a m			N<4:0> > 7
bit 7 bit 6	Indicates the or 16 when P CRCFUL : CR 1 = FIFO is f 0 = FIFO is r CRCMPT : CF 1 = FIFO is r CRCISEL : Cf 1 = Interrupt	number of valic LEN<4: $0> \leq 7$. C FIFO Full bit ull not full RC FIFO Empty empty not empty RC Interrupt Se on FIFO is empty	e bits d words in the Bit election bit oty; final word	FIFO. Has a model of data is still s	shifting through		N<4:0> > 7
bit 7 bit 6 bit 5	Indicates the or 16 when P CRCFUL : CR 1 = FIFO is f 0 = FIFO is r CRCMPT : CF 1 = FIFO is r CRCISEL : Cf 1 = Interrupt	number of valic LEN<4:0> \leq 7. C FIFO Full bit ull act full C FIFO Empty mot empty act empty RC Interrupt Se on FIFO is emp on shift is comp	e bits d words in the Bit election bit oty; final word	FIFO. Has a model of data is still s	shifting through		N<4:0> > 7
bit 7 bit 6 bit 5	Indicates the or 16 when P CRCFUL: CR 1 = FIFO is fi 0 = FIFO is r CRCMPT: CF 1 = FIFO is r CRCISEL: CF 1 = Interrupt 0 = Interrupt CRCGO: Star	number of valic LEN<4:0> \leq 7. C FIFO Full bit ull act full C FIFO Empty mot empty act empty RC Interrupt Se on FIFO is emp on shift is comp	e bits d words in the Bit election bit pty; final word plete and CR0	FIFO. Has a model of data is still s	shifting through		N<4:0> > 7
bit 7 bit 6 bit 5 bit 4	Indicates the or 16 when P CRCFUL: CR 1 = FIFO is f 0 = FIFO is r CRCMPT: CF 1 = FIFO is r CRCISEL: CF 1 = Interrupt 0 = Interrupt CRCGO: Star 1 = Starts CF	number of valic LEN<4:0> \leq 7. C FIFO Full bit ull not full RC FIFO Empty empty not empty RC Interrupt Se on FIFO is emp on shift is comp t CRC bit	e bits d words in the Bit election bit oty; final word plete and CRC	FIFO. Has a model of data is still s	shifting through		N<4:0> > 7
bit 7 bit 6 bit 5 bit 4	Indicates the or 16 when P CRCFUL: CR 1 = FIFO is f 0 = FIFO is f 1 = FIFO is f 0 = FIFO is f 0 = FIFO is f CRCISEL: CF 1 = Interrupt 0 = Interrupt CRCGO: Star 1 = Starts CF 0 = CRC seri LENDIAN: Da	number of valic LEN<4:0> \leq 7. RC FIFO Full bit ull not full RC FIFO Empty mot empty RC Interrupt Se on FIFO is emp on shift is comp on shift is comp rt CRC bit RC serial shifter ial shifter is turr ata Word Little-	e bits d words in the d bit Bit election bit oty; final word plete and CRC ned off Endian Config	FIFO. Has a m of data is still s CWDAT results	shifting through are ready	CRC	N<4:0> > 7
bit 7 bit 6 bit 5	Indicates the or 16 when P CRCFUL: CR 1 = FIFO is fi 0 = FIFO is r CRCMPT: CF 1 = FIFO is r CRCISEL: CF 1 = Interrupt 0 = Interrupt CRCGO: Star 1 = Starts CF 0 = CRC ser LENDIAN: Da 1 = Data wor	number of valic LEN<4:0> \leq 7. C FIFO Full bit ull not full RC FIFO Empty mot empty RC Interrupt Se on FIFO is emp on shift is comp rt CRC bit RC serial shifter ial shifter is turr ata Word Little- rd is shifted into	e bits d words in the d bit Bit election bit oty; final word plete and CRC ned off Endian Config the CRC star	FIFO. Has a m of data is still s CWDAT results guration bit ting with the LS	shifting through are ready Sb (little endiar	ı CRC	N<4:0> > 7
bit 7 bit 6 bit 5 bit 4	Indicates the or 16 when P CRCFUL: CR 1 = FIFO is fi 0 = FIFO is r CRCMPT: CF 1 = FIFO is r CRCISEL: CF 1 = Interrupt 0 = Interrupt CRCGO: Star 1 = Starts CF 0 = CRC seri LENDIAN: Da 1 = Data wor 0 = Data wor	number of valic LEN<4:0> \leq 7. RC FIFO Full bit ull not full RC FIFO Empty mot empty RC Interrupt Se on FIFO is emp on shift is comp on shift is comp rt CRC bit RC serial shifter ial shifter is turr ata Word Little-	e bits d words in the d words in the d words in the d words in the d words in the bits bits bits contain the the the d words contain the the the d words in the d word words in the d word words in the d word words in the d words in the d word words in the d words in the d word words in the d words in the d words in the the d words in the the d words in the the d words in the the d word words in the the d word words in the the d word words in the the the d words in the	FIFO. Has a m of data is still s CWDAT results guration bit ting with the LS	shifting through are ready Sb (little endiar	ı CRC	N<4:0> > 7







	RACTERI	STICS		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param. No.		Characte	Min.	Max.	Units	Conditions		
IS10 TLO:SCL		Clock Low Time	100 kHz mode	4.7	_	μS		
			400 kHz mode	1.3	—	μS		
			1 MHz mode ⁽¹⁾	0.5	—	μS		
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μS	Device must operate at a minimum of 1.5 MHz	
			400 kHz mode	0.6	—	μS	Device must operate at a minimum of 10 MHz	
			1 MHz mode ⁽¹⁾	0.5	—	μS		
IS20	TF:SCL	SDAx and SCLx	100 kHz mode		300	ns	CB is specified to be from	
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode ⁽¹⁾	—	100	ns		
IS21	TR:SCL	SDAx and SCLx	100 kHz mode		1000	ns	CB is specified to be from	
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode ⁽¹⁾		300	ns		
IS25	TSU:DAT	Data Input	100 kHz mode	250	—	ns		
	Setup Time		400 kHz mode	100	—	ns		
			1 MHz mode ⁽¹⁾	100	_	ns		
IS26	THD:DAT	Data Input	100 kHz mode	0	—	μS		
		Hold Time	400 kHz mode	0	0.9	μS		
			1 MHz mode ⁽¹⁾	0	0.3	μS		
IS30	TSU:STA	Start Condition	100 kHz mode	4.7	—	μS	Only relevant for Repeated	
		Setup Time	400 kHz mode	0.6	—	μS	Start condition	
			1 MHz mode ⁽¹⁾	0.25	—	μS		
IS31	THD:STA	Start Condition	100 kHz mode	4.0	—	μS	After this period, the first	
		Hold Time	400 kHz mode	0.6	—	μS	clock pulse is generated	
			1 MHz mode ⁽¹⁾	0.25	—	μS		
IS33	Tsu:sto	Stop Condition	100 kHz mode	4.7	—	μS		
		Setup Time	400 kHz mode	0.6	—	μS		
			1 MHz mode ⁽¹⁾	0.6	_	μS		
IS34	THD:STO	Stop Condition	100 kHz mode	4	—	μS		
		Hold Time	400 kHz mode	0.6	—	μS		
			1 MHz mode ⁽¹⁾	0.25		μS		
IS40	TAA:SCL	Output Valid	100 kHz mode	0	3500	ns		
		From Clock	400 kHz mode	0	1000	ns		
			1 MHz mode ⁽¹⁾	0	350	ns		
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μS	Time the bus must be free	
			400 kHz mode	1.3	—	μS	before a new transmission	
			1 MHz mode ⁽¹⁾	0.5		μs	can start	
IS50	Св	Bus Capacitive Lo	ading	—	400	pF		
S51	TPGD	Pulse Gobbler De	lay	65	390	ns	(Note 2)	

TABLE 30-50: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: Typical value for this parameter is 130 ns.

3: These parameters are characterized, but not tested in manufacturing.

DC CH/	ARACTERIS	TICS	$ \begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)}^{(1)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array} $						
Param No.	Symbol Characteristic		Min.	Тур. ⁽²⁾	Max.	Units	Conditions		
Op Am	p DC Chara	cteristics							
CM40	VCMR	Common-Mode Input Voltage Range	AVss	_	AVDD	V			
CM41	CMRR	Common-Mode Rejection Ratio ⁽³⁾	—	40	—	db	VCM = AVDD/2		
CM42	VOFFSET	Op Amp Offset Voltage ⁽³⁾	—	±5	—	mV			
CM43	Vgain	Open-Loop Voltage Gain ⁽³⁾	_	90	_	db			
CM44	los	Input Offset Current	_	-	_	_	See pad leakage currents in Table 30-11		
CM45	lв	Input Bias Current	_	_	—	_	See pad leakage currents in Table 30-11		
CM46	Ιουτ	Output Current	_		420	μA	With minimum value of RFEEDBACK (CM48)		
CM48	RFEEDBACK	Feedback Resistance Value	8	-	_	kΩ			
CM49a	VOADC	Output Voltage	AVss + 0.077		AVDD - 0.077	V	Ιουτ = 420 μΑ		
		Measured at OAx Using ADC ^(3,4)	AVss + 0.037 AVss + 0.018		AVDD – 0.037 AVDD – 0.018	V V	ΙΟυΤ = 200 μΑ Ιουτ = 100 μΑ		
CM49b	Vout	Output Voltage	AVss + 0.210	_	AVDD - 0.210	V	Ιουτ = 420 μΑ		
		Measured at OAxOUT Pin ^(3,4,5)	AVss + 0.100 AVss + 0.050	_	AVDD – 0.100 AVDD – 0.050	V V	Ιουτ = 200 μΑ Ιουτ = 100 μΑ		
CM51	RINT1 ⁽⁶⁾	Internal Resistance 1 (Configuration A and B) ^(3,4,5)	198	264	317	Ω	Min = -40°C Typ = +25°C Max = +125°C		

TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS (CONTINUED)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
- **3:** Parameter is characterized but not tested in manufacturing.
- 4: See Figure 25-6 for configuration information.
- 5: See Figure 25-7 for configuration information.
- 6: Resistances can vary by ±10% between op amps.

TABLE 31-11: INTERNAL RC ACCURACY

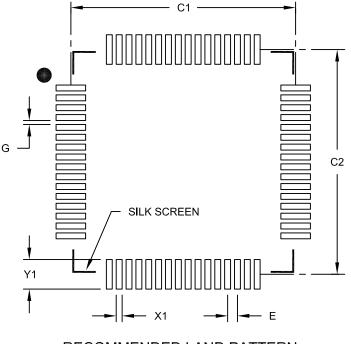
AC CH	ARACTERISTICS	RISTICSStandard Operating Conditions: 3.0V to 3.6V (unless otherwise states the operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$					herwise stated)		
Param No.	Characteristic	Min	Тур	Max	Units	Conditions			
	LPRC @ 32.768 kHz ^(1,2)								
HF21	LPRC	-30	_	+30	%	$-40^{\circ}C \le TA \le +150^{\circ}C VDD = 3.0-3.6V$			

Note 1: Change of LPRC frequency as VDD changes.

2: LPRC accuracy impacts the Watchdog Timer Time-out Period (TwDT). See Section 27.5 "Watchdog Timer (WDT)" for more information.

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimensio	MIN	NOM	MAX	
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

PMD (PIC24EPXXXMC20X Devices)	
PORTA (PIC24EPXXXGP/MC202,	
dsPIC33EPXXXGP/MC202/502 Devices) 104	,
PORTA (PIC24EPXXXGP/MC203,	
dsPIC33EPXXXGP/MC203/503 Devices) 103	5
PORTA (PIC24EPXXXGP/MC204,	
dsPIC33EPXXXGP/MC204/504 Devices) 102	,
PORTA (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices)	,
PORTB (PIC24EPXXXGP/MC202,	,
dsPIC33EPXXXGP/MC202/502 Devices) 104	
PORTB (PIC24EPXXXGP/MC203,	
dsPIC33EPXXXGP/MC203/503 Devices) 103	5
PORTB (PIC24EPXXXGP/MC204,	
dsPIC33EPXXXGP/MC204/504 Devices) 102	2
PORTB (PIC24EPXXXGP/MC206,	
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PORTC (PIC23EPXXXGP/MC203,	
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dsPIC33EPXXXGP/MC204/504 Devices) 102	
PORTC (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices))
PORTD (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices) 100)
PORTE (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices) 100)
PORTF (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices) 100	`
,	,
PORTG (PIC24EPXXXGP/MC206 and	
dsPIC33EPXXXGP/MC206/506 Devices) 101	
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